Dielectric Films for Advanced Microelectronics

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Dielectric Films for Advanced Microelectronics

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Series Preface

WILEY SERIES IN MATERIALS FOR ELECTRONIC AND OPTOELECTRONIC APPLICATIONS

This book series is devoted to the rapidly developing class of materials used for electronic and optoelectronic applications. It is designed to provide much-needed information on the fundamental scientific principles of these materials, together with how these are employed in technological applications. The books are aimed at postgraduate students, researchers and technologists engaged in research, development and the study of materials in electronics and photonics, and industrial scientists developing new materials, devices and circuits for the electronic, optoelectronic and communications industries.

The development of new electronic and optoelectronic materials depends not only on materials engineering at a practical level, but also on a clear understanding of the properties of materials, and the fundamental science behind these properties. It is the properties of a material that eventually determine its usefulness in an application. The series therefore also includes such titles as electrical conduction in solids, optical properties, thermal properties, etc., all with applications and examples of materials in electronics and optoelectronics. The characterization of materials is also covered within the series in as much as it is impossible to develop new materials without the proper characterization of their structure and properties. Structure–property relationships have always been fundamentally and intrinsically important to materials science and engineering.

Materials science is well known for being one of the most interdisciplinary sciences. It is the interdisciplinary aspect of materials science that has led to many exciting discoveries, new materials and new applications. It is not unusual to find scientists with a chemical engineering background working on materials projects with applications in electronics. In selecting titles for the series, we have tried to maintain the interdisciplinary aspect of the field, and hence its excitement to researchers in this field.

PETER CAPPER
SAFA KASAP
ARTHUR WILLOUGHBY

Preface

The excellent dielectric properties of silicon dioxide (SiO_2) have aided the evolution of microelectronics during the past 40 years. Silicon dioxide, which can be formed by thermal oxidation, has low defect density, and provides a thermodynamically stable interface. SiO_2 is characterized by a high resistivity, excellent dielectric strength, and a large bandgap. Silica films prepared either by thermal oxidation of silicon or by deposition have been successfully used for both gate and interconnect applications in ultra-large-scale integration (ULSI) devices.

However, in a continuous drive to increase integrated circuit performance through shrinkage of the circuit elements, the dimensions of MOSFETs (metal–oxide–silicon field effect transistors) and other devices have been scaled according to a trend known as Moore's law. Moore's law predicts the exponential growth of chip complexity due to decreasing minimum feature size, concurrent with improvements in circuit speed, memory capacity, and cost per bit. Starting from a certain feature size, this results in opposing requirements for the properties of gate and interlayer (ILD) dielectric films. Dielectric films for gate applications need to have higher dielectric constant, while interconnect dielectric materials need to have lower dielectric constant, compared with SiO_2.

In order to maintain the high drive current and gate capacitance required of scaled MOSFETs, SiO_2 gate dielectrics have decreased in thickness from hundreds of nanometers 40 years ago to less than 2 nm today, with a continued effort to shrink to a thickness below 1 nm. However, SiO_2 layers thinner than 1.2 nm do not have the insulating properties required of a gate dielectric. The use of ultrathin SiO_2 gate dielectrics gives rise to a number of problems, including high gate leakage current, reduced drive current, poor resistance to impurity diffusion, and reliability degradation. Therefore, alternative gate dielectric materials, with small 'equivalent oxide thickness' (EOT) are required. Equivalent oxide thickness, $t_{ox}(\text{eq})$, is the thickness of the SiO_2 layer ($k = 3.9$) having the same capacitance as a given physical thickness of an alternative dielectric layer, t_{diel}:

$$t_{ox}(\text{eq}) = t_{diel}(3.9/k_{diel})$$

Therefore, to obtain a small EOT while maintaining the bulk properties of the dielectric material, the k_{diel} should be significantly higher than the value typical for SiO_2. Dielectrics with values approximately between 10 and 30 are under consideration.

In the case of dielectric materials for interconnect applications, the requirement is the opposite. Modern ULSI devices contain 10^8–10^9 transistors in an area smaller than 1 cm^2, and operate at a clock frequency approaching several gigahertz. As device dimensions shrink, the switching speed of the transistor increases, a consequence of the decreasing carrier transit time across the smaller channel length. The transistors must be

interconnected to make the ULSI device functional. As the functional complexity of devices increase, the number of interconnection levels, and total metal interconnect length, continue to increase to the extent that an advanced ULSI device may consist of 8–10 levels of metal lines. For this reason, the effective speed of the device becomes ever more dominated by signal propagation through the horizontal and vertical metal interconnects. It is here that the resistance R and capacitance C characteristics of the interconnect materials become important. In fact, the rapid increase in RC delay time is one of the main bottlenecks for deep sub-micrometer devices. The RC delay is given by:

$$RC = 2\rho k\varepsilon_0(4L^2/P^2 + L^2/T^2)$$

where ρ is the metal resistivity, ε_0 is the vacuum permittivity, k is the relative dielectric constant of the interlayer dielectric, P is the metal line pitch (sum of line width and line spacing), T is the metal thickness, and L is the metal line length. This equation demonstrates that the RC delay can be reduced using metals with low resistivity and dielectric materials with low dielectric constant. The introduction of Cu and low dielectric constant (low-k) materials improves the situation compared with conventional Al/SiO_2 technology by reducing both the resistivity and capacitance between wires. Further reduction of the signal delay, through introduction of low-k dielectrics, is one of the main challenges today.

Therefore, the present situation is that SiO_2, having been the universal dielectric material for both gate and ILD applications for many years, must be replaced by materials with a higher dielectric constant for the gate applications and a reduced dielectric constant for interconnect applications.

These tendencies have changed the material properties of both gate and interconnect dielectrics. On the one hand, several new materials such as HfO_2, ZrO_2, and Al_2O_3 are investigated for introduction as high-k dielectrics. On the other hand, the need for dielectrics with a reduced dielectric constant requires the implementation of hydrophobic porous materials. In both cases the basic material properties are quite different compared with those of traditional dense SiO_2 and these differences create many technological challenges that are the subject of intensive research. For instance, metals forming high-k dielectric materials hardly form volatile compounds with halogens, making it extremely difficult to develop selective and damage-free dry etch processes. Diffusion of active radicals through the gate dielectric modifies the interface with silicon. Therefore, not only the development of new gate materials but also re-engineering of many technological processes is needed. In the case of low-k materials, porosity drastically increases the area of the reaction zone and the effective reactivity of these materials. Active species formed during different technological processes diffuse into the pores and create severe damage. All these problems have been stimulating the development of new technological approaches that will be discussed in the integration chapters.

This book presents an in-depth overview of novel developments made by scientific leaders in the microelectronics community. It covers a broad range of related topics, from physical principles to design, fabrication, characterization, and application of novel dielectric films. This book is intended for postgraduate level students, PhD students and industrial researchers, to enable them to gain insight into this important area of research.

The chapters included in this book can be divided into four separate sections. Chapters 1–5 are related to low-k materials developed for ILD applications. Chapters 1 and 2 focus on the deposition of low-k materials by plasma enhanced chemical vapor deposition

(PECVD) and spin-on glass (SOG) technology. Both of them are important for the preparation of different generations of low-*k* materials. Chapter 3 discusses methods developed for the evaluation of the porosity of low-*k* films. Although evaluation of porosity and pore size distribution is widely used in physical chemistry and catalysis, the introduction of low-*k* films requires the characterization of very thin films, for which most developed methods cannot be applied. Therefore, it was necessary to develop new methods applicable to thin-film analysis. Chapter 4 discusses the mechanical and transport properties of low-*k* dielectrics that presently define important integration challenges and reliability of interconnect structures. The last chapter of this section, Chapter 5, discusses the integration of low-*k* dielectric films.

Chapters 7–10 give an overview of recent developments in the field of high-*k* materials for gate applications. This section starts with a detailed discussion of the fundamentals and material science of high-*k* dielectric materials (Chapter 7), includes methods and results of physical and electrical characterization of ultra-thin high-*k* dielectrics (Chapters 8, 9), and ends with the integration of high-*k* dielectrics (Chapter 10).

Chapter 6, located between the low-*k* and high-*k* sections, is mainly oriented towards the physics and integration of materials with a 'medium dielectric constant' (ONO structures).

The last chapter of the book (Chapter 11) discusses the application of thin conductive films (ACF) for advanced microelectronic interconnects.

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Abbreviations

ACA	anisotropic conductive adhesive
ACF	anisotropic conductive film
AFM	atomic force microscopy
AL(CVD)	atomic layer chemical vapor deposition
ALD	atomic layer deposition
ARC	antireflective coating
ARXPS	angle-resolved X-ray photoelectron spectroscopy
ASIC	application-specific integrated circuit
ATC	accelerated temperature cycling
ATR	attenuated total reflection
ATR-FTIR	attenuated total reflection Fourier transform infrared spectroscopy
ATRP	atom transfer radical polymerization
BBT	band-to-band tunneling
BCB	bis-benzocylobutene
BEOL	back end of the line
BET	Brunauer–Emmet–Teller
BGA	ball grid array
BOX	bottom oxide
BTS	bias temperature stressing
bis-MPA	bis-hydroxymethyl propionic acid
BTSE	$(EtO)_3Si—(CH_2)_2—Si(OEt)_3$
BTSM	$(EtO)_3Si—CH_2—Si(OEt)_3$
CA	calixarene
C-AFM	conducting atomic force microscopy
CD	cyclodexrin
CDO	carbon-doped oxide
CEMA	channel electron multiplier array
CET	capacitive effective thickness
CHE	channel hot electrons
cmc	critical micelle concentration
CMOS	complementary metal–oxide–semiconductor
CMP	chemomechanical polishing, chemical mechanical planarization
COF	chip-on-flex
COG	chip-on-glass
CP	charge pumping
CPD	contact potential difference
CRN	continuous random network

CSP	chip scale package
CTAB	cetyltrimethylammonium bromide
CTE	coefficient of thermal expansion
CTMAC	cetyltrimethyl ammonium chloride
CVD	chemical vapor deposition
DCB	double cantilever beam
DCS	dichlorosilane
DEMS	diethoxymethylsilane
DFT	density functional theory
DI	deionized
DLC	diamond-like carbon
DMAEMA	dimethylaminoethyl methacrylate
DMDMOS	dimethyldimethoxysilane
DMOS	double-diffused MOS
DRAM	dynamic random access memory
DUV	deep ultraviolet
ECA	electrically conductive adhesive
ECMP	electrochemical mechanical polishing
ECP	electrochemical plating
EELS	electron energy loss spectroscopy
EEPROM	electrically erasable read-only memory
EFTEM	energy-filtered transmission electron microscopy
EISA	evaporation-induced self-assembly
EO	ethyleneoxy
EOT	equivalent oxide thickness
EP	ellipsometric porosimetry
ERD	elastic recoil detection
ERDA	elastic recoil detection analysis
ESL	etch stop layer
ESR	electron spin resonance
EVD	electron valence band
FCOF	flip-chip-on-flex
FD	framework density
FDLC	fluorine-containing diamond-like carbon
FE-SEM	field-emission SEM
FIB	focused ion beam
FinFET	fin field-effect transistor
F–N	Fowler–Nordheim
FRES	forward recoil elastic scattering
FSG	fluorinated silica glass
FTATR	Fourier transform attenuated total reflection
FTIR	Fourier transform infrared spectroscopy
FUSI	fully silicided
GCIB	gas cluster ion beam
GISAXS	grazing incident small-angle X-ray scattering
GOX	gate oxide
GPC	growth per cycle

GR	generation–recombination
HDP	high-density plasma
HM	hard mask
HMDS	hexamethyldisilazane
HRTEM	high-resolution transmission electron microscopy
HSQ/HSSQ	hydrogen silesquioxane
HTO	high-temperature oxide
IC	integrated circuit
ICA	isotropically conductive adhesive
ICP-OES	inductively coupled plasma optical emission spectrocopy
IL	interface layer
ILB	inner-lead bonding
ILD	interlevel dielectric
IMD	inter-metal dielctric
IPE	internal photoemission
IR	infrared
ISSG	*in situ* steam generation
ITRS	International Technology Roadmap for Semiconductors
JVD	jet vapor deposition
LCD	liquid crystal display
LEIS	low-energy ion scattering
LKE	linear kink effect
LL-D&A	layer-by-layer deposition and annealing
LOCOS	local oxidaion of silicon
low-k	low dielectric constant
LPCVD	low-pressure chemical vapor deposition
MAA	mercaptoacetic acid
MBE	molecular beam epitaxy
MEIS	medium-energy ion scattering
MEL	zeolite with a two dimensional 10-ring pore structure
m-ELT	modified edge lift-off
MFI	zeolite with a two-dimensional 10-ring pore structure and pore size 5.5.Å.
MIR-FTIR	multiple internal reflection Fourier transform infrared spectroscopy
MIM	metal–insulator–metal
MMA	methyl methacrylate
MNOS	metal–nitride–oxide–semiconductor
MOCVD	metal organic chemical vapor deposition
MONOS	metal–oxide–nitride–oxide–semiconductor
MOS	metal–oxide–semiconductor
MOSFET	metal–oxide–semiconductor field-effect transistor
MPU	multi-processor units
3MS	trimethylsilane
4MS	tetramethylsilane
MSQ	methylsilsesquioxane
MTMS	methyltrimethoxysilane
NBTI	negative-bias temperature instability
NCE	narrow channel effect

NCS	nanoclustering silica
NMOSFET	N metal–oxide semiconductor field-effect transistor
NRA	nuclear reactive analyses
NROM	nitride read-only memory
NVSM	nonvolatile semiconductor memory
ODT	octadecanethiol
OF	organic-functionalized
OLB	outer-lead bonding
OMCTS	octomethylcyclotetrasiloxane
ONO	oxide–nitride–oxide
OSG	organosilicate glass
OTP	one-time programing
P2VP	poly (2-vinylpyridine)
PAE	poly-arylene ethers
PALS	positron annihilation lifetime spectroscopy
PAS	positron annihilation spectroscopy
PCBO	post-CMP burn-out
PCL	polycaprolactam
PDA	post-deposition annealing, personal digital assistant
PEBO	post-etch burn-out
PECVD	plasma-enhanced chemical vapor deposition
PEG	propylene glycol
PEO	propyleneoxy
P–F	Poole–Frenkel
PHS	poydisperse hard sphere
PMO	periodic mesoporous organosilica
PMOS	*p*-channel metal oxide semiconductor
PMS	periodic mesoporous silica
POSS	polyhedral oligomeic silesquioxane
PPG	polypropylene glycol
PRD	pore radius distribution
Ps	positronium
PSD	pore size distribution
pSiCOH	porous SiCOH
PSZ	pure silica zeolite
PTFE	polytetrafluoroethylene
PTH	pin-through hole
PVD	physical vapor deposition
RBM	random bonding model
RBS	Rutherford backscattering
RCP	random close-packed
RF	radiofrequency
RHEED	reflection high-energy diffraction
RMM	random mixture model
ROP	ring-opening polymerization
RPC	reactive pre-clean
RPN	remote plasma nitridation

RTA	rapid thermal annealing
RTS	random telegraph signals
SAB	self-aligned barrier
SAM	self-assembled monolayer
SANS	small-angle neutron scattering
SAWS	surface acoustic wave spectroscopy
SAXS	small-angle X-ray scattering
SBD	soft breakdown
SCCO2	supercritical CO_2
SCE	short channel effect
SE	spectroscopic ellipsometry
SEM	scanning electron microscopy
SiDLC	silicon-containing diamond-like carbon
SILC	stress-induced leakage current
SiLK	silicon application low-*k*
SIMS	secondary ion mass spectroscopy
SiOC	carbon-doped silicate
SiOF	fluorinated silica
SMF	surface mount technology
SOG	spin-on glass
SOI	silicon-on-insulator
SONOS	silicon–oxide–nitride–oxide–silicon
SRH	Shockley–Read–Hall
SSQ	silesquioxane
TAB	tape-automated bonding
TAT	thermally assisted tunneling
TCP	tape carrier packaging
TDDB	time-dependent dielectric breakdown
TDGCMS	thermal desorption gas chromaograph mass specrometry
TEFS	triethoxyfluorosilane
TEM	transmission electron microscopy
TEOS	tetraethoxysilane
TF	trench first
TGA	thermogravimetric analysis
TMCS	trimethylchlorosilane
TMCTS	tetramethylcyclotetrasiloxane
TMOS	tetramethoxysilane
TOF-SIMS	time-of flight secondary ions mass spectroscopy
TOX	top oxide
TSEE	thermally stimulated exoelectron emission
TUNA	tunneling atomic force microscopy
TXRF	total reflection X-ray fluorescence
ULK	ultralow-*k*
ULSI	ultra-large-scale integration
UV	ultraviolet
VF	via first
VLSI	very large-scale integration

VUV	vacuum ultraviolet
WCN	tungsten carbon-nitride
WLACF	wafer-level anisotropic conductive film
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XRF	X-ray fluorescence
XRP	X-ray porosimetry
XR, XRR	X-ray reflectivity
YSZ	yttria-stabilized zirconia

1 Low and Ultralow Dielectric Constant Films Prepared by Plasma-enhanced Chemical Vapor Deposition

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1.1 INTRODUCTION

The semiconductor industry has been improving the performance of ultra-large-scale integrated (ULSI) circuits by shrinking the transistor size according to Moore's Law, which states that the chip performance will double about every 18 months. The shrinking of the devices has resulted in increased device speed and device density. The speed of an electrical signal in an ULSI circuit is controlled by the switching time of the individual transistors

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and by the signal propagation time through the interconnect system. The function of an interconnect or wiring system (also often referred to as the back end of the line, or BEOL) is to distribute the signals between the active devices and to provide power to and among the various circuit functions on a chip.

The signal delay of the BEOL is defined by its *RC*, *R* being the wire resistance and *C* the intralevel and interlevel dielectric capacitance. At a certain metallization level this is roughly dependent on

$$RC = 2\rho k(4L^2/P^2 + L^2/T^2)$$

where *L* is the line length, *P* the metal pitch, T the metal line thickness, ρ the metal resistivity and *k* the dielectric constant of the insulator between the lines. Reducing the capacitance of the interconnect by replacing the dielectric with a material of lower *k* also reduces the power consumption of the circuit which is given by:

$$\text{Power} = CV^2f$$

where *C* is the capacitance of the circuit, and *V* and *f* are the operating voltage and frequency.

Each shrinking of the ULSI chips, which reduced the dimensions of the electrical devices, resulted in a reduced switching time of the transistors, but also caused a corresponding reduction in *P* and *T*, thus increased *RC* delays of the electrical signals. Thus, while the signal propagation time was much smaller than the switching time for many device generations, at a certain technology generation, the signal propagation though the interconnect structure became slower than the switching time of the active devices and it became necessary to reduce the RC delay of the BEOL for maintaining the high performance of the ULSI semiconductor chips.

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) was the first to point out the need for new conductor and dielectric materials in order to meet the projected overall technology requirements.

A significant improvement in the performance of the BEOL was achieved by replacing the Al interconnects with Cu, which has ~30% lower resistivity than that of Al. The use of Cu as the BEOL metal was first demonstrated by IBM and Motorola [1, 2] by 1998, and has been generally adopted afterwards by the entire semiconductor industry. The Cu metallization was introduced while still using silicon dioxide with a dielectric constant *k* of about 4 as the insulator dielectric. Further reduction of the signal delay in the BEOL required the replacement of the insulator with materials having lower dielectric constants.

Fluorinated silicon glass (FSG, or SiOF) was the first dielectric with reduced dielectric constant ($k = 3.7$) to replace silicon oxide as the BEOL dielectric with Cu metallization at the 180 nm technology node [3].

However, the continuation of the decreasing of the dielectric constant of the insulator as predicted by the International Technology Roadmap for Semiconductors (ITRS) has been problematic. The reliability and yield issues associated with the integration of new dielectric materials with dual damascene copper processing proved to be much more challenging than initially predicted. According to ITRS, 1997 edition [4] it was expected that insulating materials with $k = 2.5$–3.0 will be introduced already at the 180 nm node in 1999. This prediction then shifted to the introduction of such materials at the 130 nm, to be finally

introduced only at the 90 nm node. Only the 2004 update of ITRS did not change the roadmap's low-*k* portion, for the first time in 10 years [5].

A large number of potential materials with low dielectric constants have been investigated over the years and details about these materials and their methods of fabrication and integration can be found in proceedings of MRS symposia [6] or ECS symposia [7] on low-*k* materials. In spite of the very large effort invested over many years by the semiconductor industry to replace the SiO_2 and SiOF dielectrics with materials having significantly lower dielectric constants, with about 150 different dielectric materials being identified by SEMATECH in the mid-1990s [8], the practical progress in implementation of new dielectrics has been delayed by 2001 up to four years relative to initial SIA roadmap projections. The delay was marked by continuous revisions outwards in time of SIA projections since 1997 [9].

The delay in the implementation of low-*k* dielectrics in ULSI interconnect structures was caused by their inability to satisfy the requirements of integration processing, as discussed later and by their mechanical weakness compared with SiO_2 and SiOF.

Most of the initial candidate low-*k* materials, organic polymers or hybrid, organosilicate glasses, were prepared by spin-on techniques. The dielectrics that will be discussed in this chapter are prepared by PECVD, although they are often *mistakenly* referred to as CVD films. In CVD, or chemical vapor deposition, the deposition of the film and its properties are controlled by the temperature of the substrate and the deposition process takes place under thermodynamic equilibrium and the film has a well-defined structure and is usually crystalline (single crystal or polycrystalline).

In contrast to CVD, the PECVD (plasma enhanced CVD) method [10] is a nonequilibrium technique, where the process is controlled mainly by the energy of the electrons in the plasma. The energy of the electrons in a plasma is defined by an average energy but is has a Druyvesteyn-type distribution with a tail extending to energies much larger than the average one [10]. As a result, the plasma dissociates the molecules in the gas phase into a variety of radicals, which recombine on the substrate to form a solid film comprising a variety of different bonds. The films deposited by PECVD are usually amorphous materials. The substrate temperature may affect the properties of the deposited film, but it is typically lower than the one required to deposit a film from the gas phase by thermal CVD.

1.2 PROPERTY REQUIREMENTS FOR INTEGRATION

As mentioned in the previous section, a large number of materials with low *k* values have been identified over the years. However the implementation of such materials in a BEOL interconnect structure proved to be a very difficult task. In order to introduce a new dielectric as the insulator of the BEOL, the material has to satisfy a large number of criteria imposed by its functionality in the structure and by the integration processing. Some of these criteria are listed next [3, 11, 12]:

1. Electrical—to make it useful as a low-*k* insulator
   - low dielectric constant
   - low dissipation factor
   - low leakage currents at operating fields
   - high breakdown voltage

2. Thermal—to enable it withstand other integration processes
   - stability at temperatures greater than or equal to 400°C
3. Mechanical—to enable the fabrication of mechanically robust devices
   - maximal elastic (Young's) modulus and hardness (to withstand harsh integration processes, such as chemomechanical polishing (CMP), or assembly/packaging)
   - low stresses (to prevent cracking or delamination from other layers in the BEOL structure),
4. Environmental stability
   - low moisture absorption
   - maintain electrical and mechanical properties under exposure to environment
5. Adhesion to and compatibility with other dielectrics (hardmask, caps, etch stops) or conductors (metal or nitride liners) in contact with it
6. Low/no oxygen and moisture diffusion through film
   - prevent oxidation of the metallization materials, especially Cu
7. Solvent resistance—to maintain its properties after exposure to wet cleans during the integration processing
8. Patternability, etching at required dimensions
   - high etch selectivity during RIE processing
9. Chemomechanical polishing (CMP) capability and compatibility
   - maintain properties after exposure to CMP slurries
10. Avoid resist poisoning
11. No/minimal damage to dielectric by the integration processes
12. Commercial availability of precursors with reasonable shelf life
13. Low cost of fabricated film
14. Environmental compliance of precursors and processing by-products.

The requirements listed above were fulfilled by the classic dielectric SiO_2, however most materials with lower k considered for replacing the oxide did fail many of these criteria and were removed from considerations. Even the low-k dielectrics that have finally been integrated in ULSI chips may not fulfill all the requirements listed above and the integration processes had to be modified to accommodate for the lack of those.

1.3 CHARACTERIZATION

This section presents the characterization techniques used for the determination of the material properties of low-k dielectrics, for evaluating their potential suitability as the dielectric of the interconnect of a ULSI. These characterizations will only evaluate the potential of a candidate material, the final suitability being established by the integration process, which is beyond the scope of this chapter.

The rest of the chapter will be separated between the discussion of organic, diamond-like carbon (DLC)-based films and the discussion of the hybrid SiCOH films. As the same characterization techniques are common for all types of dielectrics, these techniques will be discussed briefly here. Some characterization techniques will be discussed in detail in the following chapters of this book.

The low-k films were characterized as deposited and after thermal anneals. These anneals were performed for 4 h in an inert ambient either at 400 or 430°C.

The composition of the dielectric films was determined by Rutherford backscattering (RBS) in combination with forward recoil elastic scattering (FRES), the latter being used for the determination of the hydrogen content. Both RBS and FRES data were analyzed in our studies with a RUMP program [13], which was used to simultaneously fit theoretical film compositions to both RBS and FRES experimental spectra in the same time.

Optical properties of the dielectric films were determined by ellipsometry, Fourier transform infrared spectroscopy (FTIR) and $n\&k$ measurements [14]. The FTIR spectra were collected using the same substrate, from which the film was removed, as the background. In most of the cases the collected spectra were baseline corrected. FTIR absorption peaks enable the identification of the different bond structures in the films. In some cases, peaks were deconvoluted into individual components to get a better understanding of the film structure [15]. FTIR analysis can also be used to follow modifications in the films as a result of processing of the dielectric or its exposure to the environment, but only if such changes are larger than a few percent.

The index of refraction n is often used to characterize dielectric films due to its relation to the dielectric constant ($n^2 \leqslant k$, the $<$ sign stemming from the fact the n and k are usually measured at very different frequencies). The index of refraction can be determined by ellipsometry if the thickness of the film is known. The $n\&k$ tool enables simultaneous measurement of both film thickness and n values over a wavelength range of 193–800 nm.

The dielectric constants were measured at 1 MHz, on metal–insulator–metal (MIS) structures using highly doped Si wafer substrates with mΩ resistivities. The low-k films were deposited as blanket layers and the Al or Cu dots were deposited as metal contacts to the film. The backside of the Si wafer was coated with an Al film for improved electrical contact. Details of the electrical characterization techniques can be found elsewhere [16, 17]. The same structures were used to determine the leakage currents through the films by measuring the I–V characteristics through contact dots of known area.

The stresses in the films have been determined from the radius of curvature induced on the substrate by the deposited film using the equation

$$\sigma = \frac{Eh^2}{(1-\nu)6Rt}$$

where σ is the stress, $E/(1\text{-}\nu)$ is the biaxial elastic modulus of the substrate (180 GPa for (100) Si wafers), h is the substrate thickness, t is the film thickness, and R is the radius of curvature.

The elastic modulus E and hardness H of the films were measured by nanoindentation. The measurements were done on 1 μm and >3 μm-thick films. Despite the general belief that 1 μm films are sufficient for this characterization, it was found that at this thickness

the substrate effect was still significant. That effect was eliminated by measuring films at least 3 μm thick [18]. The cracking propensity of the films and the critical thickness for crack development were determined by a technique described elsewhere [19].

Thickness changes resulting from different processes undergone by the dielectric films were determined by measuring the height of steps etched in the films using profilometric techniques, or by comparing the thicknesses determined by *n*&*k* measurements before and after a certain process. Thickness changes have sometimes also been evaluated from changes in the FTIR peak intensity of the CH_i absorption band of DLC films (centered at 2920 cm^{-1} [17]) or the CF_j absorption band of fluorinated DLC (FDLC) films (centered at about 1200 cm^{-1} [20]). This technique is estimating material loss from the film rather than shrinkage.

The porosity of porous low-*k* and ultralow-*k* films was characterized by several methods: ellipsometric porosimetry (EP), positron annihilation spectroscopy (PAS) and positron annihilation lifetime spectroscopy (PALS), small-angle X-ray scattering (SAXS), and specular X-ray reflectivity. The techniques enable the determination of the degree of porosity in the films and the pore size distribution (PSD). A description of the different techniques with further references to the details of the used methods can be found in references [21–23]. A detailed description is provided in Chapter 3 of this book.

1.4 ORGANIC PECVD DIELECTRICS: DIAMOND-LIKE CARBON AND FLUORINATED DIAMOND-LIKE CARBON

Diamond-like carbon (DLC) and its modifications were the first low-*k* dielectrics prepared by PECVD. DLC is an amorphous hydrogenated carbon that can be easily modified to incorporate additional elements in its amorphous structure. Among such elements, F, Si, or metals have been incorporated in DLC to modify its tribological behavior [17, 24]. For its potential use as a low-*k* dielectric, F-containing (fluorinated DLC, or FDLC) and Si-containing DLC (SiDLC) have been considered. The preparation of the different types of films will be described next.

1.4.1 Preparation

Low-*k* DLC films have been prepared by RF PECVD in a parallel plate reactor, at pressures of 100–300 mTorr and RF powers of 25–100 W, corresponding to power densities of 0.08–0.31 W/cm^2, as described in detail elsewhere [25, 26]. The RF plasma was sustained with a RF power supply at a frequency of 13.56 MHz. The growth rate and properties of DLC films are controlled by the substrate bias during deposition [17]; therefore the deposition was performed on substrates placed on the powered electrode, thus being at a negative self-bias. For the range of used plasma conditions, the substrate bias was in the range −80 to −300 V DC.

The deposition of DLC was performed at substrate temperatures below 250°C, because deposition at higher temperatures causes the formation of films with more graphite-like than diamond-like characteristics [17] and such films are characterized by high current leakage and high *k* values. The precursor for the deposition of DLC films can be any pure hydrocarbon, such as methane, acetylene, cyclohexane.

FDLC films, generally characterized by lower dielectric constants then DLC, have been deposited from fluorocarbons, mixtures of fluorocarbons with hydrogen, or mixtures of fluorocarbons with hydrocarbons, using parallel plate RF PECVD reactors [26, 27] or high-density plasma reactors [28, 29]. Contrary to DLC, low-*k* FDLC films can be deposited at temperatures up to 400°C and on either electrode of the parallel plate reactor.

1.4.2 Properties of DLC-type low-*k* dielectrics

DLC

DLC and FDLC have been considered as potential low-*k* dielectrics as early as 1995, but the first reported films were either not stable above 300°C [30, 31], or had dielectric constants of about 6 [32]. In 1997 we reported for the first time low-*k* DLC films stable up to 400°C [25] and FDLC films with $k = 2.3$ have been reported elsewhere [27].

The low-*k* DLC films contained 40–46% hydrogen, the amount of hydrogen decreasing with increasing RF power and decreasing pressure during deposition [25]. The dielectric constant of DLC displayed an opposite behavior, decreasing with decreasing RF power and increasing pressures as illustrated in Figure 1.1. The dielectric constant could be lowered, within the range of investigated deposition parameters, from 3.9 to values as low as 2.7. The same data from Figure 1.1 is presented as a function of the substrate bias during deposition in Figure 1.2 [33], where it can be seen that the dielectric constant of DLC films prepared from one precursor is essentially controlled by the substrate bias and decreases with decreasing bias.

DLC films, generally developed for tribological applications, are usually characterized by high internal compressive stresses [17]. The stress of DLC films deposited for low-*k* applications was found to be essentially controlled by the substrate bias during film deposition, similar to the dielectric constant [33]. The compressive stress in the as-deposited films

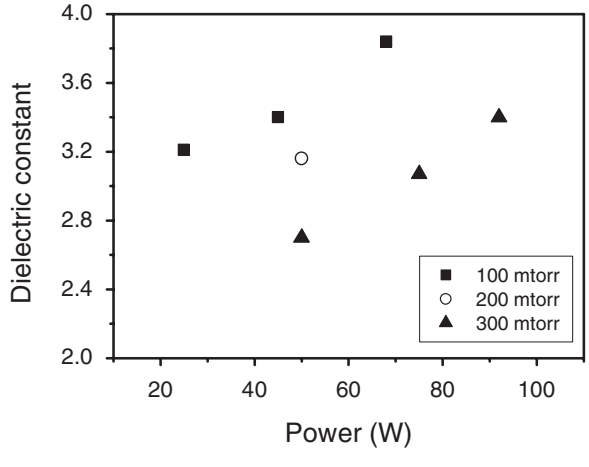

Figure 1.1 Dielectric constant of as-deposited DLC as a function of RF power at different deposition pressures (Reprinted with permission from [25] Copyright 1997 Materials Research Society)

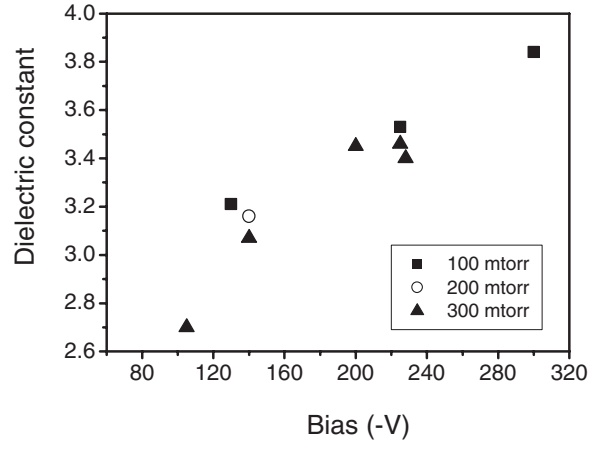

Figure 1.2 Dielectric constants of DLC vs substrate bias during deposition (Reprinted from [33] with permission from Elsevier)

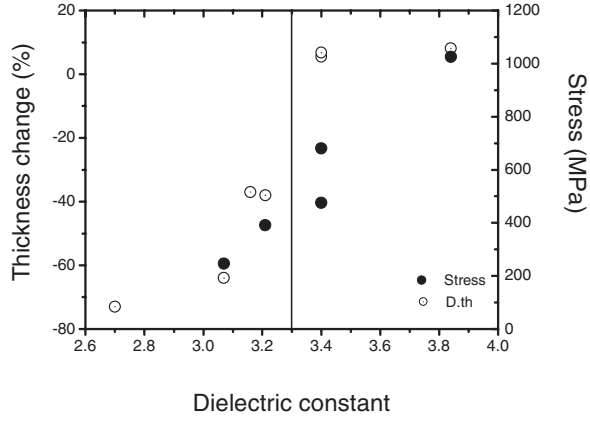

Figure 1.3 Thickness change after annealing and stress in as-deposited DLC vs dielectric constant of as deposited film (Reprinted with permission from [26] Copyright 1997 Materials Research Society)

could be reduced from about 800 MPa to about 200 MPa by decreasing the RF power and increasing the deposition pressure, or decreasing the bias. Thus, the DLC films having lower k values are also characterized by lower intrinsic stresses. This appeared to be a beneficial trend, as high intrinsic stress can be detrimental to the manufacturing process if such films could be used as the BEOL dielectric in ULSI circuits. High film stresses can cause wafer bowing and interfere with the patterning process, as well as causing stress-related adhesion failure. However, we shall see in the following that the as-deposited, low-k, low-stress films were not stable at 400°C.

Figure 1.3 [26] presents the thickness changes caused by the annealing at 400°C for 4 h in an inert ambient and the stresses in the as-deposited DLC films as a function of the dielec-

tric constant of the as-deposited films. It can be seen that films having a dielectric constant higher than about 3.3 have high intrinsic stresses and are characterized by a small increase in film thickness after annealing. In contrast, films having lower dielectric constants have smaller intrinsic stresses, but lose a high fraction of their thickness during annealing. The similar dependence of dielectric constant, hydrogen content, stress, and thermal stability of DLC films on the deposition conditions may be explained by the effect of the deposition conditions on the film structure. DLC films are amorphous cross-linked structures, whose degree of cross-linking and carbon hybridization, sp^2, sp^3, depends on the ion bombardment of the growing films [17]. Higher powers and/or lower pressures in the plasma (lower substrate bias) result in incorporation of smaller amounts of hydrogen and stronger cross-linking in the films, producing films of higher thermal stability characterized by higher dielectric constants and higher stresses.

It is apparent from the discussion above that it might be possible to deposit DLC films with sufficient thermal stability at 400°C, however the required deposition conditions produce films with dielectric constants higher then 3.3. As-deposited DLC films of lower dielectric constants and lower stresses are not stable at this thermal exposure [26]. Nevertheless, it has been found that DLC films having dielectric constants as low as 2.7 can be stabilized by annealing them first in a nonoxidizing ambience at the highest temperature dictated by the integration processes [12, 33]. Subsequent anneals at the same temperature did not modify the films any more. Furthermore, the stresses in the DLC films decreased after annealing from the as-deposited compressive stress of about 500 MPa and, for films with $k = 2.7$, the stress became slightly tensile.

Figure 1.4 [12] shows the leakage current through a DLC film having a dielectric constant $k = 2.8$ after deposition of Cu dots on the stabilized film and after annealing the Si/DLC/Cu structure at 400°C for 4 h in He. The leakage current is relatively high at 10^{-7} A/cm^2 at a field of 0.5 MV/cm, but it has been deemed to be sufficiently low to make the material usable as the interconnect dielectric. An average acceptable leakage of only 3×10^{-10} A was

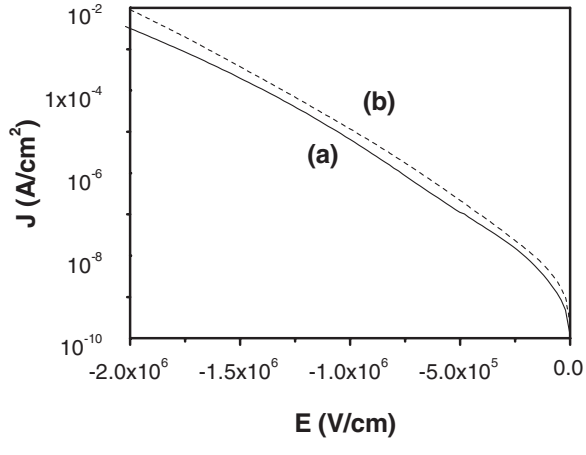

Figure 1.4 Leakage current in stabilized DLC: (a) stabilized film; (b) after annealing the MIS structure for 4 hours at 400°C in He (Reproduced from [12] with permission from The Electrochemical Society, Inc.)

measured at 1.8 V in an integrated a Cu serpentine 3.8 m long, separated from an adjacent comb structure by 0.34 μm of DLC [34]. The repeated annealing at 400°C of the stabilized films induced only a small increase in the leakage current trough the DLC film.

FDLC

Claims have been made that FDLC films can be prepared to be stable at 400°C [11, 27, 35]. Such FDLC films were also characterized by low internal compressive stresses of about 150 MPa in as-deposited conditions and decreased further after annealing [11].

FDLC films deposited from the pure fluorocarbon precursor (hexafluorobenzene) had fluorine concentrations up to 42%, which where almost constant for a large range of deposition conditions [11]. The fluorine is mostly bound in CF_2 and CF_3 bonds in such films [20]. Such fluorine concentration in the films was considered to be too high, raising concerns about possible reactions of F with the materials in contact with the FDLC layers in the BEOL interconnect structure. Hydrogen dilution of the precursor in the plasma was used to reduce the F content and, for a range of investigated mixtures, the fluorine concentration in the films could be decreased to 20% with a concomitant increase of the hydrogen concentration up to 12% [11].

The dielectric constants of as-deposited FDLC films are presented in Figure 1.5 [25] as a function of hydrogen dilution of the fluorocarbon precursor, at different RF powers supplied to the plasma. As can be seen, FDLC films deposited from pure fluorocarbon have dielectric constants as low as 2.55. Dilution of the fluorocarbon precursor with hydrogen increased the dielectric constant of the films, due to the replacement of fluorine with hydrogen in the films. The deposition power had a similar effect on the dielectric constant, which increased with increasing deposition power. Dielectric constants as low as 2.3 have been reported by other groups [27, 28].

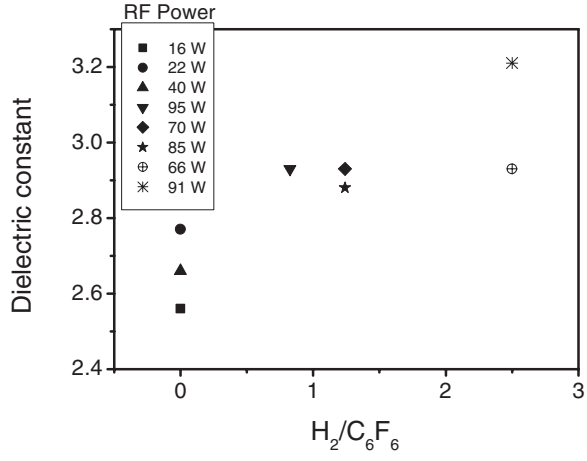

Figure 1.5 Dielectric constant of as-deposited FDLC films as a function of the precursor dilution with hydrogen (Reprinted with permission from [25] Copyright 1997 Materials Research Society)

The thermal stability of the FDLC films was initially investigated by measuring changes of film thickness after annealing at 400°C for 4 h in nitrogen. However, it was found that films having negligible thickness changes can have significant material loss during annealing [11, 26]. The characterization of the thermal stability was therefore supplemented with measurements of material loss by RBS [11, 26]. The edge of the Si background in the RBS spectra is shifted to lower energies by an amount determined by the density of atoms (in at./cm^2) on top of the Si substrate. The shift of the Si edge towards higher energies (channels) after annealing is an indication of mass loss from the films. As illustrated in Figure 1.6 [11], such a shift was observed after the first anneal, but not any more after a second anneal, indicating the stabilization of the film (no more loss of mass).

The properties of the FDLC films and growth rate could be improved by adding argon to the precursor mixture used for the deposition of the films without affecting the fluorine concentration in the films [11]. For example, addition of Ar to the gas feed reduced the weight loss after first anneal to about 7% from 20% in the films deposited without Ar [11]. The results indicated that FDLC films deposited from fluorocarbon diluted with hydrogen and argon at sufficient plasma power could be stabilized by a first anneal at 400°C and remain apparently stable to subsequent exposure to the same temperature. As we shall see later, this proved not to be true. The apparently stabilized FDLC films had dielectric constant in the range of 2.4–2.6 and appeared to be promising candidates for the low-k dielectric of the interconnect structure [11, 25].

Figure 1.7 [12] shows the leakage current trough a FDLC film after the deposition of Cu dots and after annealing the entire structure at 400°C for 4 h in nitrogen. It can be seen that the leakage current of 2×10^{-8} A/cm^2 at an operating field of 0.5 MV/cm through the FDLC film was lower than that of DLC (see Figure 1.4) and appeared to be sufficiently low to

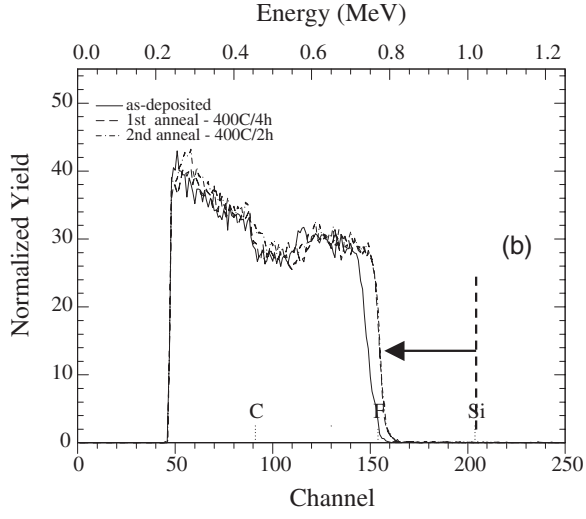

Figure 1.6 RBS spectra of as-deposited and annealed FDLC films. The arrow indicates the shift of the Si edge due to the overlaying film (Reproduced from [11] with permission from The Electrochemical Society, Inc.)

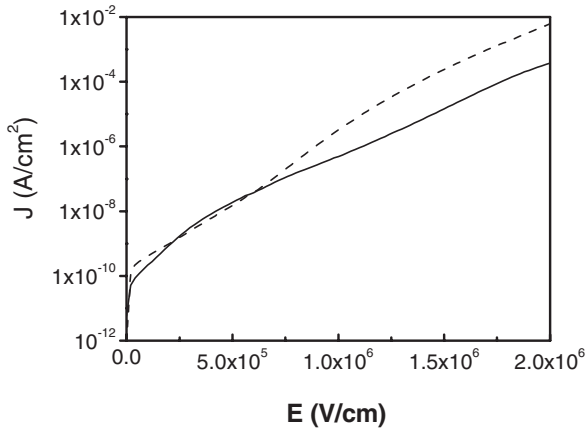

Figure 1.7 Leakage current in FDLC vs electric field. Solid line—after deposition of Cu dots; dashed line—after annealing the structure at 400°C/4 h/N_2 (Reproduced from [12] with permission from The Electrochemical Society, Inc.)

enable the potential use of this material as the interconnect dielectric. Annealing of the FDLC/Cu structure did not induce any significant changes in the leakage current.

1.4.3 Processing of DLC-type low-*k* dielectrics

DLC

DLC and FDLC films can be dry patterned by reactive ion etching (RIE) using an O_2-based plasma and a hard mask, such as SiN or SiO_2. Patterning of DLC films has been demonstrated in parallel plate RF plasma and in high-density plasma (HDP) etch chamber operated at lower pressures than the PECVD plasma [12].

A dual damascene etching process using a dual hardmask [36] has been developed to etch directly the dual damascene structure, without the need of an additional etch stop layer between the trench (line, wire) and via levels. The use of the dual hard mask process avoided potential problems during the patterning of DLC such as scumming of the resist or interaction of the resist with the organic low-*k* material and enabled a rework, if necessary, to be done at the second lithography step [12]. Patterning of DLC by this process is illustrated in Figure 1.8 [12].

The integration of low-*k* dielectric in a damascene process involves the steps of metal removal from the top of the dielectric by CMP. The stabilized low-*k* DLC films are characterized by nanohardness values H in the range 1.3–3 GPa, and Young's modulus E in the range 12–27 GPa, compared with $H < 0.5$ GPa and $E < 5$ GPa for most polymeric dielectrics [37]. The mechanical and chemical properties of DLC enabled efficient removal of the metallization and good planarization of the damascene structures by CMP [34].

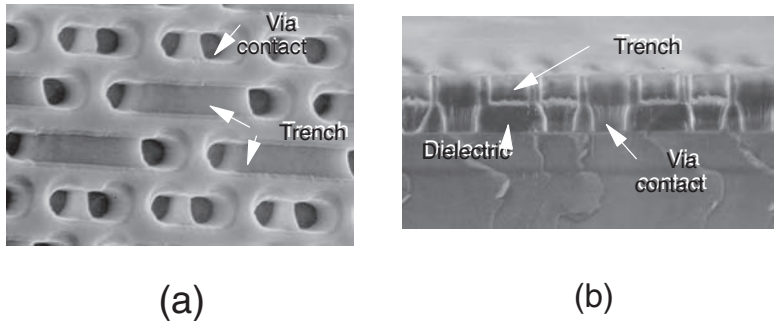

Figure 1.8 SEM micrograph of dual damascene pattern produced in DLC with a dual hardmask RIE technique: (a) top view; (b) cross-section through via and trench (Reproduced from [12] with permission from The Electrochemical Society, Inc.)

FDLC

The integration of the FDLC films in a BEOL interconnect structure requires good adhesion of FDLC to other dielectrics, such as silicon oxide, silicon nitride, and to metals, such as Ta. FDLC films, 700 nm thick, have been deposited on SiN, SiO_2, or Ta films, deposited on Si substrates. The Si/X/FDLC (X = SiN, SiO_2, Ta) structures showed good adhesion of FDLC to these films, both as-deposited and after annealing at 400°C, and indicated an apparent stability of FDLC at 400°C [12].

Inverted (Si/FDLC/X) layered structures have then been investigated: SiN, SiO_2 and Ta, each 50 nm thick, have been deposited on stabilized FDLC films deposited on Si substrates. The as-deposited films had good adhesion to FDLC. However, after annealing these structures at 400°C, they either delaminated by themselves or could be easily removed by a Scotch tape test. Investigation of the delaminations showed that the separations occurred either at the FDLC/X or Si/FDLC interfaces. XPS characterization of the delamination interface showed the formation of SiF bonds on the delaminated surface of the SiN and SiO_2 films and TaF_5 bonds on the surface of the Ta films [12]. Thus, in spite the fact that the FDLC films appeared thermally stable according to the stability evaluation based on mass loss and thickness changes, at 400°C the films interacted with layers deposited on top of the FDLC and weakened the interfaces between the layers.

The results described above indicated that the 'stabilized' FDLC still contained F atoms that were mobile in the structure at 400°C. Any residual fluorine that was released from the FDLC films in the Si/X/FDLC structures during the subsequent exposure at the high temperature was apparently able to escape from the FDLC film without causing significant damage to the bottom X/FDLC interface. However, the films deposited on top of FDLC in the Si/FDLC/X structures apparently prevented the escape of the fluorine released from FDLC. This could cause fluorine accumulation at the FDLC/X interface until it reached concentrations sufficiently high to weaken the FDLC/X interface by reaction with the top X layer [12].

1.4.4 Integration of DLC-type low-*k* dielectrics

DLC

The first stage of integration of DLC low-*k* dielectric with copper metallization is illustrated in Figure 1.9 for a first metallization M1 interconnect level [12]. The figure shows the cross-section of the Cu wires embedded in a first level DLC dielectric coated with a yet unpatterned V1 level DLC layer on top of it. The illustrated structure incorporates a SiN diffusion cap layer on top of the DLC level. The micrograph illustrates the integrity of the structure.

A further step of integration of DLC with copper metallization is illustrated in Figure 1.10 [33]. The figure shows the cross-section of two levels of Cu wires embedded in three levels of DLC dielectric. The M2 Cu wires have an imperfect shape because the etching process of

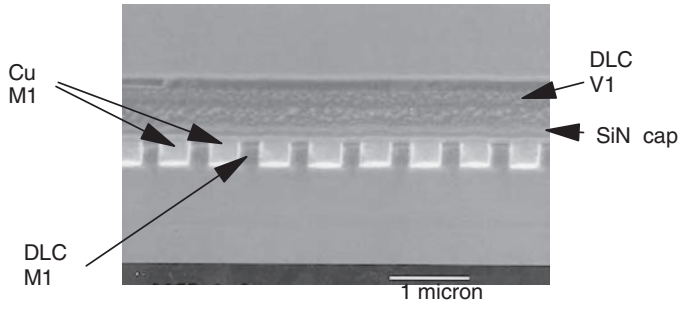

Figure 1.9 SEM micrograph of a cross-section of a M1 Cu/DLC integrated structure (Reproduced from [12] with permission from The Electrochemical Society, Inc.)

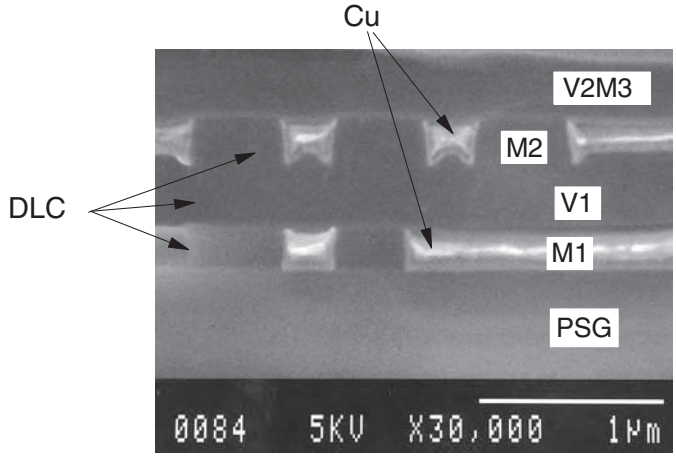

Figure 1.10 SEM micrograph of a two-level Cu/DLC integrated structure (Reprinted from [33] with permission from Elsevier)

the DLC was not yet optimized for the patterned structure on 8-inch wafers. Nevertheless, the micrograph illustrates the integrity of the structure up to the third DLC level V2M3. Initial electrical evaluation of 8-inch wafers have shown significant yields for both opens and shorts measurements. These results indicated the potential of DLC as a candidate for use as a low-k interconnect dielectric with Cu metallization in the BEOL of ULSI chips.

FDLC

It was shown above that the FDLC films were not stable enough to prevent release of fluorine and its interactions with other layers in contact with it during exposure at 400°C. While other authors claimed to have fabricated FDLC films thermally stable at 400°C [11, 27, 35], the stability of these materials has not been proven by integration with other films at this temperature. Initial integration of FDLC with Al in a gap fill process [28] and with Cu in a damascene process [29] has been demonstrated only to temperatures below 350°C.

1.4.5 Summary

The results discussed above showed that it is possible to prepare by PECVD hydrogenated (DLC) and fluorinated (FDLC) amorphous carbon films with dielectric constants as low as 2.7 for DLC and 2.3 for FDLC. DLC films with low k values could be stabilized by annealing them at 400°C.

The stabilization of FDLC by such an anneal proved to be only apparent. The annealed films seem to contain sufficient mobile fluorine that can interact with the adjacent layers at 400°C and weaken the interfaces. As a result FDLC did not seem to be a good candidate for use as the interconnect low-k dielectric.

Stabilized DLC films, with dielectric constants $k < 3.0$, have shown the potential of integration as the interconnect dielectric in ULSI chips. By the time that the first integration steps were demonstrated in Cu/DLC structures it was found that low-k hybrid films of DLC-SiO_2 (amorphous a-C:H-SiO), later to be called SiCOH, can be prepared by PECVD. The SiCOH films had better properties than DLC, did not require any stabilization after the deposition step and the BEOL technology based on PECVD dielectrics shifted its entire effort to the new SiCOH materials to be discussed in the next section.

1.5 SiCOH FILMS AS LOW-k AND ULTRALOW-k DIELECTRICS

Among the early low-k candidates for BEOL dielectrics were spin-on glasses (SOG) containing Si, C, O, H, and having dielectric constants below 3, such as methylsilsesquioxanes (MSQ) [38]. The organosilicon polymers were expected to preserve some characteristics of the silicon dioxide that would facilitate their integration in the interconnect structure. MSQ films are deposited by spin-on techniques from precursor molecules that have nanoporous geometry and the polymerization processes preserves a part of the precursor's structure in the films [39]. However, contrary to expectations, the integration of the spin-on films with $k < 3$ proved to be difficult, mainly due to their poor mechanical properties and the tendency of the films to crack.

Films deposited by PECVD usually have enhanced three-dimensional cross-linking compared with spin-on polymeric films of similar compositions and were expected to be therefore mechanically tougher. Furthermore, the integration process of PECVD films was expected to be more evolutionary from the prevailing technology relative to spin-on films. PECVD films comprised mainly of Si, C, O and H with $k < 3.0$ have indeed been developed and reported already in 1999 [40], but have been only recently successfully integrated in microprocessor products now available on the market.

These PECVD materials, characterized by dielectric constant values in the range of 2.8–3.0, are also known by names such as SiOC, carbon-doped oxides (CDO), silicon oxycarbides, organosilicate glasses (OSG) and several trade names given by the various suppliers who provide processes and tooling for these films. Such materials will be referred to in the followings as SiCOH. (The SiCOH notation describes the atoms composing the films but not the film stoichiometry.) Different groups have investigated the properties of such films and associated deposition process dependencies [41–45]. We have demonstrated that it is possible to extend this family of dielectrics to k values as low as 2.0 [46–48], thereby providing a path for the extendibility of using these films in interconnects of future generations of the Si technology.

1.5.1 Preparation

Dense SiCOH

The films described in this section are sometimes referred to as 'dense' SiCOH, indicating that no intentional porosity was induced in them with the use of a porogen. Nevertheless, such films may have some degree of porosity.

PECVD SiCOH films can be prepared from a variety of precursors or precursor mixtures that comprise all the components of the films. The initial depositions were intended to prepare films having a cage-type SiO structure similar to that of MSQ [39] and it was assumed that a ring-type cyclic siloxane precursor will be most suitable for that purpose [40]. It was expected that, by adjusting the plasma conditions for minimal dissociation of the molecules, the ring structure of the molecule could be preserved in the film, inducing molecular nanoporosity, thereby creating a material with reduced density and corresponding lower dielectric constant. The first films were prepared accordingly using tetramethylcyclotetrasiloxane (TMCTS, or $Si_4O_4C_4H_{16}$), which contains all the components of the resultant film [40]. A diagram of this molecule is shown in Figure 1.11. This cyclic molecule provides the oxygen necessary for the final SiCOH film and does not necessarily require an additional oxidizer gas in the process. Helium was added to TMCTS as a carrier gas or added to the plasma. Helium was chosen as the dilutant gas for minimizing the potential effects of the ion bombardment on the growing films. Another cyclic precursor currently used for the deposition of SiCOH films is octomethylcyclotetrasiloxane (OMCTS, or $Si_4O_4C8H_{24}$), shown in Figure 1.11.

Similar SiCOH films with low k values have also been prepared from noncyclic precursors such as methylsilanes (trimethylsilane, or 3MS being the preferred one), diethoxymethylsilane (DEMS), or dimethyldiethoxysilane (DMDMOS) (see Figure 1.11). Other precursors have also been investigated [44, 45, 49, 50]. When using methylsilanes as the SiCOH precursors an oxidant has to be added to the gas mixture. The initial depositions were

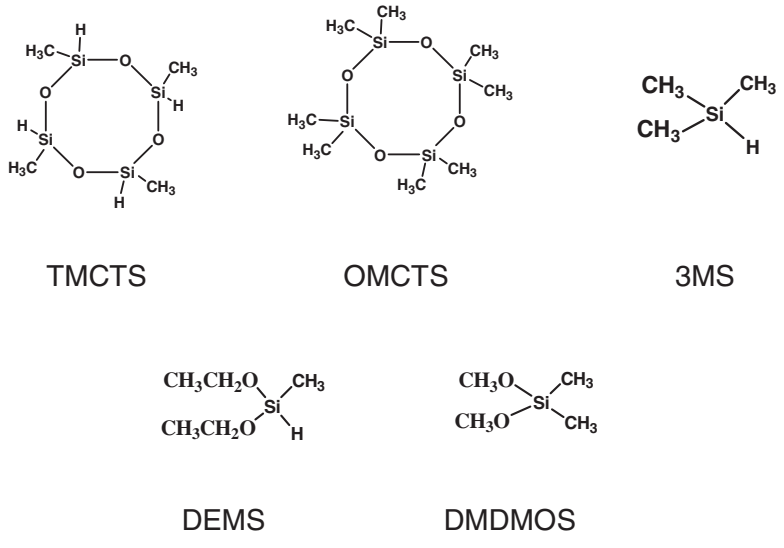

Figure 1.11 Schematic diagrams of some precursors used for the preparation of SiCOH films

performed using N_2O as the O source [51, 52], however it was found that this resulted in the incorporation of amine species in the films. These amine species caused resist poisoning during lithography performed on such films, therefore N_2O was later replaced with O_2 in the deposition process.

The deposition of SiCOH films is typically performed in a parallel plate RF PECVD reactor. The power to sustain the plasma is provided by either one or two RF power supplies of different frequencies. A typical frequency for the main power supply is 13.56 MHz, while the second power supply is usually of lower frequency and it can be used to apply a negative DC bias to the substrate. The films are deposited at temperatures up to about 400°C.

While SiCOH films are still prepared from different precursors, it was found that superior film properties are obtained when using cyclic precursors TMCTS [40] or OMCTS [18].

Porous SiCOH

One of the principal criteria for the choice of a new interconnect dielectric is its potential extendibility to later ULSI technology generations, requiring further reduced *k* values. The lowering of the dielectric constant of SiCOH below the values obtained for the dense films can be achieved by introducing porosity in the SiCOH films. It was claimed for many years that porosity can be introduced only in spin-on and not in PECVD films, but we have demonstrated that this is not true. While porosity could be created to some extent by the PECVD process through the adjustment of the plasma conditions, it can be achieved and controlled much more effectively by a subtractive process (removal of a fraction of the deposited film). The reduction of the dielectric constant can be accomplished by depositing multiphase films containing at least one unstable CH phase in addition to the SiCOH

skeleton phase and treating the films after deposition to remove the unstable phase from the material. (The CH notation reflects the atomic compositions of the phase but not its stoichiometry.) Ultralow-*k* porous SiCOH (pSiCOH) films can be prepared as a dual-phase SiCOH-CH material using the same PECVD method as described above and adding a hydrocarbon porogen (Por), as the CH precursor, to the SiCOH precursor feed to the reactor [46–48, 53].

During the deposition of pSiCOH the RF power needs to be adjusted and kept at levels small enough to prevent excessive dissociation of the SiCOH precursor, yet be sufficiently high to dissociate the porogen and incorporate its CH fragments in the deposited films. These requirements impose limitations on the choice of the organic precursor and on the plasma operating window for obtaining ultralow-*k* films.

The removal of the porogen can be done by annealing the films at 400–430°C in an inert ambient [46–48], or using e-beam or UV irradiation. The latter two techniques are much faster than the thermal anneal, can enhance the cross-linking in the cured films and improve their mechanical properties [54, 55].

The results presented later for pSiCOH are for thermally annealed films.

1.5.2 Properties of SiCOH and pSiCOH dielectrics

The structure of SiCOH and pSiCOH

Structural characterization of amorphous films is extremely difficult, but we have shown that it is possible to use FTIR to characterize the different bonding arrangements in the films and to obtain insights in the structure of SiCOH [15]. Typical FTIR spectra of such films are presented in Figure 1.12. The FTIR spectrum of a SiCOH film (Figure 1.12a) is generally

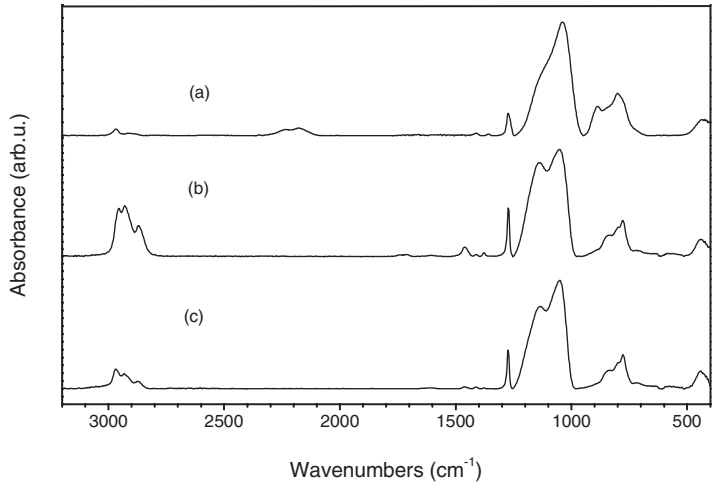

Figure 1.12 FTIR spectra of SiCOH and pSiCOH films: (a) SiCOH; (b) as-deposited pSiCOH; (c) annealed pSiCOH (Reproduced from [15] with permission from the American Institute of Physics)

characterized by a main Si–O stretch band at 1250–970 cm^{-1}, a Si–CH_3 ($SiMe_1$) stretch peak at 1274 cm^{-1}, a broad absorption band at 950–650 cm^{-1}, a small C–H stretch band at about 2900 cm^{-1} and a small Si–H stretch band at about 2220 cm^{-1}. A weak absorption at 1358 cm^{-1} can also be sometimes observed and assigned to bending of C–H in Si–CH_2–Si cross-links (references for specific peak identifications can be found elsewhere [15]).

The Si–O–Si asymmetric stretching band of the SiCOH film at 1250–950 cm^{-1} appears to have a peak at 1047 cm^{-1} with a shoulder at a larger wavelength. However, the Si–O–Si peak of the SiCOH film cannot be deconvoluted into two peaks, but has to be deconvoluted into three peaks centered at 1135, 1063, and 1023 cm^{-1}, as illustrated in Figure 1.13a [15, 56]. The assignments of these deconvoluted and all other observed peaks are presented in Table 1.1 [15].

The peak at 1135 cm^{-1} is attributed to larger angle Si–O–Si bonds in a cage structure with a bond angle of approximately 150° [15]. The peak at 1063 cm^{-1} is assigned to the stretching of smaller angle Si–O–Si bonds in an oxide network structure. The peak at 1023 cm^{-1} can be assigned to stretching of even smaller Si–O–Si bond angle, such as might be encountered in a networked silicon suboxide. While the SiCOH film may contain C–O–C or Si–O–C groups, any contributions from C–O–C or Si–O–C asymmetric stretching vibrations to the absorptions in the 1200–1000 cm^{-1} region cannot be identified because they overlap with the Si–O–Si asymmetric stretching band [15].

The broad absorption band at 950–650 cm^{-1} can be deconvoluted into five peaks centered at 892, 840, 802, 774, and 736 cm^{-1}, as shown in Figure 1.14a [15]. The peaks in this region are attributable to H–Si–O and Si–Me_n (n = 1, 2, or 3) vibrations, which overlap each other, making definitive assignments difficult. Nevertheless a detailed analysis has enabled the identification of these peaks as contributed from overlapping vibrations from H–Si–O, $SiMe_1$, $SiMe_2$ and $SiMe_3$ bonds (see Table 1.1) [15].

An absorption band at 440 cm^{-1} is also observed in Figure 1.12. This absorption has been attributed to bond bending of networked Si–O–Si, ring opening vibrations, and potentially Si–Si stretching vibrations [15].

The as-deposited pSiCOH films, prepared with the addition of organic porogen to TMCTS, are characterized by a strongly increased peak intensity in the 3100–2700 cm^{-1}

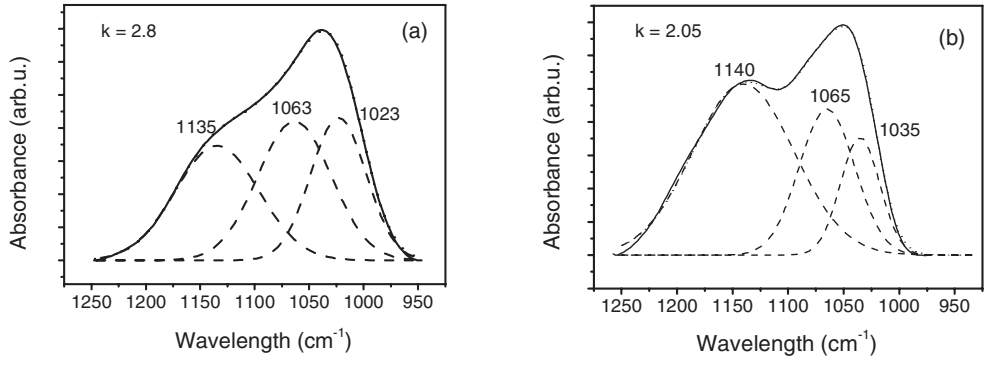

Figure 1.13 Deconvolution of the FTIR SiOSi absorption band: (a) of SiCOH; (b) of pSiCOH (Reproduced from [15] with permission from the American Institute of Physics)

Table 1.1 FTIR peak assignments. Major contributors are listed first for each vibration. ν = stretching, δ = bending, ρ = rocking, a = antisymmetric, s = symmetric (from [15], reproduced with permission of American Institute of Physics)

k = 2.8	k = 2.05	Mode	Comment
2969	2968	ν^a C–H_3	sp^3 CH_3
		ν^s C–H_3	sp^3 CH_3
2916	2932	ν^a C–H_2	sp^3 CH_2
2880	2875	ν^s C–H_2	sp^3 CH_2
2232		ν^s Si–H	H–SiO_3
2178		ν^s Si–H	H–SiO_2Si
		ν^s Si–H	H–SiOSi
	1740, 1714	ν C=O	As-deposited only
	1461	δ C–H_2	CH_2 isolated from Si
1412	1412	δ^a C–H_3	$SiMe_x$
1358	1379	δ C–H_2	Si–CH_2–Si
1273	1274	δ^s C–H_3	$SiMe_x$
1135	1140	ν^a Si–O–Si	Cage Si–O–Si angle ~150°
		ν C–O	Si–O–C
1063	1065	ν^a Si–O–Si	Network (network) Si–O–Si angle ~144°
1023	1035	ν^a Si–O–Si	Silicon suboxide, Si–O–Si angle <144° D_{3h} ring structure
890		δ H–Si–O	H–SiO_3
		ν Si–C, ρ^s CH_3	$SiMe_2$
		δ H–Si–O	H–SiO_2Si
848	843	δ H–Si–O	Network smaller angle
		ν Si–C, ρ^a CH_3	$SiMe_3$
802	800	ν Si–C, ρ^a CH_3	$SiMe_2$
		ν Si–C, ρ Si–CH_3	$SiMe_1$
773	779	ν Si–C, ρ CH_3	$SiMe_1$
		ν Si–C, ρ^s CH_3	$SiMe_3$
730	720	ν^s Si–O–Si	
440	440	δ of O–Si–O	Network and ring opening vibratins

region (C–H_i stretching vibrations), and reduced intensity of the 890 and 848 cm^{-1} absorptions (H–Si–O bending and $SiMe_x$ vibrations), compared with the films deposited from TMCTS only, as shown in Figure 1.12b. The new absorptions at 2932 (CH_2 stretch) and 1461 cm^{-1} (CH_2 bend, isolated from silicon) and the increased relative absorption of the CH_2 stretch at 2875 cm^{-1} are the result of the incorporation of organic components in the as-deposited SiCOH films.

The annealed pSiCOH film has reduced C–H_i stretching band (3100–2700 cm^{-1}) and CH_2 bend peak (1461 cm^{-1}) intensities (see Figure 1.12c) indicating a significant loss of the CH from the dual phase films during annealing. In the annealed pSiCOH film, the Si–O–Si

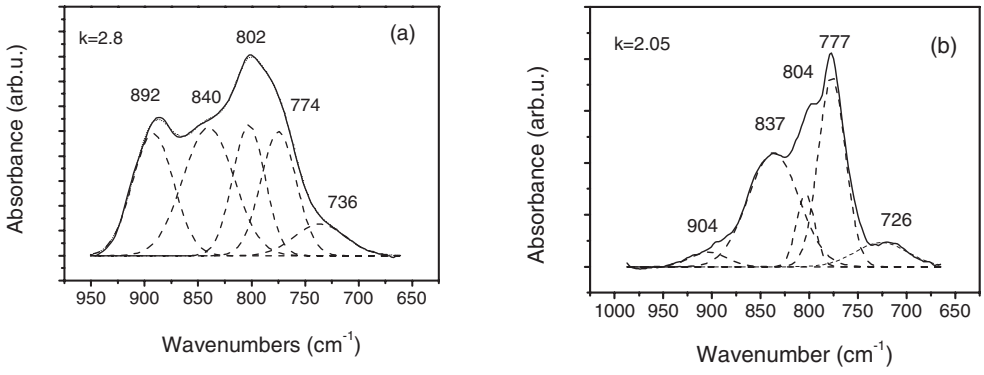

Figure 1.14 Deconvolution of the SiMe and HSiO absorption bands: (a) of SiCOH; (b) of pSiCOH (Reproduced from [15] with permission from the American Institute of Physics)

asymmetric stretching band has split into an apparent doublet, which can be deconvoluted into three peaks shown in Figure 1.13b. The fraction of the cage Si–O–Si peak of the pSiCOH film has increased compared with that of SiCOH films deposited with TMCTS only, indicating an enhancement of the cage structure in these films [15].

The broad absorption band at 950–650 cm^{-1} in the annealed pSiCOH film has decreased in intensity relative to the dense SiCOH film. Deconvolution of this band yields again 5 peaks at 904, 837, 804, 777 and 726 cm^{-1} (see Figure 1.14b). A comparison of these peaks with those of the SiCOH film shows a very strong reduction of the absorption at 904 cm^{-1}, and a decreased absorption at 804 cm^{-1}.

The FTIR spectra of the SiCOH films indicate that the films are highly cross-linked complex materials, primarily composed of a network structure formed by a mixture of different bonding arrangements in cyclic and some linear branch structures. Based on the analysis of the FTIR spectra presented above and taking into consideration the possible reaction pathways leading to the deposition of the films, the SiCOH films contain Si–O–Si, Si–Me_i, Si–CH_2–Si, Si–CH_2–O–Si and Si–Si moieties. The structure of the dense SiCOH films can be described by the diagram shown in Figure 1.15(a) and the structure of porous pSiCOH films can be described by the diagram shown in Figure 1.15(b) [15]. The pSiCOH films have an enhanced fraction of cage-type Si–O bonds and enhanced porosity created by the loss of the incorporated organic fraction during the annealing compared with dense SiCOH films [15].

The FTIR spectra and film structures described above for TMCTS-based films are typical for SiCOH and pSiCOH films prepared from other precursors. Usually, only detailed careful analysis of FTIR spectra will reveal differences (sometimes subtle) between films prepared from different SiCOH precursors.

Index of refraction

The dense SiCOH films are generally characterized by an index of refraction of 1.43 to 1.46 at 633 nm. Introduction of porosity in pSiCOH films results in a decrease in the refractive

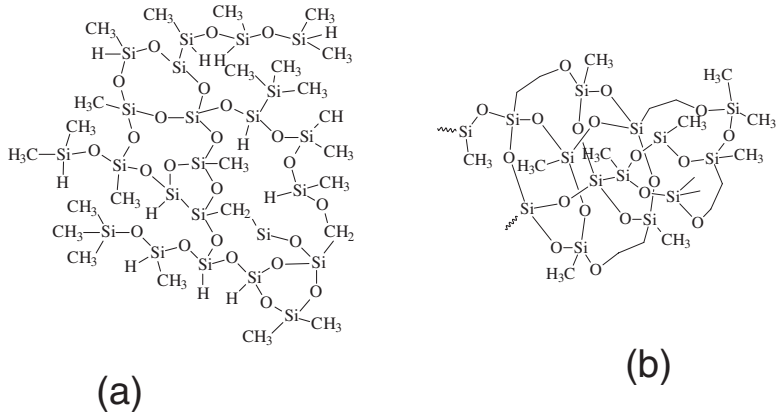

Figure 1.15 Diagram of the structure of (a) SiCOH; (b) pSiCOH films (Reproduced from [15] with permission from the American Institute of Physics)

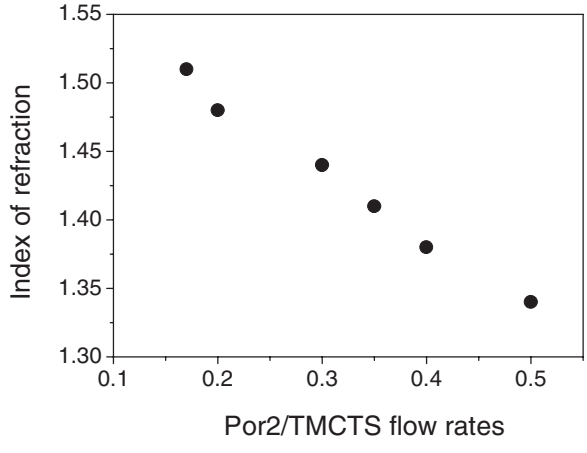

Figure 1.16 Index of refraction of pSiCOH films vs porogen concentration in the plasma feed (Reproduced from [56] with permission from the American Institute of Physics)

index of the films due to the reduction in film density. Figure 1.16 [56] illustrates the effect of increasing porogen content in the plasma on the index of refraction of annealed pSiCOH films deposited from TMCTS and a specific porogen [56]. The index of refraction decreases to 1.33 with increasing Por/TMCTS ratio in the gas feed. As we shall see later, the Por/TMCTS ratio is directly correlated to the degree of porosity in the films; therefore the decrease of the index of refraction shown in Figure 1.16 is caused by the increase in film porosity.

The trend illustrated above for TMCTS-based films is true for films prepared from other SiCOH and porogen precursor combinations, however the values of the index of refractions of films with same k values can be affected by the precursor mixture used for its preparation.

Electrical properties

It was shown in 1999 [40] that SiCOH films with dielectric constants as low as 2.85 can be obtained by adjusting the plasma parameters during the deposition of the films. It was found that low-*k* SiCOH films have to be grown under conditions which cause low dissociation of the precursor in the plasma and a minimal ion bombardment of the growing film. As mentioned above, in order to reduce further the dielectric constant of SiCOH films in a controlled way the films have to be prepared as a multiphase structure, using an organic porogen together with the SiCOH precursor in the plasma [46]. It was shown that the lowest achievable dielectric constant in pSiCOH films depends on the organic precursor used [47, 48], as illustrated in Figure 1.17 [56]. The dielectric constant of the films deposited from TMCTS with the Por1 organic precursor reached a minimum value of 2.4 when deposited at a relatively low Por1/TMCTS ratio. In contrast, the dielectric constant of the films deposited with the Por2 organic precursor decreased continuously for the investigated range, reaching an extreme low *k* value of 2.1 [46, 47, 56].

The different behaviors observed for the two precursor systems can be explained with reference to Figure 1.18 [56]. The fraction of organic porogen concentration in the as-deposited film increases with increasing Por/TMCTS ratio in the plasma. If the removal of the porogen during annealing occurred without film shrinkage the dielectric constant would decrease continuously with increasing Por/TMCTS ratio. However, Figure 1.18 shows that the films shrink significantly during the removal of the porogen and the shrinkage (thickness loss) is strongly dependent on the choice of organic precursor.

The thickness loss of the films deposited with Por1 increases continuously with the Por1 fraction in the gas feed and reaches 50% at a relatively low Por1 fractions. This indicates that, at higher fractions of porogen incorporated in the as-deposited films, the removal of the porogen results in a collapse of the thickness rather than in formation or enhancing porosity. As a result, the dielectric constant does not decrease further with increasing

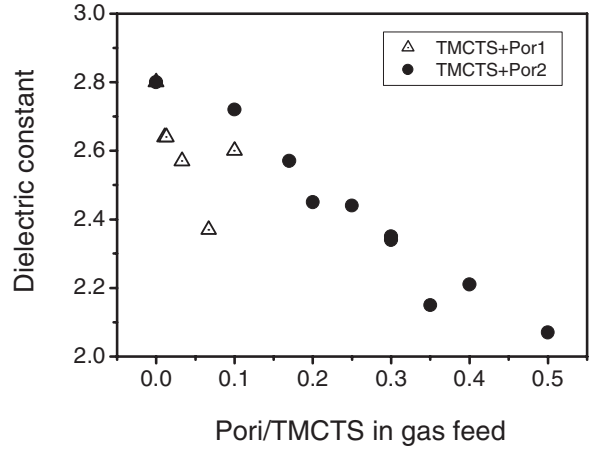

Figure 1.17 Dielectric constants of pSiCOH films deposited from TMCTS and different porogens vs porogen concentration in the plasma feed (Reproduced from [56] with permission from the American Institute of Physics)

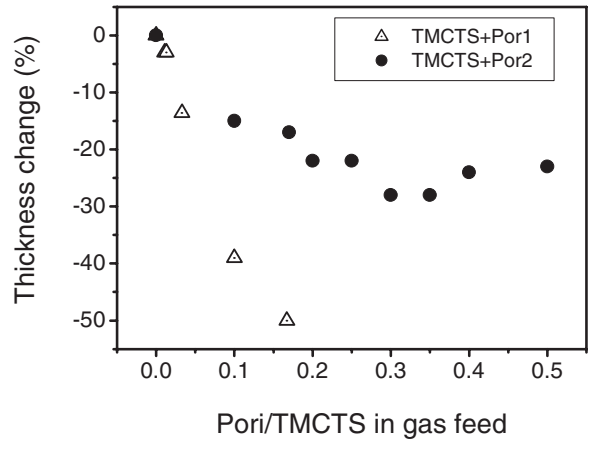

Figure 1.18 Thickness change during annealing pSiCOH films deposited from TMCTS and different porogens vs porogen concentration in the plasma feed (Reproduced from [56] with permission from the American Institute of Physics)

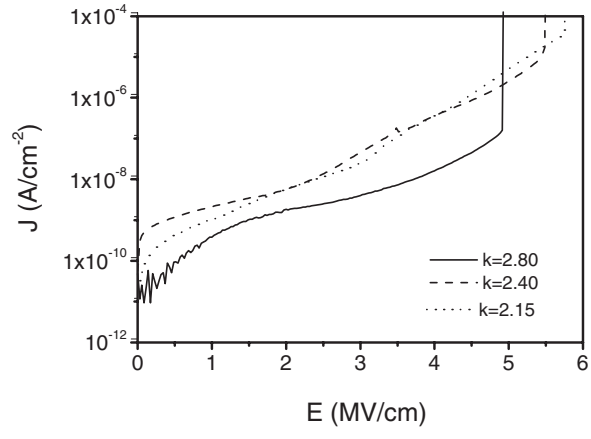

Figure 1.19 Leakage current vs electric field for SiCOH (k = 2.8) and pSiCOH (k = 2.5 and 2.15) films (Reproduced from [56] with permission from the American Institute of Physics)

Por1/TMCTS ratio beyond the value corresponding to the minimum k. For the films deposited with porogen Por2 the shrinkage reaches a plateau of about –25%, therefore the increase of the porogen incorporation results in continuous increase in the porosity of the film and corresponding decrease in its dielectric constant (Figure 1.17). The achievement of an extreme low-k SiCOH is thus strongly dependent on the choice of the proper organic precursor.

Another important electrical characteristic of dielectric films is the leakage current, which is presented for several films as a function of the electric field in Figure 1.19 [56]. The

SiCOH films with $k = 2.8$ have low leakage current, reaching a value of only 2×10^{-10} A/cm^2 at a field of 1 MV/cm. The extreme low-k pSiCOH films ($k = 2.40$, 2.15) have larger leakage currents than the dense SiCOH, yet the leakage current remains below 2×10^{-9} A/cm^2 at 1 MV/cm, a value significantly lower than imposed by the requirements for integration of the dielectric in a ULSI chip. The breakdown fields of these specific films were 4.8 MV/cm and 5.5 MV/cm, respectively. The apparent lower breakdown field observed in Figure 1.19 for the SiCOH film ($k = 2.8$) was measured for a film prepared in lab conditions and is not representative for SiCOH films prepared in manufacturing. The latter have been optimized to obtain breakdown fields larger than 9 MV/cm [18].

Mechanical properties

The mechanical properties of the SiCOH films are inferior to those of the SiO_2 or FSG dielectrics. An initial comparison of mechanical properties of SiCOH films can be found elsewhere [57] where it was observed that films prepared from cyclic siloxane precursors have superior values to those prepared from linear methylsilanes. When integrating the low-k SiCOH in an ULSI chip the lowest k values are preferred for best performance of the integrated circuit, while good reliability and mechanical robustness of the chip require the highest possible mechanical strength. The mechanical properties of SiCOH dielectrics usually decrease with decreasing k values for films deposited by a specific processing system (tool and gas mixtures). Nevertheless, the flexibility of the PECVD process combined with the amorphous structure of SiCOH provides a certain latitude in enhancing the mechanical properties of the films, while retaining the desired low k values [18].

Results of such an optimization of the properties of SiCOH films are presented in Figures 1.20 and 1.21 and Table 1.2 [18]. Figure 1.20 shows the FTIR spectra of several dense SiCOH films with $k = 2.8$–3.0, with mechanical properties improving from V2 to Gen 3 as shown in Table 1.2 [18]. No correlation was found between the elastic modulus E or

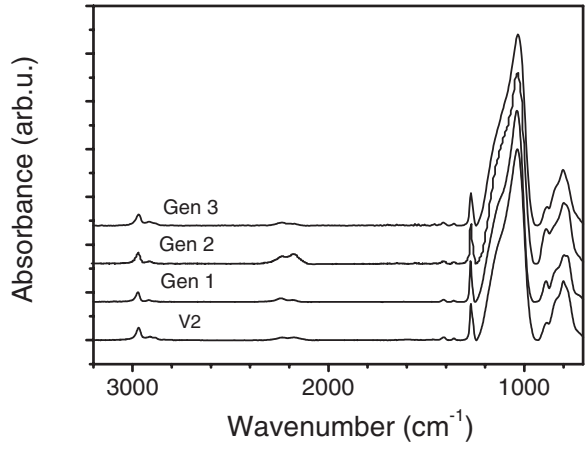

Figure 1.20 FTIR spectra of different SiCOH films deposited from cyclic siloxane precursors (Reproduced with permission from [18], Copyright 2004 IEEE)

hardness H and the intensity of the Si–H absorption peaks at 2178 and 2234 cm^{-1} [15]. However, it was found that the elastic modulus increases and the stress in the films decreases with increasing fraction of network oxide (at about 1062 cm^{-1}, obtained by the deconvolution of the SiO absorption band at 1250–950 cm^{-1}), as shown in Figure 1.21 [18].

Table 1.2 presents the dielectric constants and corresponding mechanical properties of several types of SiCOH films [18]. As can be seen in the table, it was possible to optimize the films and increase the elastic modulus from 6 to 16 GPa and decrease the tensile stress in the films from 63 to 20 MPa for only small variations in the value of the dielectric constant of the SiCOH films.

The mechanical properties of porous pSiCOH films are reduced significantly by the porosity in the films, and E and H are much smaller than in the dense SiCOH and generally decrease with decreasing k values [56, 57]. The integration of pSiCOH films in an ULSI device will therefore require modifications of the structures of the interconnect to enable the fabrication of mechanically robust devices.

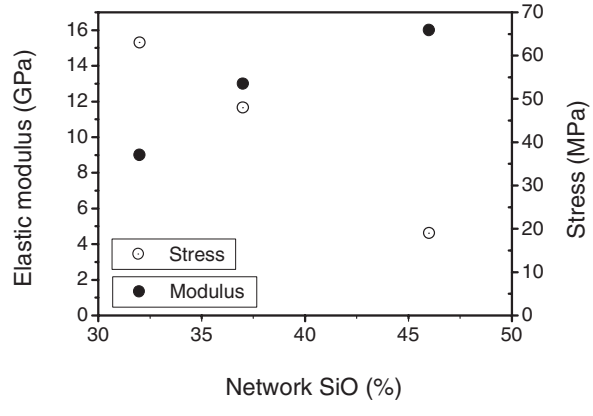

Figure 1.21 Elastic modulus and stress of SiCOH films from Figure 1.20 vs fraction of network oxide (Reprinted with permission from [18], Copyright 2004 IEEE)

Table 1.2 Properties of optimized SiCOH films

Recipe	k (0% r.h.)	V_{bd} (MV/cm)	E (GPa)	H (GPa)	Stress (MPa)	Crack velocity (m/s @ 3 μm)	Critical thickness (μm in water)
V1	2.9–3.0	6	13	2.2	55	~5E-9*	~2.5*
Gen1	2.8–2.9	8	9	1.4	63	5E-5	1.5
Gen2	3.0–3.1	9	13	2.1	50	2.2E-10	3.5
Gen3a	3.0–3.1	9	16	2.5	20	0	>7
Gen3b	2.9–3.0	9	15	2.2	30	0	>7*

*Expected value, not measured

Cracking velocities

The SiCOH films are typically under tensile stress and therefore have a tendency to crack if their thickness is larger than a critical value. Although the critical values of dense SiCOH films are typically well above the thicknesses of interest for interconnect structures, these critical values can decrease significantly when the films are deposited on a low-modulus substrate, such as lower levels of SiCOH, and when there are underlying critical Cu metal structures [58].

The driving force G leading to the cracking of a tensile film is given by:

$$G = 1.1\,\sigma^2 h/E$$

where σ = film stress and h = film thickness. The optimization of the SiCOH films, which raised the modulus from 9 to 16 GPa and reduced the stress from 63 to 20 GPa, resulted in a reduction of G by a factor of ~17 and a corresponding increase of the critical thickness for cracking in water of SiCOH films deposited on Si from 1.5 μm to beyond 7 μm. This is illustrated in Figure 1.22 [18] that shows the crack development velocity in water as a function of film thickness for a variety of SiCOH films. The increase of the critical thickness is important to enable multiple levels of thick dual damascene Cu/SiCOH lines to be built on multiple lower Cu/SiCOH levels while preventing the possibility of cracking.

Coefficient of thermal expansion

The coefficient of thermal expansion (CTE) has been determined by measuring the stress in films deposited on a silicon wafer, assuming modulus values of 11 and 3 GPa for SiCOH (k = 2.8) and pSiCOH (k = 2.1), respectively, and assuming a Poisson ratio ν = 0.3. The CTE values for Si were taken from the CRC *Handbook of Chemistry and Physics.*

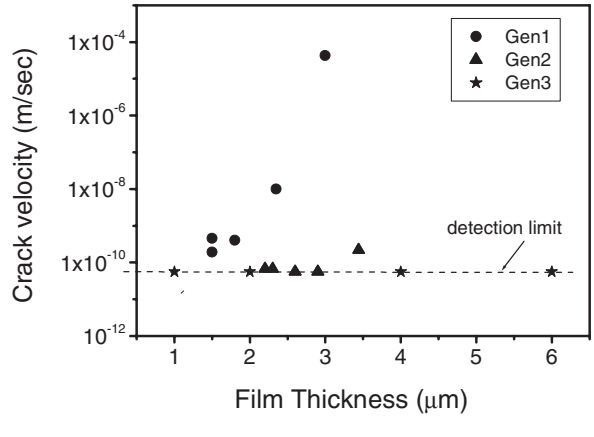

Figure 1.22 Crack development velocity at 100% humidity in the SiCOH films of Figure 1.20 (Reprinted with permission from [18], Copyright 2004 IEEE)

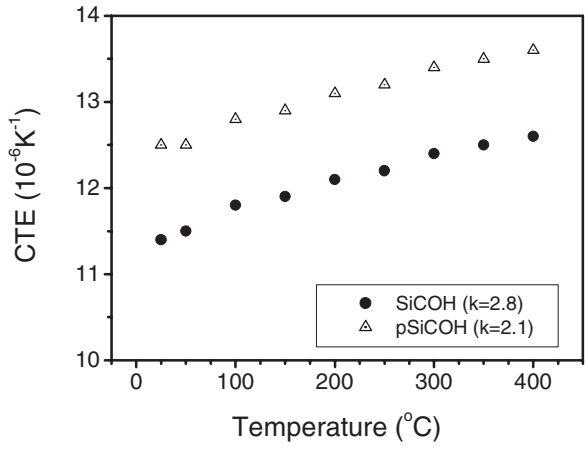

Figure 1.23 Coefficients of thermal expansion of SiCOH and pSiCOH as a function of temperature (Reproduced from [56] with permission from the American Institute of Physics)

Figure 1.23 [56] presents the CTE of SiCOH and pSiCOH films as a function of temperature, over a range of temperatures typical for the integration processing. It can be seen that the CTE of the SiCOH film with $k = 2.8$ spans a range of 11.8–12.3 $\times$ 10^{-6}/K, while that of the extreme low-k pSiCOH film with $k = 2.1$ has slightly higher values. These values are by at least a factor of 5 lower that the CTE of polymeric films and very close to that of Cu (17 $\times$ 10^{-6}/K), with which they have to be integrated. Therefore, the use of PECVD SiCOH or pSiCOH films in the interconnect structures induces lower thermal stresses than polymeric films with similar k values.

Porosity in pSiCOH

The reduction in the dielectric constant in pSiCOH film is achieved by inducing porosity in the films as described above. The degree of porosity, the size of the pores and the pore size distribution (PSD) can affect the behavior of the films during their integration in the BEOL of a ULSI, therefore it is important to characterize these material characteristics. Due to the small size of the pores in pSiCOH films (most less than 2 nm diameter) these pores cannot be visualized directly by any microscopic techniques. The porosity parameters can be evaluated only by indirect techniques whose data are interpreted by corresponding models, as described above in Section 1.3 and in Chapter 3 of this book.

Typical PSDs of two pSiCOH films of different k values, as obtained by ellipsometric spectroscopy are illustrated in Figure 1.24 [21]. A comparison of the degrees of porosity and PSD values obtained by several methods for the same films is presented in Table 1.3 [21]. The data show a scattering of the values obtained by the different techniques, however a calculation of film densities and dielectric constants based on these porosity data showed reasonable agreement to the experimental data. Due to the variability in the values of the porosity characteristics determined by different techniques it is important to compare the properties of different pSiCOH films using the same porosity characterization technique.

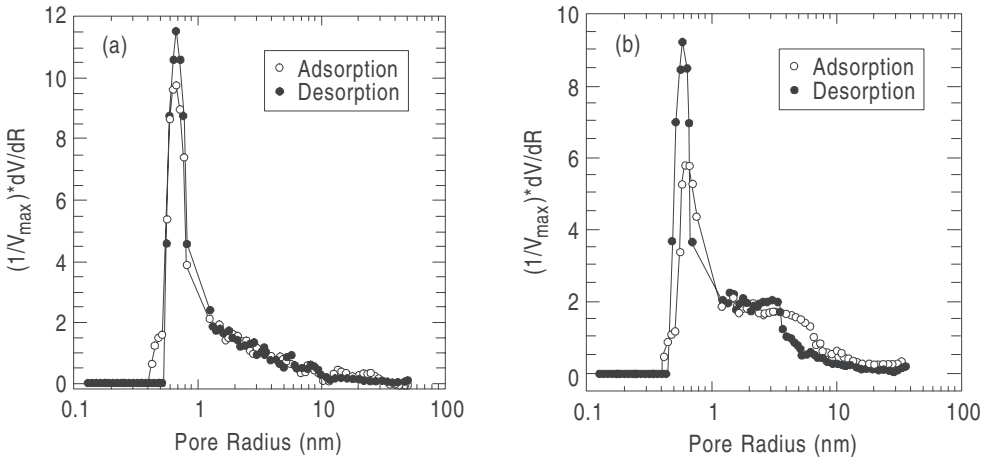

Figure 1.24 Pore size distribution in pSiCOH films: (a) $k = 2.40$; (b) $k = 2.05$ (Reproduced from [21] with permission from the American Institute of Physics)

Table 1.3 Porosity and average pore size in SiCOH and pSiCOH films (Reproduced from [21] with permission from American Institute of Physics)

Sample	k	Degree of porosity (%)			Pore diameter (nm)		
		PAS	XR	EP	PALS	SAXS	EP
SiCOH	2.85	0	0	0	N/A	N/A	N/A
pSiCOH	2.40	20	13	17	1–4	<1.6	1.3
pSiCOH	2.05	29	22	28	1–7	<2.2	<5

1.5.3 Integration of SiCOH as the interconnect dielectric

The initial integration of PECVD low-k SiCOH films with Cu metallization for 130 and 90 nm CMOS has been reported by a number of institutions as early as 2000 [59–62], however its incorporation in semiconductor products has been achieved only in the 90 nm technology. Recent presentations on Cu/SiCOH interconnect integration show that the integration of SiCOH with the Cu metallization has become the predominant path chosen by the industry for the interconnect structures at the 90 nm technology [63–66]. At IBM, the optimization of the SiCOH characteristics has enabled the successful Cu/SiCOH integration with a full-generation capacitance reduction relative to Cu/FSG with no reduction in reliability levels [63].

Figure 1.25 [63] shows a cross-section of an IBM interconnect structure in 90 nm Cu/low-k technology consisting of ten levels of Cu wiring plus one W local interconnect and one Al(Cu) terminal level. The Cu wiring has four hierarchical scaling factors for pitches and cross-sectional dimensions, denoted as 1×, 2×, and 6×. All 1× and 2× levels are built with low-k SiCOH dielectric, and the final two 6× levels are built with SiOF (FSG). Such a structure has already been incorporated in IBM's products based on the 90 nm technology

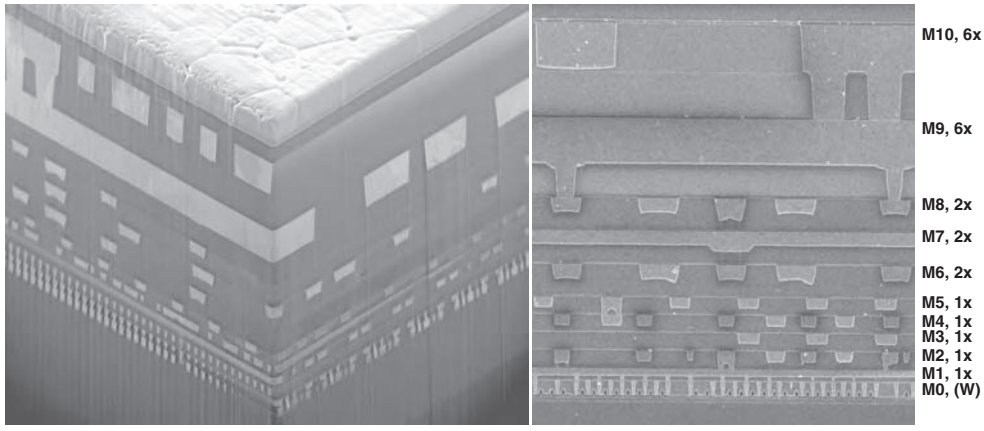

Figure 1.25 SEM micrograph of a ten Cu level microprocessor; all 1× and 2× levels are Cu in SiCOH. Metal levels: W one local interconnect level plus contact level; Cu ten levels, first eight in low-*k*, final two in SiOF; Al one terminal metal level, used for pads and wiring (Reprinted with permission from [63], Copyright 2004 IEEE)

providing ~20% capacitance reduction compared with similar structures using FSG dielectric and with very significant power reduction at same performance [63].

1.6 CONCLUSIONS

After many delays and extensive research and development efforts, PECVD dielectric films have finally reached maturity to be used as the low-*k* insulators in the interconnect structure of ULSI circuits. PECVD SiCOH has emerged as the winner low-*k* dielectric and is only the second new material, after Cu, to be introduced successfully in Si technology. Films with dielectric constants $k \sim 2.9$–3.1 have been successfully introduced in products at the 90 nm technology node and are used at the next 65 nm generation too.

The potential extendibility of SiCOH dielectrics to later technology generations has been demonstrated by the development of porous SiCOH films (pSiCOH) with ultralow dielectric constants down to 2.0. The development of pSiCOH films has also shown a path for the creation of other types of porous materials by PECVD.

ADDENDUM

In spite of the difficulties associated with the integration of ultralow-*k* dielectrics in the ULSI interconnects, the technology has lately made fast strides. Thus, by the time of the proofreading of this manuscript in November 2006, integrations of ultralow-*k* PECVD dielectrics have been demonstrated for advanced SiCOH ($k = 2.7$) at 65 nm [67] and for pSiCOH ($k = 2.4$) at 45 nm [68].

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2 Spin-on Dielectric Materials

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2.1 INTRODUCTION

As device sizes decrease and device densities increase, chip performance will begin to erode without modified materials. This is a significant problem for the semiconductor industry where, until relatively recently, improvements in performance have been dictated by scaling issues which have resulted in doubling of device densities every 12–18 months [1]. This situation began to change as we passed the 0.25 μm generation and the effect on performance is exacerbated as the dimensions continue to shrink.

The degradation of chip performance is characterized by cross-talk between conductor lines and signal delays in the back-end-of-the line (BEOL) interconnect wiring. As device sizes decrease and densities increase, the signal delays are dominated by the BEOL wiring levels rather than by the semiconductor devices themselves. BEOL signal delays are characterized by an *RC* time constant where *R* is the metal line resistance and C is the integrated capacitance [2]. In modern chips there can be 8–10 wiring levels, hundreds of millions of functioning devices and up to 10 000 m of interconnect wiring. The RC interconnect delays depend on the metal resistivity, the wiring configuration (levels, length, dimensions, aspect ratios, wiring pitches, etc.) and the capacitance as shown in Figure 2.1. In 1997, IBM described the introduction of copper to replace aluminum which until then had been the

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$$RC_{delay} = 2\rho\varepsilon\left(4L^2/P^2 + L^2/T^2\right)$$

$$Power = CV^2 f$$

R = line resistance
C = line capacitance
L = line length
P = metal pitch
T = metal thickness
ρ = resistivity
ε = dielectric constant
V = applied voltage
f = frequency

Figure 2.1 Delay and power consumption for back-end-of-the-line (BEOL) interconnect wiring

standard interconnect wiring [3]. This resulted in a drop in the wiring resistivity of almost 30%. It also necessitated a change in the process for producing planar layers from etch back to metal removal using chemical mechanical polishing (CMP) damascene processes [4]. CMP places additional mechanical stresses on the dielectric materials, resulting in new integration issues. Advantageous initially, the switch to copper would provide only a short-lived solution to the *RC* delay issues. Equally important is the back-end capacitance which increases with decreasing wiring pitches and spaces between the individual wiring levels. A primary determinant of the wiring capacitance is the dielectric constant *k* of the insulating media such that a decrease in *k* results in a corresponding decrease in *C*. Although it receives far less publicity than the signal delay, power consumption, which is also shown in Figure 2.1, is a critical issue for modern chips, limiting the speed to which they can be driven or ultimately requiring elaborate cooling schemes to maintain performance.

Figure 2.1 shows that power consumption depends on the driving voltage *V* of the transistor devices, which is already approaching threshold minima, operational frequencies *f*, which are steadily increasing, and the capacitance. The result is that by decreasing the dielectric constant of the insulating media, you can, in principle, produce faster chips running at lower power. Herein is the driver pushing semiconductor manufacturers inexorably toward low-*k* dielectric insulators.

From the beginning of integrated on-chip devices through the 0.18 μm generational node, the insulator has been SiO_2. As a result, many of the integration procedures that have evolved are based on the growth, patterning and removal of SiO_2 during processing. This material has remarkable properties for device fabrication including exceptional thermal stability, superb electrical properties and enviable mechanical properties. The dielectric constant ranges from 3.9 to 4.2, depending on the mode of deposition, thermal stabilities exceed 500°C, breakdown voltages >6 MV cm^{-1} are achieved and the modulus ranges from 55 to 73 GPa, again depending on the mode of deposition. In almost every important category, except for dielectric constant, the properties of any low-*k* material may be expected to be inferior to SiO_2. Furthermore, in order to produce a dielectric material with device generational extendibility (i.e., similar elemental composition, but progressively decreasing dielectric constant), the concept of porosity must be embraced. The introduction of porosity superimposes a host of porosity-specific integration issues onto an already daunting list. The latter includes thermal stabilities to 450°C, glass transition temperatures T_g above 450°C, dielectric constants <4.0, good adhesion to caps, hardmasks, etch stops, liners, etc., low water absorption, chemical compatibility with metallurgy, solvent resistance, compatibility with CMP, selective etch characteristics, good mechanical properties and others. For porous variants, all of the above apply, in addition pore sizes must be small relative to the

Table 2.1 Dielectric material candidates. CVD = chemical vapor deposition, SOD = spin-on deposition

Dielectric material	Deposition method	k
Dense materials		
Silicon dioxide	CVD	3.9–4.5
Fluorosilicate glass (FSG)	CVD	3.3–4.0
Polyimides	SOD	3.1–3.4
HSSQ	SOD	2.9–3.2
Diamond-like carbon (DLC)	CVD	2.7–3.4
Carbon-doped oxide/(CDO)	CVD	2.8–3.2
Parylene N	CVD	2.7
Benzocyclobutenes	SOD	2.6–2.7
Fluorinated polyimides	SOD	2.5–2.9
Silsesquioxanes	SOD	2.6–2.8
Polyarylene ethers	SOD	2.7–2.9
Polyarylenes	SOD	2.6–2.7
Parylene-F4	CVD	2.4–2.5
Fluoropolymers	SOD/CVD	1.9–2.1
Porous materials		
Porous organics	SOD	2.1–2.2
Aerogels (silica)	SOD	1.8
Xerogels (silica)	SOD	2.0–2.5
Mesoporous silicas	SOD	1.3–2.6
Mesoporous organosilicas	SOD	1.8–2.2
Porous HSSQ/MSSQ	SOD	1.5–2.2
Zeolite nanocrystals	SOD	1.8–2.3
Porous CDO	CVD	2.0–2.5

smallest device features and be evenly distributed throughout the film. The porous films must also be compatible with processing chemicals and environmental influences. Table 2.1 shows a variety of materials which have been auditioned as low-k dielectrics at one time or another; all fall short of SiO_x in one or more important categories.

Approximately 9 years ago, interest in low-k on-chip insulators was accelerating, there were a plethora of possible candidates and the ITRS roadmap predicted that $k < 2.0$ materials would be in use by 2003 in the 130 nm node and dielectric constants <1.5 would appear by 2009 in the 65 nm node. In 2006, the list of potentially viable low-k candidates has narrowed substantially and the integration of low-k materials has proven more difficult than ever imagined. As a result, the ITRS schedule for low-k dielectrics has slipped dramatically. The first true low-k materials ($k \sim 3.0$) have only recently appeared in volume production at the 90 nm node and the next generation chips (65 nm node) will utilize dense materials with $k = 2.7$. The semiconductor roadmap updated in 2005 [5], calls for $k < 2.4$ at the 65 nm node in 2007 and ULK materials with $k < 2.2$ in the 45 nm node targeted for the 2009–2010

timeframe. The $k < 2.0$ materials originally targeted in 1997 for 2003 (130 nm node) now appear on the roadmap in 2012–2013 in the 45 nm node and beyond.

Dielectric materials may be roughly classified as either largely inorganic containing elements of carbon, hydrogen, oxygen, nitrogen, etc., but also substantial amounts of silicon or largely organic, containing the same elements, but usually relatively little or no silicon. These two main classes of dielectric materials have very different properties. While both can be thermally stable with good electrical properties, the organics tend to be soft, but tough, with thermal coefficients of expansion (CTE) exceeding 50 ppm. The inorganic materials, on the other hand, are hard, but brittle, and are prone to fracture. The coefficients of expansion are much lower, usually less than 25 ppm. Each class of materials therefore provides its own unique set of integration challenges.

Dielectric materials may also be distinguished by the mode of application. Spin-on techniques have been perfected over the years, primarily for the application of liquid photoresists and consistently deliver high-quality coatings of controlled thickness. In general, organic dielectrics are applied by spin coating, although the technique may also be utilized for some inorganic materials as well. Gas phase deposition techniques such as chemical vapor deposition (CVD) and plasma-enhanced chemical vapor deposition (PECVD) are also common deposition modes. Here the reagent(s) are delivered in the gas phase to a chamber containing the substrate to be coated. The substrate is usually heated to high temperatures to initiate surface reactions and this is often used in conjunction with a plasma discharge for activation. As a result of the thermal and/or plasma activation, considerable bond breaking occurs and highly energetic species are produced. Dielectric materials prepared by CVD and PECVD processes are largely inorganic although Parylene-based conformal coatings are organic and are prepared by thermal cracking of a precursor to produce highly reactive *p*-xylylene intermediates which polymerize upon condensation [6]. CVD and PECVD deposition processes have a long history in semiconductor manufacturing, dating back to the application of silica dielectrics. As a result, risk-adverse semiconductor manufacturers have become comfortable with gas phase deposition processes and have accumulated a considerable capital investment in the complex tools required. In general, deposition equipment for spin-on deposition is cheaper than that for PECVD, but the materials are more expensive and there is more waste associated with spin-on. The early heats in the race for low-*k* dielectrics have gone to the CVD proponents [7]. The CVD dielectrics are largely inorganic, cross-linked organosilicates termed carbon-doped oxides (CDO), although the term SiCOH often appears in the literature for such materials. CVD deposited CDO films are the materials of choice for the current 90 nm node and dense materials with somewhat lower *k* values (2.7) will likely be utilized at 65 nm. In general, materials with $k > 2.5$ are considered to be dense and those with $k < 2.5$ are porous to some degree, although even dense materials have some porosity associated with free volume. Spin-on materials are still in play for porous materials, particularly ultra low-*k* (ULK) with k values of 2.2 or lower.

As mentioned, PECVD processes involve considerable bond breaking and the formation of high-energy species. In this regard, the bonding arrangement in the product is often very different from that in the starting materials. This is not the case for spin-on materials, where the basic structure and bonding arrangement of the initial material are usually maintained to a large degree in the product. Product structural characterization of the insoluble cross-linked dielectric products is most easily performed using FTIR [8], Raman and solid state NMR (^{13}C and ^{29}Si) [9]. For organosilicates, the NMR techniques are extremely useful. Obviously spin-on precursors, which are soluble, may also be characterized spectroscopi-

cally using the same techniques. Although the product structural complexity for CVD materials is sometimes disconcerting, the range of processing parameters is large (e.g., mass flow rates, reagent mixtures, pressure, bias voltage, microwave/RF power, functional additives etc) and provides an opportunity for tuning the thermal, electrical and mechanical properties of the deposited film simply by turning some dials rather than by synthesizing new materials. This alone can provide a significant advantage in a quasi-combinatorial approach toward property optimization. However, there are certain applications for which CVD processes are ill suited. For example, if gap filling is required, this is often best achieved with spin-on materials. The generation of ULK porous materials with dielectric constants below 2.0 and good mechanical and electrical properties is problematic with CVD, but easily achievable with spin-on. The deposition of thermally sacrificial layers and features is often more easily accomplished with spin-on materials. If the film properties are enhanced by some organization and long-range order in either hybrid materials or the porous films so derived, this will not be achieved using CVD or PECVD techniques. Finally, block copolymer self-assembly for the generation of sublithographic features (e.g., the generation of nanoporous etch masks, formation of oriented templates, etc.) requires spin-on capabilities [10].

CVD processes are adequately described elsewhere; likewise, thin dielectric film characterization and techniques for characterizing porosity have been reviewed previously [11] and will not be discussed in detail here. The purpose of this chapter is to discuss dielectric materials that may be applied by spin-on techniques. This discussion will survey both dense and porous materials, since the latter are needed to produce truly extendible dielectrics.

2.2 SPIN-ON DENSE MATERIALS

2.2.1 Organic polymers

In the mid-1990s when the hunt for new low-k replacements for SiO_2 was heating up, there were numerous high-temperature organic polymers under consideration. Mechanically these materials are soft relative to inorganic materials, but the polymers are tough and resist cracking. Thermal stabilities are often questionable above 400°C and the thermal coefficients of expansion are large (>50 ppm) relative to many of the inorganic materials and metallurgy used in integration. The latter causes stress build-up during the repetitive thermal cycling required for multilayer BEOL integration. In addition, processes such as wire bonding often cause deformation in the softer organic materials which was not an issue in SiO_2. The demanding requirements for integration (described previously) rapidly eliminated some promising candidates (e.g., polyimides, polyquinolines, polybenzocyclobutenes etc.). Polyimides, which have many other microelectronic applications, presented integration concerns because the dielectric constants of very thermally stable examples were often not that low ($k > 3.0$), the electrical properties were sometimes anisotropic and water uptake (1–4%) was viewed as a problem. These and other integration requirements also quickly eliminated surfactant- stabilized nanoparticulate Teflon [12] in spite of the very low ($k < 2.2$) dielectric constants. Initially promising dielectric studies on Cyclotene™, a benzocyclobutene [13] substituted thermosetting material containing a small amount of silicon marketed by Dow Chemical, were side-tracked by the conclusion that the thermal stability above 350°C was questionable, particularly in the presence of small amounts of air. The

demands for thermal stability to 450°C and dimensional stability to at least 425°C effectively eliminated many other organic polymers from consideration. T_g values in this range for organic polymers are relatively rare and dimensional stability usually requires extensive crosslinking. Coordination–addition poly(norbornenes) made a brief appearance as interesting hydrocarbon-like polymers with high T_g values which were cross-linkable through appended substituents [14]. Concerns over thermally stabilities at high temperatures helped to eliminate this interesting class from serious dielectric consideration. The use of copper metallurgy prevents the use of air during curing, a requirement which limits number of cross-linking schemes. The list of viable organic candidates rapidly narrowed to the structural classes of polyarylene ethers, polyarylenes, and polybenzoxazoles and a number of products appeared utilizing such structures.

Cross-linkable versions were offered by Allied Signal/Honeywell (Flare™) [15] and Air Products/Schumacher (Velox™) [16] with dielectric constants ranging from 2.6 to 3.0 for the dense films. For various reasons based on integration difficulties, the polyarylene ethers faded rapidly from the low-*k* dielectric scene. Similarly, polybenzoxazoles were considered briefly as organic polymer dielectrics since they have high thermal stability, adhere well to most caps, hardmasks and metallurgy, show good electrical properties, have low water uptake and have dielectric constants in the 2.7 range for dense materials [17]. In spite of the characterization and integration efforts by Infineon, these materials also seem not to have caught on as on-chip low-*k* dielectrics.

Polyarylene materials have been a bit more successful in the on-chip dielectric arena. Dow Chemical generated a series of exceptionally thermally stable polyarylenes, either by polymerization of multifunctional *o*-diethynyl aromatics or by condensation of biscyclopentadienones with polyfuctional aryl acetylenes [18]. These materials are marketed under the trade name of SiLK™. In the latter case, the end groups can be tailored by control of reagent stoichiometries and cross-linking is achieved using reactive end group and unreacted pendant chain substituents. T_g values in excess of 450°C with a dense dielectric constant of 2.65 and excellent thermal stabilities have been reported. For some time, the SiLK™ materials were considered to be the primary competitors to CVD deposited and solution-spun inorganic materials and numerous integration studies have been reported.

Ultimately, however, the semiconductor manufacturers opted to go with inorganic-like materials with which they were more comfortable through their experiences with oxide insulators. Part of the driving force for the selection of inorganic materials over organic polymers for BEOL integration is the generally soft nature of organic polymers and their relatively large coefficients of expansion. In spite of this, SiLK™ has not quite faded from the scene, like the other organic dielectric polymers, and hybrid device structures containing SiLK™ and porous SiLK™ together with organosilicates (dense and porous) are still receiving industry attention [19].

2.2.2 Inorganic polymers

Silicates and organosilicates constitute the bulk of inorganic dielectric materials. They represent a broad class of materials, ranging from its simplest member, orthosilicate, to compositionally more diverse structures including silsesquioxanes, siloxanes, and copolymers thereof. Figure 2.2 illustrates the general structural elements of the various repeat units encountered in silicon-based sol–gel materials.

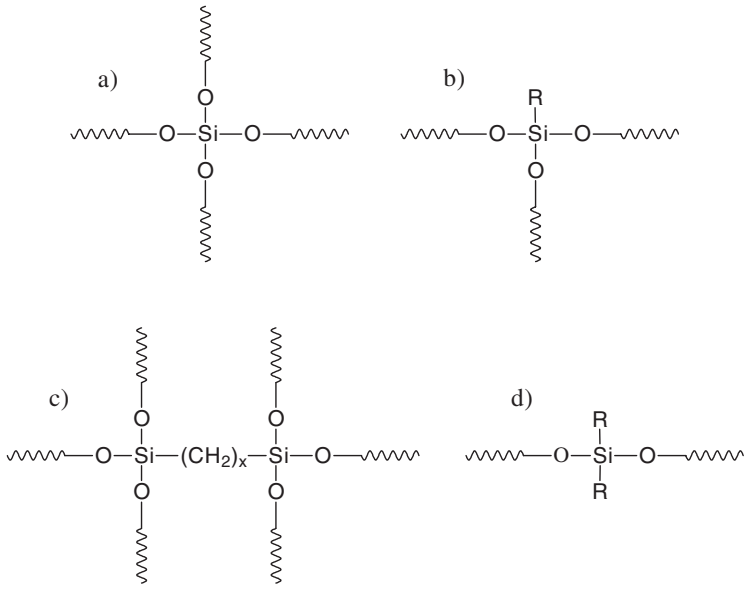

Figure 2.2 Structural repeat units of organosilicate homopolymers and copolymers: (a) orthosilicate; (b) silsequioxane; (c) alkane-bridged silicate; (d) siloxane. R = H, alkyl, aryl, etc.

For repeat units with a functionality greater than 2, randomly crosslinked homo- and copolymers should be obtained. However, this is rarely the case, especially for organosilicates, where silsesquioxanes $(RSiO_{1.5})_n$ comprise the majority of repeat units, (example b in Figure 2.2). Depending on the particular Si-substituent and polymerization conditions, a combination of linear, randomly crosslinked, cyclic, ladder, and cage-like structural units are possible, see Figure 2.3 [20, 21]. Such structural variations may be invoked in explaining observed differences in both mechanical and electrical properties of various organosilicate materials. In part, the use of organosilicate copolymers derived from a combination of various comonomers often helps to randomize the structure. Control of the electrical properties is generally affected by adjusting the C/O ratio of the copolymer by balancing orthosilicate and silsesquioxane structures.

Due to the presence of carbon or hydrogen substituents, organosilicates are more hydrophobic, they have a lower dielectric constant and different etch characteristics relative to SiO_2. Cross-linked organosilicates also have excellent thermal and electrical properties, are unusual among thermosets in that the T_g can be much higher than the curing temperature, and often adhere well to other semiconductor materials. The presence of Si–H bonds (HSSQ) or Si–Me bonds (MSSQ) within the organosilicate network has an important effect on their electrical and mechanical properties (Table 2.2) [22, 23, 24].

Spin-on versions of organosilicate materials are usually prepared by traditional sol–gel processing. This method is generally associated with the preparation of glasses or ceramic materials derived from metal alkoxides based on Si, Al, Ti, Zr, B, P and other transition or alkaline earth metals [25]. However, the majority of sol–gel work relates to silicates due their ready availability and relative stability of the corresponding alkoxides. The sol–gel process dates back 150 years [26, 27], however, it took almost another 100 years, marked

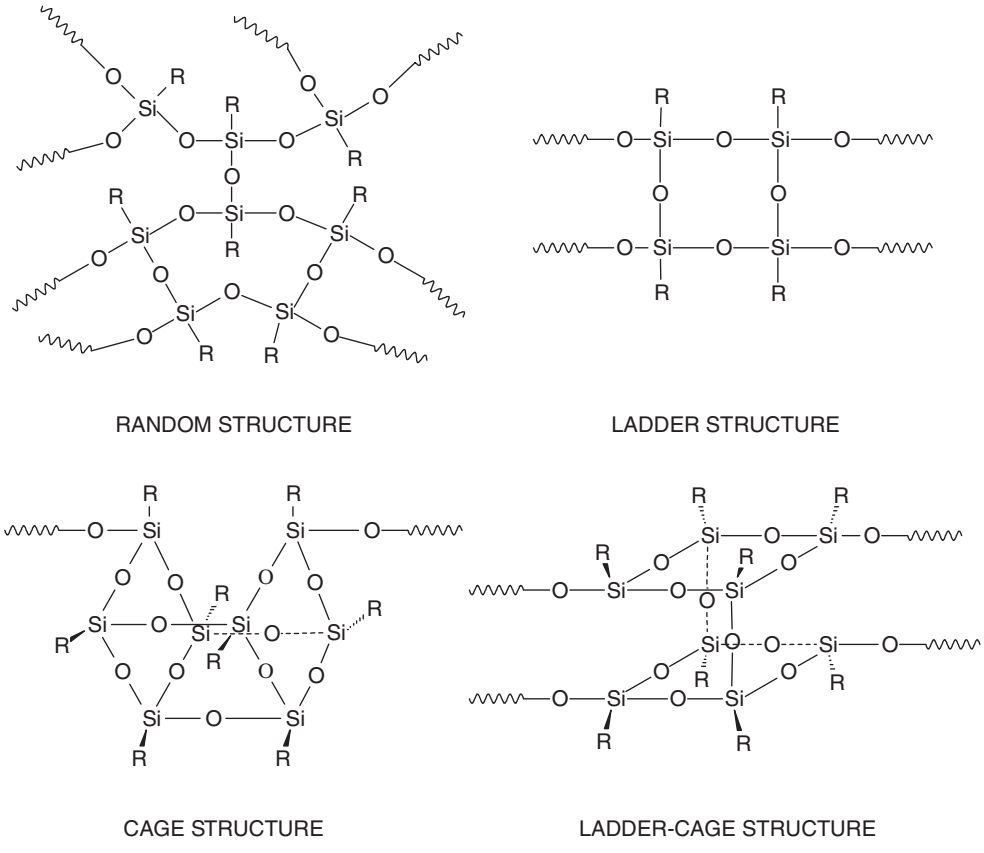

Figure 2.3 Potential structural variations proposed for organosilicate materials

Table 2.2 Effect of Si substituent on properties

Dielectric material	k (1 MHz)	Modulus E (GPa)	Hardness, H (GPa)	Contact angle (°)
SiO_2	4.0	71.7	8	28.5
HSSQ	2.9	13.7	2.2	50.5
MSSQ	2.7	3.6	0.6	97

by the pioneering work of Iler and Stoeber, for silicates to enter the mainstream of chemistry, leading to the commercialization of colloidal silica particles [28, 29]. The motivation for sol–gel processing lies in the higher purity and homogeneity of the final product as well as lower processing temperatures when compared with traditional melt or sintering processes [30]. These features make the sol–gel process and the resulting materials excellent

candidates for solution deposition, i.e., spin coating, dip coating etc., of dielectric insulators. Sols are dispersions of solid, colloidal particles (1–100 nm diameter) in a liquid resulting from the initial hydrolysis and condensation of silica precursors. The sol represents the processable state of these materials. Gels, on the other hand, are interconnected rigid network structures characterized by the lack of tractability and solubility. Thus, silica gels may be produced from the growth of discrete colloidal particles or by the simultaneous hydrolysis and condensation of a suitable precursor, generally an alkoxysilane. The latter approach does not need to exhibit a distinct colloidal stage and condensation is preferably, temporarily arrested while still in the soluble stage. The uniqueness of the sol–gel approach is further characterized by the ability to generate materials of varying porosity, ranging from dense materials to the highly porous xerogels and aerogels, depending on the precise conditions of solvent removal [31]. In order to produce dense films, solvent evaporation has to occur prior to gel formation, i.e., in the soluble state, followed by cross-linking of unreacted, pendant alkoxysilane or silanol groups during the thermal treatment. The dense film approach represents the basis for spin-on deposition of inorganic dielectric materials. More detailed information can be found in reviews and many books published on this matter [32–37].

The classical preparation of these materials by the sol–gel process involves the hydrolysis and polycondensation of alkoxy- and/or halogenated silanes in the presence of water and a suitable catalyst, see Figure 2.4.

The catalyst is typically a mineral acid (HCl, HNO_3, etc.), which promotes the hydrolysis reaction to yield silanols. On the other hand, basic catalysts tend to favor the

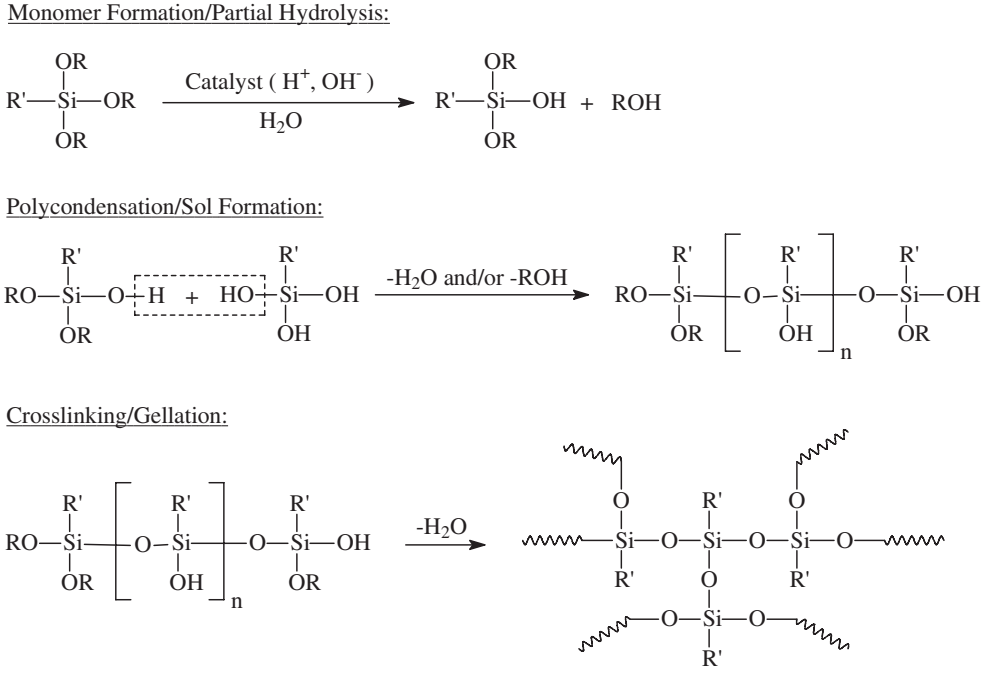

Figure 2.4 Simplified sol–gel reaction scheme. R = H, alkyl; R′ = H, alkyl, aryl, or alkoxy

polycondensation reaction. The silanol functionality readily reacts with itself or an alkoxy/chloro group in a condensation step, which eliminates water or alcohol/HCl. In this fashion, a highly cross-linked network is ultimately formed. The sol–gel approach is a complex process subject to many variables, such as the nature of the catalyst, the amount of water relative to alkoxide groups and reaction temperature. Traditionally, the alkoxysilane derivatives are hydrolyzed and condensed by the addition of acid/water to a solution of the monomers in a polar organic solvent (method 1). However, it has been reported that when the initial hydrolysis of the alkoxysilane is performed solely in the presence of water and acid for 2 h at 5°C, followed by addition of organic solvents and further condensation at elevated temperatures and work-up, mechanically superior coatings consistently resulted upon thermal curing of the hydrolysate at temperatures of 400–450°C (method 2) [38]. Table 2.3 contrasts the modulus, hardness and cracking tendency as studied by nanoindentation measurements for materials prepared by these two methods.

In addition to the differences in mechanical properties, FTIR spectroscopy indicates a significant difference in the 1030 cm^{-1} absorption associated with the Si–O–Si long-chain network structure. Monomer acid hydrolysis by method 1 leads to a much stronger FTIR absorption at 1030 cm^{-1} at the expense of the cage-like structural component at 1170 cm^{-1}. Hence, differences in organosilicate architecture appear to have a profound effect on the mechanical properties.

Other than acids or bases, certain transition metal alkoxides (preferably Zr, Ti) can also act as catalysts without apparently being incorporated into the silicate network [39]. The

Table 2.3 Mechanical properties of organosilicate resins. MSSQ = methylsilsesquioxane, DMS = dimethylsiloxane, BTMSE = bis(trimethoxysilyl)ethane, THF = tetrahydrofuran

Composition/process	M_w	Modulus (GPa)	Hardness (GPa)	Crack resistance
Method 1 (acid hydrolysis in the presence of H_2O and THF, 21°C/30 min)				
MSSQ/(0.67 mL H_2O, 10 mL THF, overnight THF reflux)	8 500	1.95	0.25	Cracked
MSSQ/DMS = 10/1/(3.50 mL H_2O, 20 mL THF, overnight reflux)	4 200	2.03	0.17	Cracked
MSSQ/BTMSE = 10/1/(1.20 mL H_2O, 15 mL THF, overnight reflux)	26 000	3.99	0.62	No cracking
MSSQ/(4.05 mL H_2O, 10 mL THF, overnight reflux)	11 000	2.31	0.32	Cracked
Method 2 (acid hydrolysis in H_2O only @ 5°C/2 h)				
MSSQ/(0.67 mL H_2O, no THF, no reflux)	18 300	4.89	0.76	No cracking
MSSQ/DMS = 10/1/(3.50 mL H_2O, 15 mL THF, 4 h reflux)	6 500	3.41	0.48	No cracking
MSSQ/BTMSE = 10/1/(1.20 mL H_2O, 15 mL THF, 4 h reflux)	9 000	5.52	0.87	No cracking
MSSQ/(4.05 mL H_2O, 10 mL THF, 4 h reflux)	9 100	3.95	0.64	No cracking

addition of β-diketones or β-diketoesters helps to complex the transition metal alkoxide [40]. Metal-alkoxide-catalyzed polymerization of alkoxysilanes is reported to yield organosilicate precursor solutions with excellent shelf life. Corresponding coatings exhibit outstanding uniformity, good adhesion to other interfaces and even lower dielectric constants than similar materials prepared by via acid or base-catalyzed reactions [41].

However, this does not exhaust the possible synthetic routes to organosilicates. Recently, a procedure was reported that also greatly minimizes the formation of cage-like structures in addition to introducing alkane bridges in the silicate network, which are believed to impart mechanical enhancement [42]. The synthetic approach utilizes the well-known hydrosilylation reaction of vinyl or allyl linkages with silanes in the presence of a platinum catalyst. As illustrated in Figure 2.5, this allows for the preparation of linear and cyclic, multifunctional silicates containing alkane bridges.

It is reported that incorporation of the highly functional bridged organosilicates in the amount of approximately 10 mol% with either silsesquioxane and/or orthosilicate linkages yields greatly improved organosilicate coatings. No film properties for the various compositions discussed in the patent are given. In another manifestation [43], similar bridged organosilicates are prepared via Grignard reactions of haloalkylalkoxysilanes [44], (see Figure 2.6).

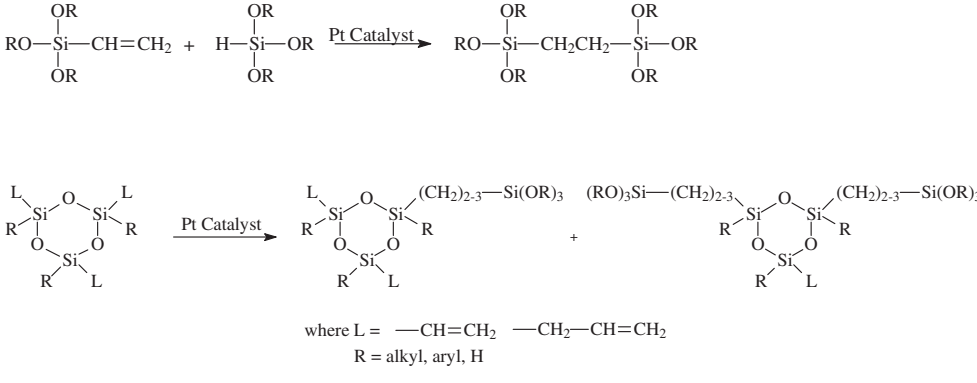

Figure 2.5 Preparative pathway to carbon-bridged silicates using hydrosilylation

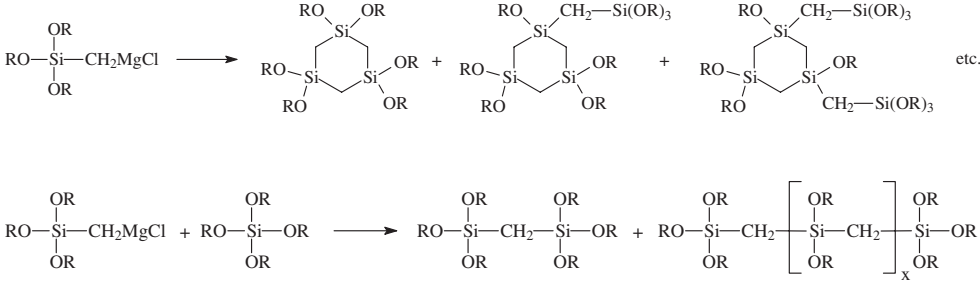

Figure 2.6 Preparative pathway to cyclic and linear carbon-bridged silicates using Grignard reagents

Table 2.4 Properties of organosilicate materials

Composition	M_w	Hardness (GPa)	k (MIS @ 1 MHz)	Crack propagation ($m\,s^{-1}$)
Example 1	11 807	0.62	2.78	2.4×10^{-12}
Example 2	27 716	0.58	2.75	5.3×10^{-12}
Example 3	3 100	1.1	2.83	1.2×10^{-12}
MSSQ	11 000	0.32	2.73	1.3×10^{-9}

Thus, reaction of the Grignard reagent with itself leads to highly functionalized, cyclic silicates, whereas reaction of the Grignard reagent with tri- and tetraalkoxy silanes leads to relatively linear polymers with abundant functionalities along the polymer backbone. Of course, the polymer structure is highly dependent on the stoichiometry of the two reagents, with high concentrations of Grignard reagent favoring branched and ultimately cross-linked polymers. These highly functional derivatives are generally used in conjunction with other organosilicate precursors or precursor hydrolysates. Comparative properties are reported for several organosilicate compositions in Table 2.4. Example 1 consists of the hydrolysis product obtained from the reaction of 1.5 parts of the cyclic carbon-bridged derivatives (Figure 2.5) and 4.6 parts of methyltrimethoxysilane. Example 2, is a composition derived from the reaction of carbon-bridged compound (Figure 2.6) and methyltrimethoxysilane in the ratio of 44 parts/18 parts. Example 3 is similar to Example 1, except that the co-reactants are methyltrimethoxysilane and tetramethoxysilane in the ratio of 9 parts cyclic derivative to 30 parts of methyltrimethoxysilane and 3.4 parts of tetramethoxysilane. For comparative purposes, a hydrolysate of methyltrimethoxysilane prepared under similar conditions was chosen. As shown in Table 2.4, all examples exhibit very similar dielectric constants, however, mechanically the cyclic carbon-bridged/methyltriethoxysilane systems consistently have better properties compared with the MSSQ resin prepared under similar conditions. Hardness values are 2–3 times higher than for MSSQ organosilicates, while crack propagation velocities for 1 μm films decrease by three orders of magnitude.

Integration issues

Organosilicates are generally hard relative to organic polymers, but are often brittle and prone to cracking, characteristics which get worse as the dielectric thickness increases. This is a major reliability issue in a multilayer BEOL build and subsequent packaging. Mechanical characteristics are a major concern because many of the integration processes require good mechanical properties (chemical mechanical polishing (CMP), chip dicing, wire bonding, etc.). In addition to the intrinsic material deficiencies, attempts to integrate low-k organosilicates have uncovered other integration-specific issues. For example, there is damage to the dielectric that occurs during the etching, which degrades electrical performance and must be repaired. Removal of the photoresist, which for SiO_2 insulators involved oxidative plasma treatment, can now cause serious damage to the low-k organosilicate. This is manifested by carbon depletion, formation of polar species, increased water uptake and increases in leakage current and dielectric constant. This is somewhat mitigated by the use

of downstream plasma strips and reducing plasmas (N_2/H_2, He/H_2, NH_3, etc.), but the problem is not eliminated. One repair approach consists of treating the damaged materials with $SCCO_2$ containing dissolved additives in order to restore to some degree the initial electrical and chemical properties [45]. Most commonly employed additives are silylating reagents designed to react with the increased SiOH functionalities produced during processing. Damage is exacerbated with porous materials and repair reagents must not only be tailored for reactivity, but size becomes an important feature as well. One issue is that surface reactivity can be high, but the added functionality can impede the further access of the reagents into the pores. An important observation is that, although the contact angle of the material always rises substantially upon silylation, the electrical properties are not always restored. Careful selection of both the silylation reagents and the process could in principle address not only the damage issues, but also those associated with pore sealing. There are also numerous reports on the use of $SCCO_2$ for cleaning features and removing process residues in integration processes, but these applications will not be discussed in detail here.

Since mechanical properties of organosilicates are a major issue, the search for predictive metrics has been intensive. Many mechanical quantities could be relevant here, including fracture toughness K_{1c}, driving force for cracking G, cohesive fracture energy G_c, film stress, elastic modulus, etc [46]. Of these, film stress and modulus are the easiest to measure. While fracture toughness, fracture energies and driving force for cracking are somewhat difficult to measure, usually requiring techniques such as four-point bending, double cantilever beam (DCB) procedures, modified edge lift-off (m-ELT), crack growth during nanoindentation, etc., the film modulus can easily be measured by nanoindentation [47] or surface acoustic wave spectroscopy (SAWS) [48]. Nanoindentation, however, is subject to substrate effects in thin films and often depends on indentation depth. SAWS values are always less than those measured by nanoindentation, sometimes substantially so [49]. For silsesquioxane materials the ratio of modulii determined by nanoindentation to those measured by SAWS was as large as 1.5–2.0 in our hands. The ratio, however, is not constant and depends on the chemical structure. Nanoindentation techniques have also been utilized to measure other thin film mechanical properties such as toughness and adhesion [50]. Intrinsic film stress is another critical thin film property and one, which can be related to the rate of initiated crack growth (Figure 2.7).

A number of techniques, including wafer curvature procedures [51] can be used to measure film stress. The real question is whether these easily measurable quantities

$$\ln V = b_1 + b_2\left(\frac{h}{E}\right)$$

$$b_1 = \ln(V_0)$$

$$b_2 = \frac{Z\pi\sigma^2}{4nkT}$$

V_0 = material constant related to kinetic and thermodynamic driving force of fracture = 1.45 x 10^{-17} m sec^{-1}
h = thickness
E = film modulus
b_1 = -38.8 m sec^{-1}
b_2 = 5.58 x 10^{16} N m^{-3} assuming s is constant
k = Boltzman constant
Z = channel crack elastic constant factor
σ = film stress
T = temperature

Figure 2.7 Crack velocities for organosilicates under conditions of high humidity [54]

(modulus, hardness, film stress) have any predictive power. In the case of blanket CMP, studies have shown a correlation between the modulus and the tendency to delaminate. In a study of many organosilicate samples at SEMATECH, the data suggest that a modulus of >4 GPa was sufficient to survive CMP [52]. Cracking issues in organosilicates are typically studied by measuring the crack growth velocity from a defect, often in the presence of water (liquid or high humidity) as a stress corrosive agent for organosilicates [53]. Crack growth rates of $<10^{-10}$ m s^{-1} in water are considered a good indicator of integration reliability. The driving force for fracture may be defined as the strain-energy-relief rate G, which is defined in Figure 2.8.

Recently Tsui *et al*. have studied the rate of crack growth in high humidity (~40%) as a function of G, which in turn is inversely related to the elastic modulus [54]. Figure 2.9(a) shows the measurement of crack growth rates for a series of 3-μm-thick dielectric films, each with similar film stress. Figure 2.9(b) presents a calculated plot of crack growth rate for a series of 3-μm-thick films with a fixed modulus of 10 GPa as a function of film stress. The data show that crack growth is affected both by modulus and film stress (the latter appears as a quadratic function). For these reasons, among the dielectric community, the important, easily measurable predictive parameters related to fracture in organosilicates are modulus, film stress and the rate of crack growth particularly under high humidity conditions.

$$G = \frac{Z\pi\sigma^2 h}{2E}$$

$$G = \frac{(K_{1c})^2}{E}$$

σ = film stress
h = thickness
E = film modulus
G = strain energy relief rate in J m^{-2}
Z = channel crack elastic constant factor
K_{1c} = fracture toughness

Figure 2.8 Driving force for fracture as defined by the energy strain relief rate G

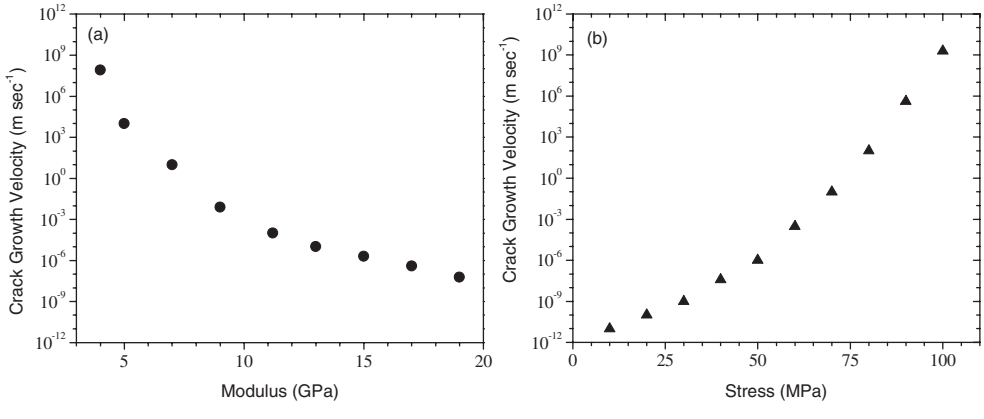

Figure 2.9 (a) crack growth velocity versus modulus (stress is similar); (b) crack growth velocity versus stress (fixed modulus of 10 GPa). Data adapted from Tsui *et al.* [54]

Poor mechanical properties, manifested by cracking, are clearly a problem for organosilicates, regardless of the mode of deposition. A number of approaches could be envisioned for improving this situation. A high surface area, strengthening additive such as silica nanoparticles could be added to improve the mechanical properties. The particles must be small in order to be compatible with the integration process. However, unless the particles themselves are porous, the addition of silica particles will raise the dielectric constant of the cured films [55]. A second approach is the application of a post-curing treatment in order to toughen the material. Initially, e-beam curing was considered. Although the mechanical properties could be improved significantly by e-beam treatment [56], this approach has been largely abandoned because of damage concerns for the front-end devices. This procedure has been replaced by photothermal treatment (350–400°C) of the dielectric material using short-wavelength UV light, to facilitate the silicon–oxygen reorganization [57]. By controlling the dose and temperature, increases in film modulii ranging from 50 to 100% with relatively small increases in dielectric constant could be realized. Although impressive results have been achieved, the procedure is not without issues. UV curing requires another processing step and one in which the dielectric wafers are exposed serially for a period of 4–10 min, depending on the source intensity and wavelength distribution. Generating a uniform exposure over an entire 300 mm wafer is challenging and thicker films are often subjected to inhomogeneous exposure because of the significant film optical densities. The latter is particularly troublesome when the UV curing is also be used to accelerate porogen removal to generate porous films. Finally, there is the danger of causing undesired changes in other absorbing layers within the dielectric stack. An ancillary benefit of UV treatment is that it can facilitate the removal of porogen, particularly when it is chemically bound to the matrix. Another approach toward improving mechanical properties is to alter the structure of the polymerizing monomers to produce a cross-linked film (see page 64). While this may be a viable approach for spin-on materials where the bonding integrity of the monomers is maintained in the polymer, it is questionable for PECVD processes where considerable bond breaking and atom redistribution occurs in the high-energy plasma.

Unfortunately, all the integration issues encountered for dense spin-on organosilicates are exacerbated when porosity is introduced, making the integration of ultra low-k materials an even more difficult challenge.

2.3 SPIN-ON POROUS MATERIALS

The introduction of porosity in organic and ceramic materials is ubiquitous throughout the literature as the only viable method to obtain ultra low-k materials ($k < 2.2$). A distinguishing feature here is that the porosity for dielectric applications must be nano-sized, should be evenly distributed, must be produced under typical integration conditions and must be generated in thin films (often substantially less than 1 μm). Porosity in thin films may be characterized by the porous volume, morphology, long-range order, pore size, shape and pore distribution. By definition, micropores are smaller than 2 nm, while mesopores range in size from 2 to 50 nm. A rule of thumb for integration of porous materials is that the pore size should not exceed 10% of the minimum device feature size. In addition, the porosity may be classified as interconnecting or non-interconnecting [11, 58]. It is generally assumed that isolated pores are more compatible with integration demands, but this is hard to achieve at void volumes above 25%. The relationship between dielectric constant and void volume

is not linear and is modeled by a number of effective media theoretical treatments [59]. The methods of generation of porosity in thin films fall into two general categories; those which utilize sacrificial pore generators (porogens) and those that don't.

2.3.1 Porogen-free systems

Routes to nanoporosity without porogens include: (i) incorporation of polymer free volume generated by large poorly packing substituents; (ii) supercritical fluids which dissolve in and plasticize films so that nucleation sites are generated upon release of the pressure at elevated temperatures; (iii) interstitial volume generated *in situ* by gel morphology; (iv) interstitial voids created from packing of dense or porous surface functionalized shape-persistent inorganic particles. Under normal circumstances polymer free volumes are small (<10%) and hence have a limited effect on the dielectric constant. Recently however, organic polymers with large, nonpacking substituents have been incorporated into organic polymer to generate dielectric constants below 2.5 without fluorine substituents [60]. Regarding route (ii), nanoporous high-temperature polymers (e.g. polyimides) with dielectric constants as low as 1.8 and pore sizes in the 20–50 nm range have been generated using elevated temperatures and supercritial CO_2($SCCO_2$) [61]. The problem here is that this route has yet to be demonstrated for thin films with thicknesses less than 2 μm which is typical of most on-chip dielectric layers. Route (iii) is based on the observation that sol–gel preparation by either acid or base catalysis can also have a significant effect on the morphology of the final gel [62]. Thus, drying of acid-catalyzed gels, where condensation rates are low compared with the rate of solvent removal, leads to high-density, low-pore-volume gels. In contrast, desiccation of base-catalyzed gels, where condensation rates are high compared with the rate of solvent removal, yields clustered structures with an inherently lower density due to the interstitial volume associated with the globular structure, see Figure 2.10.

In fact, this difference in gel morphology and resulting fully cured material has been utilized to prepare organosilicate materials, which are inherently porous and display significantly lower dielectric constants [63, 64]. These patents disclose the copolymerization of organosilicates, including dimethylsiloxanes and alkylene bridged silicates, with orthosilicate using highly basic catalysts. Typical basic catalysts are tetralkylammonium hydroxides, alicyclic amines (piperazine, diazabicycloundecene) and KOH, which are utilized in amounts varying from 0.01 to 0.5 mol per total mol alkoxy groups. The best properties are obtained when 5–75 wt.% of all alkoxy groups have been hydrolyzed and condensed. The resulting hydrolysate/condensate, however, is not particulate. After hydrolysis/condensation, the pH of the reaction mixture is adjusted to <7 by (a) adding a pH regulator, i.e., organic acids; (b) distilling off the basic catalyst; (c) sparging the base from the reaction mixture with nitrogen or argon; (d) removal by ion-exchange treatment; (e) extraction/washing procedures. Reaction of 1 mol methyltrimethoxysilane (MTMS) and 1 mol tetraethoxysilane (TEOS) in the presence of water/ethanol and base for 2 h at 55°C, followed by addition of propylene glycol monopropyl ether, concentration of the reaction mixture and pH adjustment with acetic acid, yielded copolymers with surprisingly low dielectric constants as shown in Table 2.5. These dielectric constant values are considerably lower than the expected composite dielectric constant of 3.35 calculated (assuming a linear relationship) for equal mole fractions of methylsilsesquioxane MSSQ (k = 2.7) and TEOS (k = 4.0).

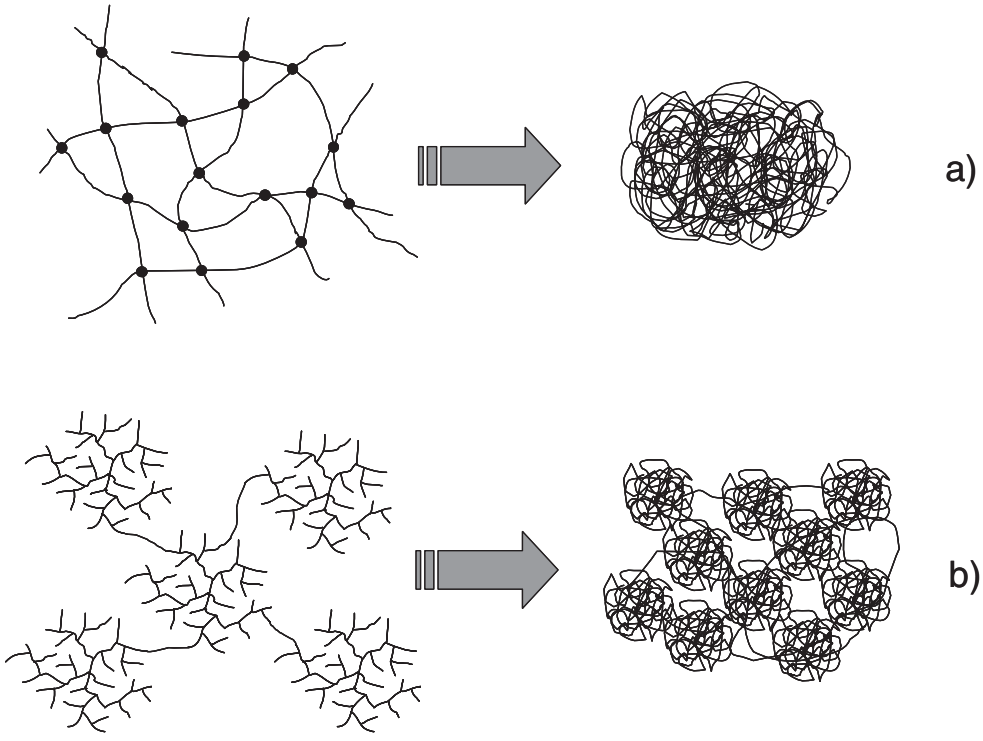

Figure 2.10 Schematic representation of densified gels derived from: (a) acid-catalyzed sol–gel process; (b) base-catalyzed sol–gel process

Table 2.5 Dielectric constants of a MSSQ/TEOS = 1/1 organosilicate obtained using different basic catalysts

Catalyst	*k*
Tetramethylammonium hydroxide	2.27
Piperazine	2.29
Diazabicycloundecene (DBU)	2.14
NaOH	2.16

The interstitial volume generated by packing of silica or organosilicate particles is another method of creating porosity, which has been exploited with the goal of making low-*k* dielectric films. However, within the confines of calcination temperatures well below 500°C and particle sizes commensurate with microelectronic device dimensions, the controlled sintering of fine particles is considerably more difficult than anticipated. In its simplest manifestation, small silica particles, suspended in an organic solvent, are formulated with a low-molecular-weight organosilicate binder and cured to generate a porous silica/organosilicate hybrid. Careful control has to be exercised in order to balance the porosity

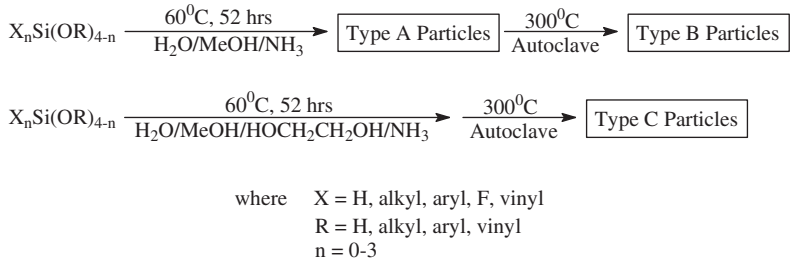

Figure 2.11 Synthetic scheme for the preparation of amorphous silica particles

generated by the interstitial volume derived from particle packing with the amount of binder used to glue the particles together to avoid complete filling of the interstitial space. In addition, the relatively high dielectric constant of silica particles ($k = 4.0$) and their hygroscopic nature, limit the overall utility of this approach. Nevertheless, mechanical properties can be improved by this approach [55]. In 2003, a report by Fujitsu appeared, which mentioned the use of a low-k dielectric material based on nanoclustering silica (NCS) characterized by a pore size <4.5 nm and a k value of 2.25 [65]. Furthermore, a modulus of 10 GPa along with good electrical properties (leakage current $<4.76 \times 10^{-11}$ A cm^{-2} at 0.2 MV cm^{-1}) generated a lot of interest. Upon closer examination of the report, it appears that this dielectric insulator is based on materials developed by Catalysts & Chemicals Industries Company (CCIC). In a series of patents [66–69], dielectric materials are described, which utilize fine silica particles derived from the basic hydrolysis of an alkoxysilane as shown in Figure 2.11.

Depending on the general reaction conditions, three types of silica particles can be prepared. After the initial slow addition of the alkoxysilane to the aqueous basic alcoholic solution, and heating, the particles are purified by ultrafiltration and ion-exchange resin treatment (type A particles). Generally, the purified particle suspension, type A, is further treated by heating in an autoclave at temperatures of 200–300°C, producing type B particles. The hydrothermal treatment causes densification of the particles and approximately 10–15% shrinkage in the particle diameter. Furthermore, if a portion of the methanol is replace by ethylene glycol, then porous type C particles are produced. Particle diameters of 20–40 nm are typical for this type of synthetic scheme. It should be noted, that since no surfactant or other structure-directing agent is present during the particles synthesis, the resulting silicates should be amorphous, although this is not specifically noted in the patents.

As a rule, formulations based solely on silica particles yield poor coatings. Therefore, the particles are generally combined with a binder, most commonly produced by the acid hydrolysis reaction of alkoxy and/or halogenated silanes. To optimize adhesion between the particles and the binder, the formulations may be heated at 50°C for 1 h or so. Table 2.6 illustrates several compositions prepared from various particle types using a binder based on hydrogen silsesquioxane (HSSQ) derived from the acid hydrolysis of triethoxysilane.

Closer examination of the reported experimental data reveals that type A particles give rise to coatings which exhibit a marked increase in the dielectric constant upon prolonged exposure to ambient conditions, whereas type B particles show only slight changes upon similar exposure. The increase in the dielectric constant upon atmospheric aging is often a

Table 2.6 Dielectric constant of coatings prepared from SiO_2 particles and a binder based on low-molecular-weight HSSQ; k_1 was measured immediately after cure and k_2 was measured after one week under ambient conditions

Silica particles (X)	Hydrolyzate (Y)	Weight ratio (X/Y)	k_1	k_2
Type A	HSSQ	80/20	2.8	4.1
Type B	HSSQ	80/20	2.4	2.5
Type B	HSSQ	95/5	2.3	2.4
Type C	HSSQ	70/30	2.6	2.8

direct result of the hydrophilic nature of the coating and reflects the absorption of moisture. It is not surprising that type A particles, treated at only 60°C, would exhibit a significantly higher concentration of surface silanol groups due to incomplete reaction, compared with the type B particles prepared hydrothermally at 300°C. Another important observation can be made when comparing type B particles formulated with different amounts of HSSQ binder. The composition incorporating only 5 wt.% HSSQ exhibits a lower dielectric constant than the composition based on 20 wt.% HSSQ binder. Presumably, more binder results in partially filling the interstitial porosity, increasing the dielectric constant. A dielectric constant of 2.6 measured for the porous type C particles, could also be explained in this fashion. Unfortunately, this formulation was prepared with a much higher binder concentration, making a direct comparison of dense versus porous particles impossible.

Further refinements of this basic system are possible by increasing the intimacy of particles and binder. This can be accomplished by modifying the surface of the particles using a phenyl trialkoxy silane or phenyl trichlorosilane under basic conditions at approximately 50°C for 15 h [70]. The mixing ratio, in terms of SiO_2, of the phenylalkoxysilane to silica particles is generally 0.01–0.3 parts by weight, preferably 0.05–0.2 parts by weight. This yields particles, which are at least partially covered with phenyl groups, see Figure 2.12.

These modified particles are then used in conjunction with a binder derived from the reaction of an alkoxysilane/halogenated silane hydrolysate with a poly(silazane). The reaction product is referred to as a polysiloxazane. In effect, the polysilazane acts as a coupling agent to any silanol containing component, i.e., polysiloxane hydrolysate and modified silica particles, including any surface silanols present on the substrate surface. It is claimed that mechanical properties, crack resistance and adhesion are improved by this approach.

2.3.2 Porogen-containing systems

Several examples of porous organic polymers where the porosity was generated by sacrificial porogens have been described. Nanoporous polyimides generated from block copolymers containing the porogen as a labile block have been reported [71]. In these cases, however, the pore stability was inadequate when cycled to temperatures >400°C. Fluorine-containing materials met resistance because of early observations with fluorinated polyimides. These observations suggested that at high temperatures fluorinated substitutents caused

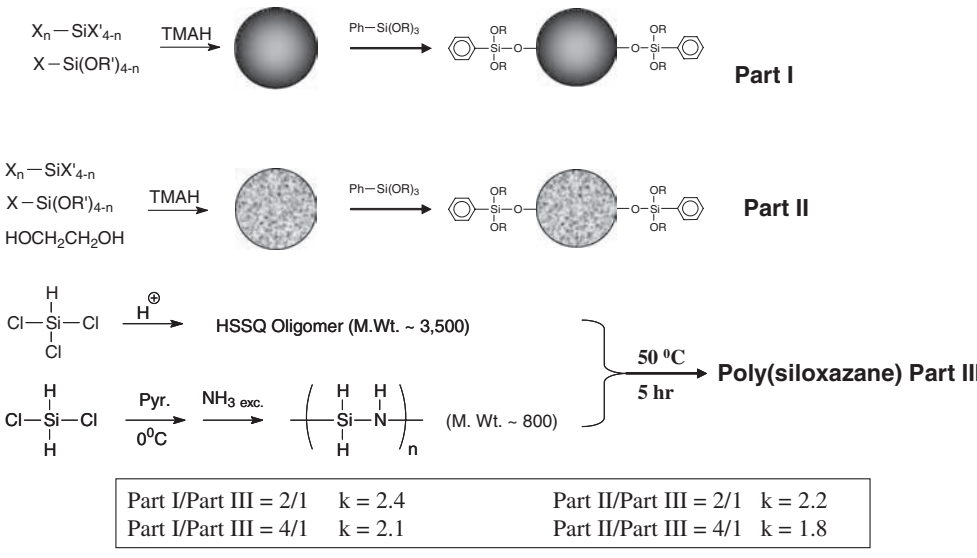

Figure 2.12 Phenylsilsesquioxane surface modified silica particles. Part I = dense, amorphous SiO_2 particles; Part II = porous, amorphous SiO_2 particles; Part III = polymeric particle binder resin

delamination of the metal liners, presumably due to the formation of volatile metal fluorides. The Air Products/Schumacher polyarylene ether Velox™ materials could also be made nanoporous using a solvent-induced phase separation scheme and dielectric constants around 2.0 were reported, although the pore sizes were in the range of 20 nm and the size distribution changed throughout the film [72]. Porous versions of the poly(arylene) thermoset SiLK™ from Dow Chemical have been prepared using sacrificial polymeric porogens and dielectric constants down to 2.3 with pore sizes of only a few nanometers have been described. These materials seem to be the best of the porous organic polymer class, but implementation has been hindered by industry reluctance to accept organic polymeric dielectrics [73].

On the other hand porous spin-on dielectrics with an inorganic backbone are still considered as potential candidates for ultra low-*k* applications. These materials can be classified into three categories: amorphous, semicrystalline and crystalline. The common feature for all these materials is the formation of a silica or organosilicate three-dimensional porous network through the hydrolysis and polycondensation of reactive silicon precursors (for instance alkoxysilanes), in the presence of a porogen. Here, the term 'porogen' refers to solvents, small organic molecules, oligomers and polymers, which after removal lead to the formation of pores. When solvent is used as a porogen, the silicate network needs to be rigidified enough before solvent removal in order to create porosity. Based on the technique used for drying, a distinction between aerogels and xerogels, both amorphous solids, can be made. Xerogels are formed through conventional drying by evaporation, while in the case of aerogels, supercritical drying is the method of choice. When small organic molecules or polymers constitute the pore generator, the porous volume and pore size distribution are governed by a phase separation process occurring before or during the thermal treatment of the resin, supporting two different mechanisms: nucleation and growth (N&G) or

templating. Finally, the materials are considered to be semicrystalline when pore organization is obtained, and crystalline if they are synthesized via typical hydrothermal crystallization methods.

Amorphous porous spin-on silicates and organosilicates

The formation of a more or less rigid skeleton structure before extraction of the liquid from a wet gel is of tremendous importance in the formation of highly porous materials. Even if the gelling point is reached after spin-coating of the sol, the hydrolysis and polycondensation is still incomplete. An additional aging step is then required to promote sol–gel condensations, resulting in the strengthening of the network structure. At this stage, solvent can be safely extracted without collapse of the network backbone. The level of residual porosity is consequently tuned through the ratio of solvent to solid content in the initial sol.

Aerogels

Aerogels are sol–gel-derived materials, invented in the United-States in the 1930s by Samuel Kistler [74], who recognized that removing the pore fluid from wet gels without establishing capillary forces would create an air-filled, ultraporous solid containing the full free volume of the wet gel. Different drying methods have been developed (supercritical, freeze-drying, ambient-pressure) which minimize capillary forces and conserve the pore structure of the wet gels (minimum shrinkage) [75]. The resulting materials after drying have extremely low densities (up to 95% of their volume is air), large open pores, and a high inner surface area, resulting in materials with ultralow dielectric constants as reported by Hrubesh in 1993 [76]. In this study, dielectric constants of bulk materials: a silica aerogel and two organic aerogels (resorcinol–formaldehyde and melamine–formaldehyde) were found to vary linearly between values of 1.0 and 2.0 for aerogel densities ranging from 10 to 500 $kg\,m^{-3}$. Nevertheless, the dielectric properties of these aerogels are significantly affected by the adsorbed water internal to the bulk material. Later, the same author tuned the special conditions of existing coating methodologies, for instance spin-coating, in order to prepare thin aerogel films, thus making these materials compatible with microelectronic processes [77]. The method is essentially the same as that used to spin-coat glass coatings for electronic applications, except that the spinning apparatus is maintained in a closed atmosphere entirely saturated with a solvent. Typically, the gel forms in few minutes after deposition, the substrate is then manually transferred to a solvent bath prior to supercritical drying. Following this procedure, a 3.4 µm silica aerogel film with a dielectric constant of 1.79 (78% porosity) was obtained.

Because of the number of residual silanols present after supercritical drying (as-synthesized aerogel), water is adsorbed inside the pores, resulting in an increase of the dielectric constant and of the leakage current density [78]. A subsequent thermal treatment at 450°C can be applied that reduces the amount of hydrophilic groups. A relatively lower dielectric constant ($k = 2.0$) and leakage current density ($J = 10^{-7}\,A\,cm^{-2}$) were obtained compared with the as-synthesized material ($k = 2.1$, $J = 10^{-6}\,A\,cm^{-2}$) [79]. A similar effect is observed via silylation using trimethylchlorosilane (TMCS) [80]. Here a 12% of reduction

in dielectric constant and almost two orders of magnitude improvement in leakage current were obtained after capping of Si–OH groups with $SiMe_3$.

Most of the aerogels reported in the literature are synthesized from tetraalkoxysilane precursors, resulting in materials exclusively composed of silica. Inspired by the integration of fluorinated silica glass (FSG) in manufacturing processes, Roepsch has prepared fluorine-doped aerogels [81]. Triethoxyfluorosilane (TEFS) was used in this case as the precursor for the preparation of aerogel samples. Although fluorine was partially retained in the structure of the aerogel due to hydrolysis of the Si–F bond, bulk materials having ultralow dielectric constant ranging from 1.13 to 1.19 were obtained.

While supercritical drying has been employed successfully for the synthesis of ultralow-k aerogels, this approach is of concern to semiconductor manufacturers for various reasons. In terms of materials properties, aerogels have big pores (10–20 nm), extremely poor mechanical properties and are highly hydrophilic if an additional silylation step isn't performed. From a processing point of view, several delicate steps are involved: control of the spin-coating atmosphere, transfer to a solvent bath for aging and supercritical drying at high pressure, which make this process not easily adaptable to continuous thin film forming operations. Not only would integration issues have to be solved, but the overall production cost is also predicted to be higher. On the other hand, ambient drying appears to be an alternate processing method that would mitigate some of the issues described above. Materials synthesized following this approach are called xerogels.

Xerogels

Silica sols used for the synthesis of xerogel films are preferentially prepared following a two-step acid/base catalyst procedure [37, 82, 83]. In the first step, TEOS, ethanol, water and HCl are mixed in a precise molar ratio and the solution is aged. In the second step, a basic catalyst is added to the above solution and gelation is observed within 5–60 min, depending upon the sol–gel conditions. Spin-coating of the above solution (before gelation) is normally performed under an ethanol atmosphere to prevent premature drying of the film. The spun film is kept for few minutes under the same atmosphere and can be aged in an alcoholic solution to ensure densification of the silica network so it can withstand the capillary forces generated during drying. Immersion of the film in a nonpolar solvent, e.g., n-hexane allows the replacement of ethanol and consecutive surface modification with a capping agent (hexamethyldisilazane (HMDS), trimethylchlorosilane (TMCS)). Capping-off of reactive terminal hydroxyl groups is of tremendous importance in the ambient drying process because it makes the drying shrinkage reversible (springback effect) [84, 85]. Indeed, organosilyl-terminated surfaces do not participate in condensation reaction or hydrogen bonding, as the gel is collapsed by the capillary tension developed during drying, therefore the shrunken network elastically springs back to its original porous state. While this strategy is the most commonly used for xerogel films synthesis, there has been a single report of a highly porous xerogel film (79.5% porous, $k = 2.0$) obtained by an ambient drying process (2 days aging in n-heptane and curing at 270°C) without surface modification [86].

In general, silylation of xerogel films is important to maintain a high porous volume and is also beneficial for the dielectric constant through removal of polar Si–OH groups. As an example, when the same sol is used to prepare two xerogel films: the unmodified film consists of very small particles (<10 nm), has a porous volume of 15% and a dielectric

constant of 3.95, while the corresponding modified film is composed of coarse (~40 nm) particles and pores, is 47.5% porous and presents a dielectric constant of 2.45 [87]. Interestingly, if silylation is necessary to obtain highly porous materials, too much surface modification results in lower porosities and higher dielectric constants as the pores get filled with organic moieties [88]. It is also worth noting that trimethylsiloxy groups are stable up to 450°C under an inert atmosphere, but they start decomposing at higher temperatures [89]. Since most of the processes in the semiconductor industry take place at temperatures ≤450°C, the thermal stability of the organic moiety of surface modified xerogel films shouldn't present an issue. Silylation of xerogels is often coupled with a thermal anneal in forming gas to further increase the hydrophobicity of the films. This additional processing step significantly reduces the leakage current density from 3.21×10^{-5} A cm^{-2} (before anneal) to $6–8 \times 10^{-6}$ A cm^{-2} (after anneal) [90].

The properties of xerogel films depend on the pH of the catalysis step, the reactant concentration, the type of solvents used, and the spinning, curing, aging, surface modification, and drying conditions. For example, the longer a gel is allowed to age, the more of its original porosity it retains upon drying and the lower its dielectric constant [88]. The aging time also affects the fracture toughness of xerogel films and it has been shown that there may be an optimal aging time and temperature for maximum fracture toughness [91]. However, close to their gel point, xerogel solutions become non-Newtonian, affecting the porosity and uniformity of the film [92]. Optimization of the sol–gel conditions and control of the amount of solvent evaporation during spin-coating, are therefore required to obtain uniform xerogel films with dielectric constants lower than 2. Because control of the solvent evaporation is not always easy, another approach has been developed where a nonvolatile co-solvent (ethylene glycol) is added to the sol, allowing spin-coating in an open, ambient atmosphere [93]. Compared with the controlled evaporation process, porosity is now determined by the ethylene glycol/TEOS volume ratio. In this case, a narrower pore size distribution is obtained compared with the film made with only ethanol as a solvent, resulting in higher thermal conductivity [94], hardness and modulus (at constant porosity) [95]. A power law dependence of the Young's modulus as a function of the porosity (25–75%) has been found, suggesting that the xerogel structure can be modeled as open-cell foams [95].

Xerogels films can also be synthesized starting from TEFS (triethoxyfluorosilane) instead of TEOS as the silicon precursor. Previous studies have shown that fluorine distorts Si–O rings and increases silica tetrahedral framework formation, limiting the lattice polarizability and thus decreasing the dielectric constant. Fluorinated silica xerogel films exhibit low dielectric constants (2.1 as processed and 2.3 after heat treating at 450°C in air) and good mechanical properties ($E = 12$ GPa, $H = 1$ GPa) [96]. The increase in dielectric constant after annealing is likely associated with the loss of fluorine at high temperatures. Microstructural characterization of TEFS xerogels reveals a 'coral reef' morphology, different from the one usually observed for TEOS or TMOS tetramethylorthosilicate xerogels. Typically, silica gels have very separated features with only a small amount of material forming links, whereas TEFS gels show larger diameter links which also define the pore structures. It has been suggested that the presence of thickened links are responsible for the improved mechanical properties: over twice the elastic moduli of comparably porous xerogel films [97].

While low dielectric constants can be obtained in the case of aerogels and xerogels, control of the pore size is difficult to achieve and the processing conditions are not always compatible with mainstream manufacturing. To solve these issues, new routes involving the

use of small molecules, oligomers or polymers as sacrificial porogens have been recently developed.

Nucleation and growth/templating

The most common approach to the generation of porous organosilicates is the sacrificial porogen route. This strategy is effective for both spin-on and PECVD processes, although the porogen is more difficult to remove from the latter films as they are usually chemically incorporated into the highly cross-linked matrix. A number of reviews on porogen-based routes to nanoporous thin films have appeared [98]. With this procedure, a low-molecular-weight thermosetting polymer such as a soluble silsesquioxane is dissolved in a suitable solvent and a sacrificial pore generator (porogen) is added to the solution. The sample is dispensed onto a substrate and the film heated to remove most of the spinning solvent. The film is then heated either directly or in stages to a final temperature of 425–450°C to complete the resin cure and decompose the porogen into small fragments which diffuse through the matrix, leaving pores behind. Porogen materials may be small molecules such as cyclodextrins or calexaranes, they could be oligomers or they can be polymers. There are a number of things that have to happen for this conceptually simple procedure to work effectively. First, the porogen and the matrix must either be soluble in the solvent or compatibilized in the media to form an optically transparent solution and film after spinning. Second, the resin must stiffen substantially before the porogen decomposes so that the matrix will resist the capillary forces trying to collapse the pore during porogen decomposition, as shown in Figure 2.13.

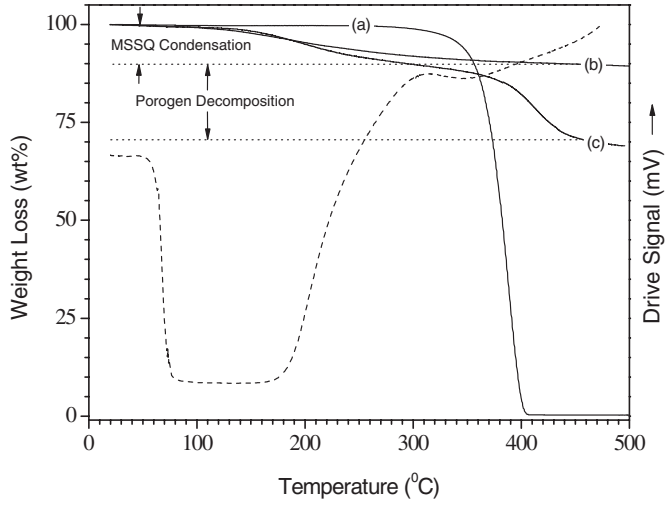

Figure 2.13 Thermogravimetric analysis study of: (a) multi-arm organic porogen; (b) MSSQ homopolymer; (c) MSSQ/porogen = 80/20 hybrid upon heating. Dashed line, dynamic mechanical analysis of neat MSSQ; drive signal represents the change in film stiffness of the material upon heating over the same temperature range and the same heating rate compared with the TGA

Figure 2.13 shows clearly that vitrification of the resin begins at elevated temperatures after the resin softens at the *T*g. The temperature at which the modulus increases due to vitrification is lower than the decomposition temperature of the porogen. Finally, the pores must be nanoscopic in size and survive the final cure and integration processing temperatures.

In such a blending approach, the formation of pores may take place either by a N&G process or by templating. Each process is quite distinct, can be differentiated by several characterization techniques and will be discussed separately. In N&G, the porogen and the initial resin are miscible in the film prior to significant vitrification (miscible blend). Upon heating, the resin vitrifies and the porogen begins to phase separate because the porogen is less compatible with the vitrified structure. If phase separation does not occur upon vitrification, the pores may be too small and collapse before the resin has reached full strength. On the other hand, if it occurs too soon, the polymer domains may give large or macroscopic pores. The rule of thumb is that if the porous film scatters visible light, the pores are too large for dielectric applications. The N&G process is described by the idealized phase diagram in Figure 2.14. Initially random, nucleation produces small domains. If vitrification has proceeded substantially, they remain small because the media viscosity impedes diffusion and the resulting pores are small. If phase separation occurs very early in the vitrification process, the domains diffuse and become larger, producing larger pores. The point where nucleation begins depends on resin structure, porogen solubility, porogen molecular weight, polydispersivity, loading level, etc., and hence the pore size is variable. The result is a conceptionally simple process which is actually very hard to control.

Different porogens have been auditioned, ranging from small molecules to high-molecular-weight polymers. In the case of small molecules, cyclodextrins (cyclic glycosides) were the molecules of choice because they are composed of a hydrophobic cavity and a hydrophilic perimeter that makes them compatible with the SSQ resin. Initial studies using these materials as porogens led to worm-like pores with diameters of a few nanometers and lengths up to a few tens of nanometers characteristic of porogen supramolecular assembly

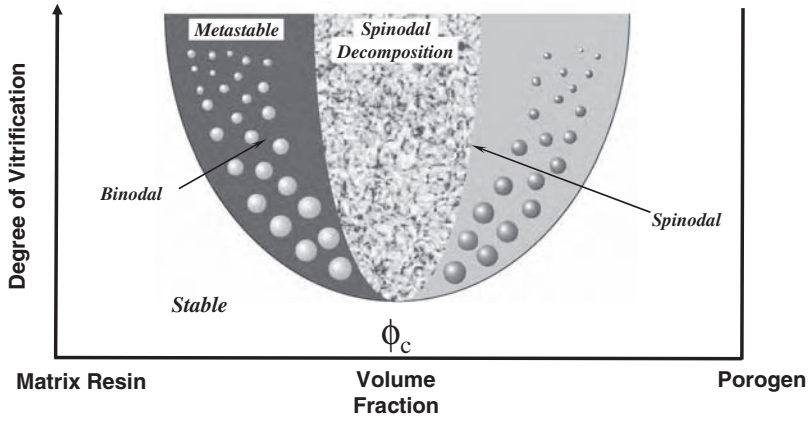

Figure 2.14 Idealized phase diagram of an organosilicate thermosetting matrix containing a thermally labile porogen in nucleation and growth processes. The extent of matrix vitrification is depicted on the vertical axis

[99]. Chemical modification was pursued to mitigate supramolecular stacking and promote compatibility with the organosilicate resins. Methylated β-cyclodextrin has produced films with dielectric constants below 2.0 and pore size <2 nm, but increasing porogen concentrations (>50%) leads to worm-like aggregates [100]. Another issue is that most cyclodextrin CD derivatives do not decompose cleanly and leave a significant char residue. It is not clear what effect this char will have on critical electrical properties such as leakage and breakdown.

For polymeric porogens, polymer–polymer miscibility is somewhat unusual and requires strong enthalpic interaction between the components. These interactions could be dipolar, electrostatic, acid–base, hydrogen bonding, etc. Failing these, the components will very likely macroscopically phase separate. Most of the organosilicate matrix materials employed are derived from silsesquioxanes (SSQ), structurally imperfect materials, often of low molecular weight, containing numerous chain ends such as SiOH, SiOR, etc., resulting from the incomplete hydrolysis and/or condensation of the organosilicate sol–gel precursors [20]. As a result, the matrix polymer is relatively polar with acidic substituents. Conventional wisdom suggests that since most main chain polymer functionality will be weakly interacting, the chain ends are driving the strong polymer–polymer interactions and that low-molecular-weight porogens are more likely to be more miscible than higher molecular weights. Since linear chains have only two polymer ends, the original focus went to multi-arm and highly branched systems. Some of the early porogen studies focused on dendrimers, the quintessential branched polymer with multiple polar ends [101]. Early studies on TEOS-based systems using nitrogeneous dendrimers yielded porous silica, although the pore size did not correlate well with the dendrimer size in solution. Silica-based systems for dielectric applications suffer from the hydrophilicity of the porous matrix coupled with the high k value of the matrix material requiring high porosity levels to achieve low-k dielectric targets. Recent studies by Ree *et al.* [102] used well-defined multi-arm polypropylenimine dedrimers (PEI-32 and PEI-64) with 32 and 64 amino chain ends capped with ethyl acrylate (64 and 128 arms respectively) in a methylsilsesquioxane (MSSQ) matrix to achieve dielectric constants as low as 1.7 at porogen loadings of 40%. Small Angle X-ray Scattering (SAXS) studies showed random porosity, little tendency for the porogen to aggregate and pore sizes <5 nm. As expected for N&G, with the 64 arm porogen the pore sizes increased with loading level and the size distribution broadened. This effect was less obvious with the more compact and spherical 128 arm derivative.

Some early studies from our laboratories utilized polycaprolactone (PCL) polymers prepared by controlled ring-opening polymerization. Since the ester functionality is weakly interacting with SSQ end groups, multi-arm systems were necessary for compatibility. Figure 2.15 shows the effect of porogen architecture in MSSQ.

The Field Effect Scanning Electron Microscope (FE-SEM) pictures show a progressive decrease in pore size as the number of chain ends increase. From these initial studies evolved the focus on multi-arm porogen-based systems. The synthesis capitalized on advances in controlled ring-opening polymerization (ROP) of caprolactone from multi-arm hydroxylated star polymers initiators using a core-out approach where additional branching points could be introduced by incorporating bis-hydroxymethyl propionic acid units (bis-MPA) at defined intervals [103]. This synthetic procedure provided a vast array of porogens with defined molecular weights and molecular architectures including materials with 4, 6, 12, 24, and 48 polymer arms [104]. The PCL–based porogens were thermally stabile to above 250°C, temperatures adequate for sufficient vitrification of the organosilicate matrix to occur prior to the generation of porosity [105]. The synthetic procedure could also be

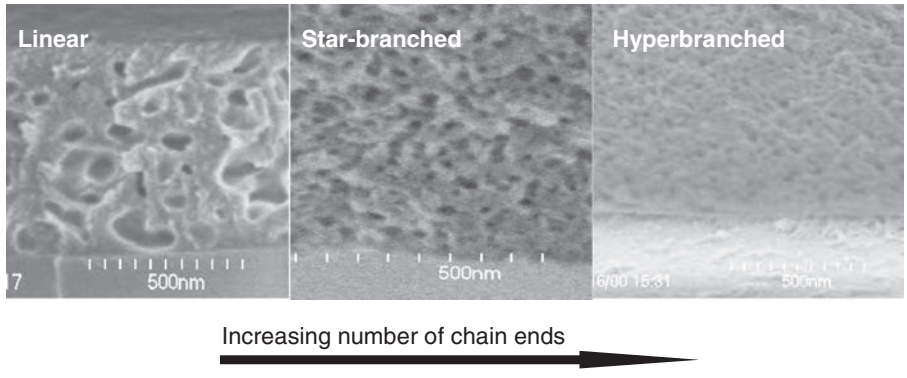

Figure 2.15 FE-SEM snap-fractured cross-sections of organosilicates containing polycaprolactone porogens varying in molecular architecture initially blended into a low-molecular-weight MSSQ resin and processed by heating

expanded to include multi-arm star polymers where the chains were produced via atom transfer radical polymerization (ATRP) [106]. Block copolymers were accessible from the multi-arm initiators by sequential growth including miktoarm systems where controlled blocks could be prepared using successive ring opening polymerization (ROP) and atom transfer radical polymerization (ATRP). The latter could be used to incorporate a range of pedant chain substituents to facilitate control of polymer–polymer interactions. An extensive review of the preparation of star-branched PCL homo- and copolymers is provided by Hedrick *et al*. [104]. Many of these materials were compatible with low-molecular-weight MSSQ resins and produced nanoporous films upon heating with good efficiencies. Dielectric constants of 2.0 or less were achieved at porogen loading levels around 40% with pore sizes in the 12–20 nm range. Although these early studies showed that molecular architecture can matter in N&G processes, the pore sizes are too large for future devices. This is particularly true for block copolymer porogen materials prepared by tandem (consecutive) polymerization routes.

The efficacy of chain branching for promoting polymeric porogen miscibility in polar, low-molecular SSQ resins was demonstrated early and is a critical structural feature in systems where the chain functionality is only weakly interacting. It is not necessary, however, for polymers with strongly interacting chain functionality, although we suggest that chain branching provides increased solubility at high loadings, protects against aggregation and can control the pore shape. Small molecules and linear polymers can be effective porogens if properly functionalized in N&G schemes. The most common backbone polymer functionalities used to promote SSQ miscibility seem to be ethyleneoxy (EO), propyleneoxy (PEO), block copolymers of EO/PEO, polyTHF, etc. Pendant polar substituents such as polyethylene glycols (PEG), hydroxyalkyl and nitrogeneous units such as pyridyl, acrylomidyl, dimethylacrylomidyl, dimethylamino alkyl, ethylene imine, propylene imine and others also facilitate miscibility. Interacting substituents may be incorporated, either in random fashion or as polymer blocks. The latter often lead to self assembly of the porogens. The PEO/EO block copolymers and EO/PEO/EO triblock copolymers are amphiphilic materials and can be effective pore generators when properly purified. In this regard, Yang *et al*. [107] have reported dielectric constants as low as 1.5 using Pluronics® triblock

copolymer surfactant porogens and pore sizes in the 2.7–5 nm range using MSSQ as a matrix host.

The compatibility of many nitrogeneous porogens with SSQ derivatives is not surprising, given their tendency to form strong hydrogen bonds and the acidic nature of the SiOH functionality. Polyoxazolines were some of the earliest porogens exercised in silica formed by hydrolysis of TEOS. Chujo and coworkers [108] suggested, based on IR spectroscopic studies, that the miscibility of the porogen was due to hydrogen bonding between the porogen and the polymerizing silicate. Random vinyl addition copolymers of methyl methacrylate (MMA) and dimethylaminoethyl methacrylate (DMAEMA) have also been studied in some detail [109]. Materials containing at least 25–30% DMAEMA are miscible in low-molecular-weight MSSQ resins over a wide loading range (10–80%) and tend to form high-quality optical coatings which can be rendered porous by heating. Interestingly, the presence of basic substituents on the polymer chain does not destabilize the SSQ resin solutions, whereas the addition of small-molecule bases such as triethanolamine causes rapid gelation. The system is one of classical N&G, as pore size and distribution increase with porogen loading level and molecular weight, as shown in Figure 2.16 [110].

The relatively small pores produced suggest good miscibility with the resin and late phase separation upon curing. Recent studies on the mechanical properties of porous MSSQ materials derived from this porogen suggest that porogen residues can substantially improve the film mechanical properties [111]. The presence of basic substituents also provides some unexpected results. Presumably because of acid–base interactions on silica, Transmission Electron Microscopy (TEM) and Small Angle Neutron Scattering (SANS) studies show that there is an accumulation of porogen at the interface and subsequently a higher pore density at the film–substrate junction [112]. This does not happen for porogens without basic substituents. Block copolymers derived from styrene and 2-vinyl pyridine (P2VP) have also been studied as porogens [113]. The P2VP block could be increased up to 65 mol%. As expected, these materials form excellent, optical-quality films because of strong interactions between the matrix and resin. Pore sizes in MSSQ films were around 12 nm.

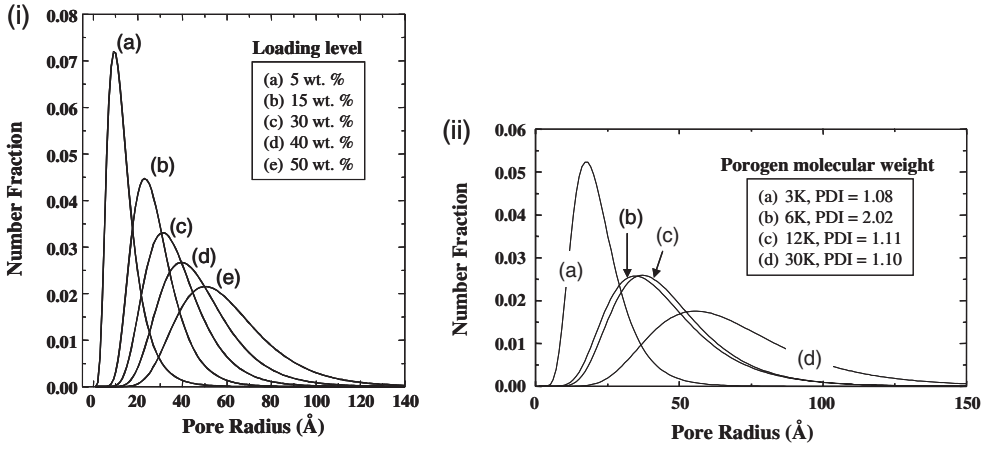

Figure 2.16 Small-angle X-ray scattering (SAXS) of DMAEMA/MMA = 25/75 porogen in MSSQ: (i) as a function of porogen loading (fixed porogen molecular weight); (ii) as a function of porogen molecular weight (fixed porogen concentration)

Although it is much less common, the porogen can be chemically bound to the organosilicate resin [114, 115] prior to hydrolysis. This route assures no porogen aggregation during processing and the porogen may be removed after curing. Photothermal curing could be useful here as it is effective for removing bound porogens from PECVD organosilicate films. Such a route can, in principle, deliver very small pores (<2 nm) because the porosity is not generated until the organosilicate is fully cured. Mikoshiba and Hayase [114] have described the thermal stripping of alkyl substituents from the co-hydrolysate of trifluoropropyltrialkoxysilyl and methyl trialkoxysilane. The alkyl substituents are stripped at 450–500°C to yield a porous film. Only the trifluoropropyl substituent stripped easily and a dielectric constant of 2.3 was measured with pores sizes in the <1 nm regime. Another interesting example is the BOSS process reported by Dow Corning. Hydridosilane resins could be hydrosilylated with terminal olefins to produce resins with long-chain alkyl substituents [115]. These could be removed thermally (>450°C) to produce dielectric constants ranging from 1.8 to 2.2 with pore sizes around 2 nm.

There are a number of recent reports of porogens bound directly to the preformed SSQ matrix material [116, 117]. Such systems have been described as hybrid systems in the article by Yoon *et al.* [116]. The porogen was poly(methyl methacrylate) grown from the SSQ matrix by atom transfer radical polymerization (ATRP). Calcination produced sub-2.5 nm pores and a dielectric constant of 2.2 at 30 wt.% loading level of porogen. Another hybrid system is produced by the co-hydrolysis of a 4-arm caprolactone porogen with triethoxysilyl functionalities on the arms with MSSQ monomeric precursors [117]. Calcination of cast films produced 5 nm pores and only a 5% drop in refractive index at a porogen content of 30%.

Chemical incorporation of polymeric porogens into the vitrifying prepolymer matrix has also been described [118–121]. Here the porogen is not bound to the resin initially, but becomes incorporated during curing. Ree *et al.* [118, 119] have functionalized poly(caprolactone) chain ends in multi-arm polymers (4–6 arms) with trialkoxysilyl alkyl substituents and blended them into MSSQ. The pore sizes generated are much smaller (5–7 nm) than for the porogens without reactive end group functionalization and dielectric constants as low as 1.67 for 40% loading have been achieved. The major benefit seems to be that the pore size does not increase significantly with loading level. In a related study, Ko and co-workers [120, 121] disclose the use of alkoxysilane terminated, branched organic molecules, which can act as porogens. Branched molecules, such as pentaerythritol tetraacrylate and triallylcyanurate, are hydrosilylated with trialkoxy silane using the Karstedt platinum catalyst to yield the corresponding tetrakis- and tris-trimethoxysilyl derivatives, respectively. The two structures, shown in Figure 2.17, are then incorporated in the traditional acid-mediated hydrolysis and condensation of partially hydrolyzed and condensed organosilicate materials derived from tetralkoxysilanes, alkyltrialkoxysilanes, dialkyldialkoxysilanes as well as the structures described earlier in Figure 2.5.

The use of relatively low-molecular-weight organic fragments, which are intimately mixed with the organosilicate hydrolysate has the potential to yield small pores. However, no data indicating relative porogen loadings and corresponding dielectric constants were given.

A block copolymer of styrene and triethoxysilylpropyl acrylate has also been described as an example of a porogen [122] which becomes incorporated into MSSQ upon curing. Pore sizes of 2.2–5.2 nm have been realized and dielectric constants as low as 1.5 at >50% loading were measured.

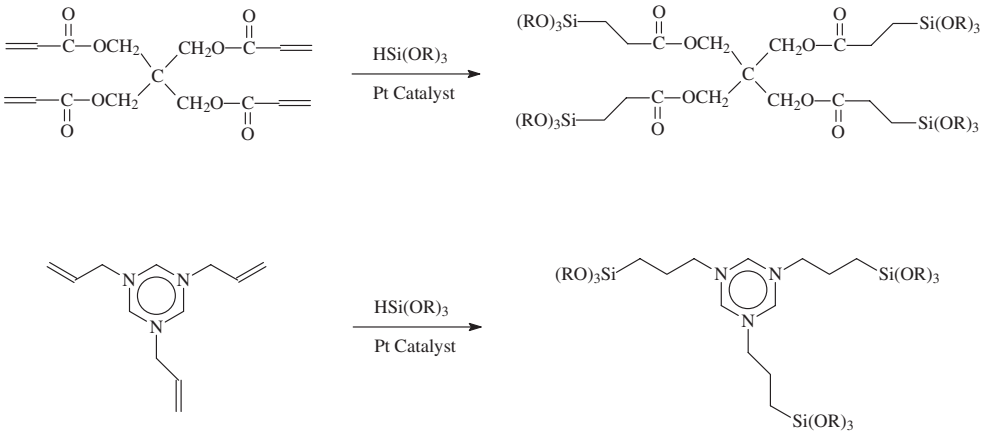

Figure 2.17 Reactive end group functionalization using hydrosilylation

In summary, N&G procedures for porosity generation are operationally simple and are capable of generating small pores with the right materials and processing conditions. The main problems are process control, given that pores sizes depend on resin chemistry, porogen structure, molecular weight (porogen and/or resin), loading levels, processing conditions, etc. The pores are randomly nucleated and are often irregular in shape with a significant pore size distribution. Furthermore, percolation to generate interconnecting pores occurs at relatively low loading levels (10–20%) unless the porogen/matrix is specifically designed to resist aggregation.

More recently the search for improved porogens has gravitated toward organic nanoparticles, some of which are synthesized by bottom-up procedures. These are being utilized as templates for porosity generation. In the templating process, the particle does not need to be miscible with the resin, but must be compatibilized so as to prevent aggregation in solution or in the film. This usually requires surface functionalization to compatibilize the particles with the resin. The synthetic challenge is to control the surface functionality and to drive the particle size below 5 nm.

Highly cross-linked organic polymer particles prepared by microemulsion polymerization constitute a templating particle [123]. This is the approach taken by Shipley in preparation of their low-*k* offering, Zirkon™ [124]. Porous organosilicates with dielectric constants tunable between 2.0 and 3.0 and sub-5 nm pore sizes have been described using this procedure and various SSQ-based matrix materials. These materials have been studied intensively within SEMATECH. Microemulsion polymerized latex particle porogens have also been incorporated into polyarylene thermosetting resins [73].

We have developed at IBM an alternate route to cross-linked nanoparticles using intramolecular cross-linking of reactive functionality initiated either thermally or with radical initiators in dilute solution [125]. When these particles are mixed with a MSSQ resin, dielectric constants down to 2.0 with pore sizes of 15 nm were achieved. The cross-linking causes the particle size to decrease from the dimensions of the random polymer coil. Because of the high dilutions required, the particle preparation procedure is hard to scale up. The dilution requirements are relieved somewhat when the intramolecular cross-linking is carried out on multi-arm stars containing the reactive functionality.

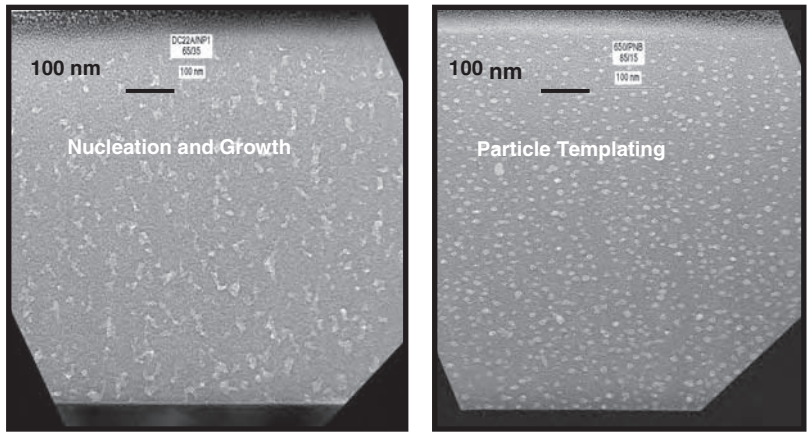

Figure 2.18 TEM samples of two different porogens at 20 wt.% loading in a low-molecular-weight (high silanol content) MSSQ resin: (a) DMAEA-MMA; (b) core–shell nanoparticles

Particle-like behavior can also be achieved without extensive cross-linking provided the porogen molecule is cleverly designed. What is needed is a core–shell organic polymer where the core is composed of hydrophobic polymer chains which are long and numerous enough that they collapse into a dense particle in the presence of a polar SSQ resin. Normally this would lead to aggregation so a compatibilizing corona needs to be added to keep the particles dispersed in the solution and in the initial films. The first materials to this type were derived from living ring-opening metathesis polymerization of substituted norbornenes followed by the addition of a branching reagent and core out growth of a hydrophilic corona. These materials templated the vitrification of MSSQ, yielding porous materials with dielectric constants as low as 2.0, albeit with pore sizes ranging from 20 to 30 nm [126]. The pore sizes were commensurate with particle size and were consistent with a one particle–one pore approach. With increased loading, the size of the pores didn't increase, they just became more numerous. The porous films were morphologically very different from the randomly initiated pores in nucleation and growth. TEM comparison pictures for both N&G and templating films are shown in Figure 2.18.

The elliptical shape of the pores in the templated film is an artifact of the focused ion beam (FIB) sample preparation procedure [127]. Since these initial studies, controlled free radical and anionic routes to multi-arm amphiphiles serving as nanoparticle templates in MSSQ have been devised [128]. Porogens as small as 5 nm have been prepared using surface small-molecule and oligomer coupling routes, obviating the need for tandem polymerizations which greatly increase particle size. The lesson to be learned here is that templating organic nanoparticle porogens provide a much more controllable route to porous organosilicates than N&G with control of pore size, density and relaxed processing constraints. The challenge seems to be reducing the porogen particle size using bottom-up synthetic routes.

Alternatively, templating can be achieved by means other than organic nanoparticles. These approaches present the opportunity of obtaining a higher degree of organization, which could potentially offer new interesting material properties. Semicrystalline porous spin-on silicates and organosilicates synthesized by these approaches are described.

Semicrystalline porous spin-on silicates and organosilicates

SCCO2 block copolymer mineralization. Recently, an interesting application of SCCO2 has been reported by Watkins and co-workers [129]. This scheme employs self-assembly and selective mineralization to produce an organized porous dielectric film. Here a block copolymer is cast on a substrate and allowed to self-assemble into a pattern dictated by the copolymer volume fractions. In the procedure, a block copolymer containing polyethylene oxide as one constituent is self-assembled in the presence of a small amount of nonvolatile acid which selectively accumulates in the PEO phase. The film is then exposed to SCCO2 containing TEOS and water which selectively mineralizes the PEO phase containing the acid catalyst. Calcination leads to a porous structure, reflecting the organized block copolymer. Organized dielectric films with good electrical properties and dielectric constants as low as 2.2 on 8-inch wafers that survive CMP conditions [130] have been demonstrated.

Periodic mesoporous silicas (PMSs). In 1992, Mobil researchers discovered that surfactant self-assembly conducted in aqueous solutions of soluble silica species results in spontaneous co-assembly of silica-surfactant mesophases. Surfactant removal creates periodic mesoporous silicas (PMSs), essentially silica fossils of the liquid-crystalline assembly [131, 132]. Despite excellent control of pore size, early mesoporous materials were in the form of powders, precluding their use in thin-film applications such as low-dielectric-constant interlayers. Mesoporous silica films obtained by spin-coating [133] or by solution deposition [134, 135], were reported for the first time in 1996. In the case of solution deposition, substrates are typically introduced into silica/surfactant/solvent systems used to prepare bulk hexagonal mesophases, where initial surfactant concentrations, c_0, are greater than the critical micelle concentration, *cmc*. Alternatively, Ogawa used a starting solution where $c_0 < cmc$, and observed that aging this solution in closed vessel until gelation, leads to an amorphous product, whereas the film obtained by spin-coating is well organized [133]. This phenomenon, studied in more detail by Brinker *et al.*, is called evaporation-induced self-assembly (EISA) [136, 137]. They have shown in the case of films prepared by dip-coating that preferential evaporation of the solvent concentrates the depositing film in water and nonvolatile surfactant and silica species. The progressively increasing surfactant concentration drives self-assembly of silica-surfactant micelles and their further organization into liquid-crystalline mesophases.

Highly ordered mesoporous silica films with dielectric constants ranging from 1.45 to 2.1 were prepared using nonionic poly(alkylene oxide) triblock copolymers and low-molecular-weight alkyl(ethylene oxide) surfactants under acidic conditions by employing a dip-coating technique [138]. As-deposited films are first heated in deionized water at 80°C overnight to increase the degree of polymerization of the silica framework and to further improve the thermal stability. In a second step they are calcined in air at 450°C to remove the block copolymers. After calcination, films porosity varies from 51 to 75% and pore size range from 34 to 90 Å, depending upon the surfactant used. A swelling agent (oil), such as polypropylene glycol (PPG), can be used in addition to the surfactant to further increase the pore size and volume [139]. In this study, PPG was added in varying amounts to a P123/TEOS/ethanol/H_2O/HCl mixture, and the sols spin-coated onto a wafer before calcination in air at 600°C. The films were then subjected to a HMDS vapor treatment at 160°C to make the pore surfaces hydrophobic. Controlled porosity, ranging from 50 to 90%, and dielectric constant between 1.3 and 2.6 were obtained. Mechanical properties of the films degrade as the amount of PPG increases; an elastic modulus of 4 GPa (nanoindenta-

tion) is obtained for a dielectric constant of 2.1. Unfortunately, the pores are too big for microelectronic applications. For instance, at 15 wt.% PPG loading, the treated film is 88% porous, and the average pore size is 12.5 nm.

Periodic Mesoporous Organosilicas (PMOs). In 1999, three different groups: Ozin, Stein and Inagaki, developed a novel class of organic–inorganic nanocomposites based on PMOs synthesis, using a silsesquioxane derived from $(EtO)_3Si–R–Si(OEt)_3$ as the sole precursor [140–142]. In these materials, known as PMOs: (periodic mesoporous organosilicas), the organic groups are located within the channel as bridges between Si centers, while a high degree of order and uniformity of pores is conserved. These new nanocomposites found their first application as low-*k* materials in 2000 with the report of films obtained by the evaporation-induced self-assembly of sols composed of TEOS, $(EtO)_3Si–(CH_2)_2–Si(OEt)_3$ (BTSE), EtOH, H_2O, HCl and Brij 56^{TM} surfactant [143]. In this study, a series of films were prepared with increasing molar percentage of BTSE: 25, 50 and 75 relative to the TEOS. Films were calcined at 350°C under N_2 and consequently vapor-treated with HMDS to limit water adsorption. For a TEOS/BTSE (25 : 75) composition, the film is 56% porous and a dielectric constant of 1.98 was obtained with a Young's modulus of 4.3 GPa (nanoindentation). The dielectric constant of these films decreases while the Young's modulus and hardness increase with substitution of the bridged silsesquioxane $(O_{1.5}Si–(CH_2)_2–SiO_{1.5})$ for silica (SiO_2) in the framework. A similar trend was observed for PMO films made with CTMAC (cetyltrimethylammonium chloride) as a surfactant by gradually replacing silica with $(EtO)_3Si–CH_2–Si(OEt)_3$ (BTSM), BTSE and a cyclic silsesquioxane: 1,3,5-tris[diethoxysila]cyclohexane $[(EtO)_2SiCH_2]_3$ [144, 145]. The measured dielectric constants, after removal of the surfactant at 300°C are 4, 2.9, 2.9 and 2.5 for porous silica, methane silica, ethane silica and 'cyclic silica', respectively. For the same materials, mechanical properties measured by nanoindentation are 10, 12.7, 13.3 and 11.8 GPa. Interestingly, methylene silica and 'cyclic silica' films treated at 400°C exhibit a lower *k* compared with the ones treated at 300°C, suggesting that the known rearrangement occurring between Si–OH and $Si–CH_2–Si$ at high temperature is beneficial to the dielectric properties of the films [146]. A similar result is observed with the ethylene silica film even though this rearrangement is not observed to a significant extent. This observation suggests that silanol condensation, as expected, also occurs between 300 and 400°C, and contributes to the decrease in dielectric constant. It is therefore difficult to decouple the effect of the rearrangement from the silanol condensation on the dielectric constant. The effect of the thermal treatment on the hydrophilicity of methylene silica samples was also studied. The change in dielectric constant for methylene silica samples exposed to 80% relative humidity for several hours is less significant for samples treated at higher temperatures: *k* changes from 1.8 to 3.3 (400°C), from 2.0 to 2.4 (450°C) and after 4 days exposure from 1.8 to 1.9 (500°C). At high temperature, silanols condensation, coupled with the 'self-hydrophobization' reaction apparently strongly decreases the hydrophilicity of the films. While this self-hydrophobization induced by thermal curing is easier to perform compared with vapor-phase silylation treatments, real manufacturing processing conditions for copper metallurgy are limited to 425°C or lower. Control over the surface properties of PMOs materials can be also obtained via a single-step synthesis in which TEOS and MTMS are co-condensed [147]. Inspired by this strategy, Balkenende and co-workers have prepared porous films, where the molar ratio of MTMS to TEOS varied from 0 to 9 [148]. They have found that with an increasing degree of methylation, up to 27 mol% of cetyltrimethylammonium bromide (CTAB) (60% porosity) could be incorporated without pore collapse, whereas this

amount is normally limited to 13 mol% for pure TEOS materials (45% porosity). Therefore, at a MTMS to TEOS ratio >0.33, a significant loss of long-range mesoporous ordering is observed compared with pure silica. Nevertheless, the MTMS to TEOS ratio has a direct influence on both the hydrophobicity and on the dielectric constant of the film. FTIR studies indicated that mesoporous films containing more than 50% MTMS in TEOS do not show a significant Si–OH signal and are hydrophobic. Furthermore, at a constant porogen loading, the dielectric constant decreases when the ratio of MTMS in TEOS increases. Mechanical properties were measured by both nanoindentation and SAWS for porous films (48–66% porosity) prepared from solutions containing 50% MTMS in TEOS and varying amounts of CTAB [149]. The Young's modulus decreases as the porosity increases, as expected, and a relatively low value of 1.5 GPa was reported for a dielectric constant of 2.0. Preliminary integration of this material showed a well-defined etch pattern, but removing of the photoresist resulted in some undercutting and bowing [149].

More recently, we have reported the synthesis of low-*k* PMO films based on the templated sol–gel polymerization of bridged silsesquioxane precursors [150]. Compared with previous studies, we have developed a process that is compatible with current integration requirements, i.e., the surfactant has to be nonionic and thermally decomposed (extraction by solvent washing was avoided), high-quality films without defects can be spin-coated on 8-inch wafers (EtOH can't be used as a solvent), halogenated acids such as HCl need to be replaced by HNO_3 to prevent chloride ion contamination and finally sol solutions should be stable for at least one month at room temperature.

We first demonstrated that sol–gel hydrolysis conditions for bridged silsesquioxane precursors need to be precisely controlled in order to obtain high-quality films with the targeted electrical and mechanical properties. Optimization of the hydrolysis conditions: solvent, precursor concentration, water and acid stoichiometries, was based on the measured refractive index, dielectric constant, film thickness and Young's modulus after curing. Results of this study are presented in Table 2.7.

When a sub-stoichiometric amount of water is used, either no film is left after baking (entry 1) or the film obtained contains more porosity than expected, suggesting that low-molecular-weight oligomers of the bridged silsesquioxane volatilized during the thermal treatment (entry 2). When a stoichiometric amount of water or higher is used (entries 3–7), little influence on the studied properties is observed, indicating that the hydrolysis conditions allow the formation of higher-molecular-weight polymers to eliminate volatiliza-

Table 2.7 Optimization of the room-temperature hydrolysis conditions for a bridged silsesquioxane solution containing 21.5 wt.% porogen

Entry	H_2O (equivalents)	H^+ (mol%)	*R* index (632.8 nm)	Thickness (nm)	E_{SAWS} (GPa)
1	1.5	2.7	No film	—	—
2	3	5.4	1.1908	685.7	1.41
3	6	10.8	1.2360	591.1	4.85
4	9	16.2	1.2351	546.6	6.76
5	12	21.6	1.2343	525.2	6.82
6	15	27	1.2409	512.1	6.35
7	18	32.4	1.2401	498.9	6.01

tion during the baking stage. Furthermore, the stability of 30 wt.% bridged polysilsesquioxane solutions in 1-methoxy-2-propanol containing a poly(alkylene oxide), water and a catalytic acid was studied over time, based on the time to formation of a gel. At room temperature the prepared formulations were stable at least for one month before a gel is formed. Under optimized conditions, the acidic hydrolysis of bridged silsesquioxanes in 1-methoxy-2-propanol with no porogen present, followed by spin-coating and curing to 450°C leads to high-quality films with a modulus of 27 GPa (nanoindentation) and a dielectric constant of 3.6.

The electrical and mechanical properties for bridged polysilsesquioxane films of varying porosity generated using a typical poly(alkylene oxide) porogen were also investigated and are presented in Table 2.8.

While the dielectric constant decreases with increasing porosity as expected, a more linear behavior of the Young's modulus as a function of the level of porosity is observed. This result contrasts with SSQ–porogen mixtures where the fall-off in modulus is exponential. The modulus numbers obtained for bridged polysilsesquioxane films (Table 2.8) are the largest by far of any of that we have observed for porous films generated using the sacrificial porogen route. The comparative modulus values for a number of porous materials are given in Table 2.9 for dielectric targets of 2.3 and 2.0.

Table 2.8 Electrical and mechanical properties of porous bridged silsesquioxane films

Porogen loading (wt.%)	*R* index (632.8 nm)	Thickness (nm)	E_{SAWS} (GPa)	E_{nano} (GPa)	*k* (25°C)
0	1.4482	326.2	22.76	27.34	3.61
5	1.3701	389.8	13.09	17.62	2.97
10	1.3174	436.1	9.99	12.67	2.69
15	1.2705	499.0	7.86	8.88	2.40
20	1.2303	571.6	6.40	6.37	2.05
22.5	1.2156	590.7	5.54	4.88	1.98
25	1.2026	613.8	3.78	4.19	1.88
27.5	1.1905	651.2	2.51	2.87	1.82

Table 2.9 Film mechanical properties for different matrix at $k = 2.3$ and $k = 2.0$

System	Deposition method	*k* (25°C)	E_{SAWS} (GPa)	E_{nano} (GPa)
MSSQ-1	spin-on	2.3	2.02	3.52
MSSQ-2	spin-on	2.3	1.90	—
MSSQ-2/UV treated	spin-on	2.3	2.80	—
CDO*	CVD	2.3	—	3.8
Oxycarbosilane	spin-on	2.3	7.86	8.88
MSSQ-1	spin-on	2.0	1	1.65
Oxycarbosilane	spin-on	2.0	5.54	4.88

*Carbon-doped oxide with UV post-porosity toughening

As presented in Table 2.9, the Young's modulus measured for bridged polysilsesquioxane films are exceptionally high, ranging from 4 to 6 times the value produced from SSQ derivatives with similar porogens. Moreover, the porous bridged polysilsesquioxane mechanical properties are 2 to 3 times higher than the best porous UV-treated materials deposited by either spin-on or CVD processes. It is worth noting that the mechanical properties obtained for the bridged polysilsesquioxanes at $k = 2.3$ and 2.0, presented in Table 2.9, correspond to cured samples with no post-porosity treatment. As a result of the exceptional mechanical properties of these materials, coupled with their remarkable electrical properties, we believe that these bridged polysilsesquioxane materials are promising new candidates for dielectric applications at $k = 2.3$ and beyond. Preliminary integration studies for 2.0 dielectric constant films are currently underway.

Crystalline porous spin-on silicates: silica zeolites. Zeolites (derived from the Greek words *zeo* (to boil) and *lithos* (stone)) are microporous crystalline materials that consist of open aluminosilicates frameworks derived from $[SiO_4]^{4-}$ and $[AlO_4]^{5-}$ tetrahedra, linked to form cages, channels or cavities of various sizes [151]. The negatively charged frameworks are balanced by positively charged cations of appropriate size located at various positions in the lattice. Because of their well-defined micropores and the presence of acidic sites inside the pores, zeolites have been successfully employed for a diverse range of applications: ion exchange, separations and catalysis (oil refining, petrochemistry, organic synthesis) [152]. While pure silica zeolites: silicalite-1 (similar to ZSM-5) [153] and silicalite-2 (similar to ZSM-11) [154] were synthesized for the first time at the end of the 1970s, it is not until recently that these materials have received some attention from semiconductor manufacturers as potential low-k intermetallic dielectrics. Since silicon is tetravalent, pure silica zeolites (PSZ) do not contain framework charges and consequently no cations, that would be detrimental for electronic applications, are present. Due to their dense crystalline structure, better mechanical properties are expected, and since their pore size (<2 nm) is significantly smaller than integrated circuit (IC) features, the problem of electrical breakdown should be mitigated by the absence of any randomly occurring large pores.

The first films made of silica zeolites were obtained following two strategies [155]:

(a) *in situ* crystallization in a Teflon-lined Parr autoclave (165°C, 2 h) of a solution composed of 0.32 TPAOH (tetrapropylammonium hydroxide)/TEOS/165 H_2O;

(b) spin-coating of a silicalite nanocrystals containing solution [156, 157].

Independent of the method used to grow silicalite films, a post-synthesis thermal treatment at 450°C for 2 h is applied to remove the tetrapropylammonium hydroxide (TPAOH) template.

In the case of *in situ* crystallized films, thicknesses vary from 200 to 500 nm, and chemical mechanical polishing (CMP) needs to be performed initially to smooth the surface. These films possess excellent mechanical properties with $E = 30–40$ GPa (nanoindentation) for dielectric constants ranging from 2.7 to 3.1. The effect of water adsorption on the k value of silicalite films was examined by exposing the sample to air at 60% relative humidity. The k value increases from 2.7 to 3.3 after an exposure time of 30 h ($k = 3.5$ after several days).

On the other hand, silicalite spin-on films present lower dielectric constants ($k = 1.8–2.1$) due to the additional porosity gained from inter-nanocrystal packing voids [155]. A uniform interparticle pore size of 17 nm and an interparticle pore volume of 0.40 cm^3g^{-1} were meas-

ured by N_2 adsorption experiments performed on bulk samples. While beneficial in terms of dielectric constant, the presence of larger mesopores is not only of concern for practical applications, but also affects the adhesive properties of these films, leading to failure during CMP. To address this issue, a brief secondary growth of silicalite nanocrystals can be applied, resulting in the loss of the interstitial porosity, an increase of the dielectric constant to a value of 3.0 and restoration of the adhesive properties observed for the *in situ* crystallized films. This second silicalite growth can be avoided by using an amorphous silica containing silicalite nanocrystals solution. Here, the mesopore size is reduced from 17 to 2.3–2.6 nm, resulting in a film with better mechanical properties (E = 16–18 GPa by nanoindentation) and a dielectric constant of 2.3 [158]. Positron annihilation lifetime spectroscopy (PALS) was used in this case to confirm the presence of micropores (0.55 nm) due to the zeolite framework, in addition to open/interconnected mesopores (2.3–2.6 nm) [159]. Unfortunately the film is quite hydrophilic, as shown by an increase in dielectric constant from 2.3 to 3.9 within 1 h exposure to ambient air at 50–60% relative humidity. To render the film hydrophobic, vapor phase silylation was conducted. After silylation, a dielectric constant of 2.1 was obtained, this value changes slightly over time upon exposure to air. Interestingly, because these films are composed of a mixture of amorphous silica and silicalite nanocrystals, not only the overall ratio of one silica component versus the other (in other words the total level of film crystallinity), but also the nature of the zeolite (MFI or MEL), influence the dielectric properties of the material. Using a two-stage hydrothermal synthesis method, the yield of nanocrystals for a given particle size, can be increased in the solution used for film preparation. A direct effect is observed on the dielectric constant of the films with higher crystallinity, leading to lower k values [160, 161].

At the same relative level of crystallinity, changing the nature of the zeolite nanocrystals from MFI to MEL also results in a lower dielectric constant. The authors point out that a lower k is expected because MEL has a lower framework density (FD) than MFI [161]. Since different sizes of nanocrystals are used in this study, and the total porous volume of the films is different, it is not clear whether this result can be directly correlated to the nature of the zeolite or is governed by other parameters such as size of the nanocrystals, mesoporous volume and number of residual silanols. Without silylation, and independent of the level of crystallinity, the synthesized films are still highly hydrophilic. To prevent water adsorption in PSZ films, organic-functionalized PSZ MFI films (OF PSZ) have been synthesized [162]. Incorporation of Si–Me groups in the zeolite framework was achieved through addition of $MeSi(OMe)_3$ to the synthesis solution of MFI nanoparticles. Upon exposure to ambient air for 1 h, the dielectric constant of the OF PSZ film increased from 2.25 to 2.74 (20%), compared with a 70% increase for the nonfunctionalized film (10% after silylation). Whether the introduction of Si–Me groups affects the crystallinity of the zeolite and therefore changes the mechanical properties of the film is not known.

In order to achieve a tunable k value in an even lower range on the MFI low-k material, incorporation of nanosized voids using γ-cyclodextrin as a porogen was explored [163]. By introducing 5–15 wt.% γ-cyclodextrin, controllable interparticle porosity ranging from 2.71 to 3.29 nm was created. The dielectric constant decreases in relation to the amount of porogen used. A value of 1.8 is obtained for 15 wt.% porogen loading, while the mechanical properties for this film remain excellent (E = 14.3 GPa by nanoindentation). Unfortunately all of the cyclodextrin containing films required heating to 450°C for 9 h to ensure full decomposition of the porogens (cyclodextrin and TPAOH), making this process unsuitable for integration.

2.4 NEW PROCESSING STRATEGY TO INTEGRATION ISSUES

Addressing the shortcomings of porous organosilicate materials, especially as experienced during device fabrication, has led to an innovative approach, which targets the poor mechanical properties complicating CMP, surface roughness and etch sensitivity. Traditional microelectronic device fabrication using porous dielectric materials involves deposition of a B-staged material, curing of the dielectric material at elevated temperatures to achieve sufficient dimensional stability and generation of porosity, followed by conventional damascene processing. In addition to the expected decrease in dielectric constant and mechanical properties, such as modulus and hardness, the presence of pores during subsequent damascene processing can cause problems with respect to the sidewall surface roughness of features etched into the porous material. This surface roughness is a source of increased etch damage encountered during patterning by reactive ion etching and photoresist stripping. The etch damage manifests itself by surface oxidation of the dielectric material, leading to increased moisture sensitivity and ultimately affecting the electrical properties, particularly leakage current and dielectric constant, of the insulating layer. In addition, the presence of such roughness may create discontinuities in the deposition of seed or barrier layers commonly employed in device fabrication. At very high porosities, i.e., above the percolation threshold, the possibility of copper intrusion into the dielectric material due to incomplete barrier deposition becomes increasingly likely.

One way to circumvent such problems is by conducting the damascene processing in the pre-porous state, as disclosed in the patent literature [164, 165]. Of course, such an approach has very stringent requirements. Foremost among these is the shrinkage of the nonporous dielectric upon final cure to generate the porosity. Shrinkage values of less than 1% are required. Shrinkage of the dielectric can be held to a minimum if the dielectric precursor can be cured to high levels of condensation. The degree of dielectric resin cure is directly linked to the cure temperature. Hence, in the absence of nonthermal curing methods (UV, e-beam), high degrees of condensation require high temperatures. At the same time, porogen materials have to be thermally labile and should decompose cleanly and efficiently at maximum curing temperatures of 425–450°C. Based on these requirements, porogens which decompose cleanly over a relatively narrow temperature range (350–425°C) would be preferable. Unfortunately, porogens with such thermal characteristics are quite rare. The best candidates are particle porogens with maximum temperature stabilities of 250–300°C [128, 166]. Microemulsion-polymerized cross-linked, nanoparticle porogens formulated in organosilicate resins form the basis of the Zirkon® family of porous dielectric resins and hardmasks. These materials have been excercised in the ‘solids first’ approach to device fabrication using the hybrid nonporous state of the cast and partially cured film [167]. The integration approach is illustrated in Figure 2.19.

Describing the process in greater detail, the dielectric material/particle porogen is deposited on the wafer by spin-coating and baked at temperatures avoiding significant porogen decomposition (150–250°C). The blanket layer is then patterned using traditional lithographic techniques, yielding smooth via and trench sidewalls. This step is then followed by barrier layer deposition, which typically involves a PVD process with line-of-sight deposition and temperatures of approximately 275°C. This temperature reflects the maximum temperature experienced by the pre-porous stack. Following the liner and seed deposition, Cu metal is electroplated. Removal of the Cu overburden by chemical mechanical polishing (CMP) is a mechanically very aggressive procedure and benefits from the increased

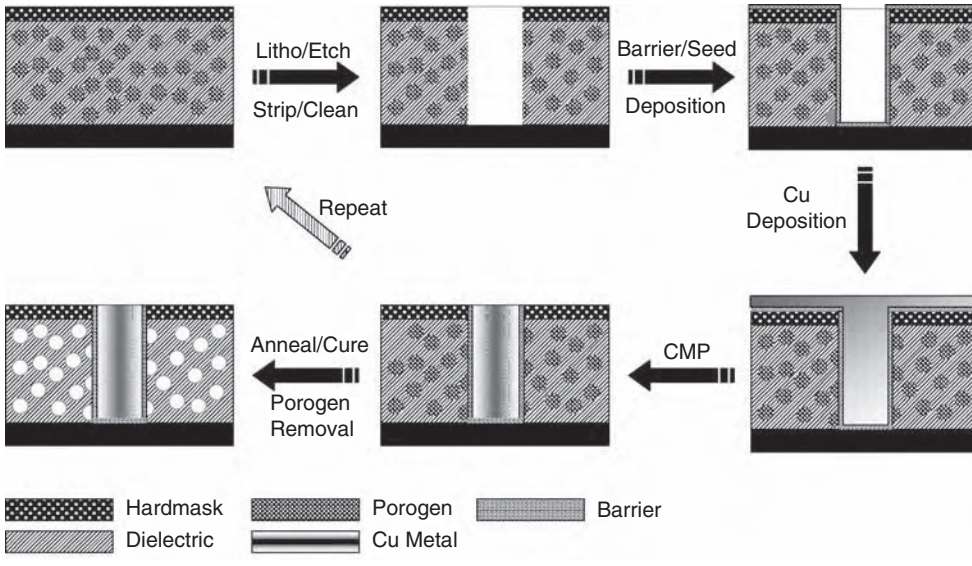

Figure 2.19 Damascene processing in the pre-porous state. The dashed arrow indicates that the process can be repeated multiple times to generate the dielectric stack

mechanical robustness of the nonporous dielectric. Presence of a semipermeable hard mask ensures the integrity of the underlying dielectric to scratching and other damage. At this stage, the personalized layer can be annealed at temperatures of 425–450°C, facilitating porogen decomposition and diffusion and generating the porous dielectric. Of course, the coating and damascene processing can be repeated numerous times in a sequential fashion to build a multi-stack structure and annealing and porogen removal can then be achieved in a single step. It should be noted that the hard mask material must be permeable to the porogen decomposition products. This permeability can be facilitated by incorporation of small amounts of porogen in an organosilicate material similar to the dielectric material. Of course, the presence of layers in addition to the interlevel dielectric (ILD) results in a slight increase of the overall dielectric constant.

2.5 SUMMARY

Spin-on polymers, which can be organic- or inorganic-like, provide greater structural diversity than available with CVD precursors for the production of both dense and porous films. This in part is due to the volatility limitations imposed on the latter by current tooling. Another feature limiting structural creativity for PECVD precursors is the production of high-energy species in the plasma and the generation of films with bonding structures which can be very different from the starting materials.

While spin-on materials can be either organic polymers or inorganic materials, the CVD dielectrics are almost exclusively inorganic-like. The difficulty of integration of any low-k dielectric material has placed a premium on dielectric extendibility through a number of

generational nodes. This will therefore require porous materials. In spite of the potential plethora of spin-on materials for both dense and porous dielectric applications, the industry will go with PECVD solutions at least through $k > 2.4$ (65 nm node). This is due in part to the capital investment in CVD tools accumulated by semiconductor manufacturers and their confidence in gas phase deposition processes. Beyond $k = 2.2$ extending to the ultimate dielectric (air gaps), the road is less clear and much more data have been accumulated for spin-on candidates. On the low-k dielectric pathway, the industry flirted briefly with organic polymers, but rapidly moved to organosilicates relegating the organic polymers to possible hybrid build applications. Some interesting conclusions that have emerged from the low-k adventures thus far are that the semiconductor manufacturing community is both very conservative and risk-adverse and it is unlikely that one manufacturer will embark on a pathway alone independent of other players.

It seems likely that organosilicates will constitute the bulk of low-k dielectrics for the future, independent of the method of application. These materials are generally thermally stable and hard but are fragile and prone to cracking. In this regard, these low-k materials are quite inferior to SiO_2 in most aspects except for the lower dielectric constants. This situation is further exacerbated as we move from dense to porous materials. Currently, it seems that the generally poorer mechanical properties will be addressed by either post-porosity toughening procedures, novel integration schemes designed to mitigate the mechanical deficiencies (porosity last, hybrid builds, incorporation of stabilizing structures, etc.) or by new materials concepts. The latter includes the use of bridging monomers, generation of nanocrystalline materials, control of pore size, morphology and order in amorphous, semicrystalline and crystalline materials, the generation of novel reactively functionalized inorganic nanoparticles, etc., and encouraging results have been described. For porous materials these concepts will all be influenced by porogens when needed and templating porogen nanoparticles and self-assembly have demonstrated utility. From the data reported, it seems that non-porogen routes to porosity will be limited to dielectric constants >2.2.

While all of the suggested routes to improve the mechanical properties through Chemistry are deeply rooted in spin-on materials, the post-porosity toughening approach is, in principle, applicable to either CVD or spin-on materials. Although the predicted meteoric rise in the usage of spin-on dielectrics relative to CVD materials suggested only 6 years ago has not occurred [168], potential applications for spin-on materials will arise to address issues for which CVD materials may be less suitable (ULK and beyond, gap-filling procedures, structures where organization matters, photodefinable and/or nano-imprintable dielectrics, block copolymer self-assembly, etc.

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3 Porosity of Low Dielectric Constant Materials

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3.1 INTRODUCTION

The most important properties of porous low dielectric constant films such as density, stiffness/strength, thermal conductivity and chemical reactivity depend on the pore structure and the evaluation of porosity is of great importance for their successful integration in ULSI technology[1]. An important step towards achieving the control of porosity, in addition to materials concerns, is the development of methods that quantitatively measure the pore structure, including porosity, average pore size, pore size distribution, and pore interconnectivity.

Different methods have been developed for evaluation of porosity and pore size distribution in bulk materials: *stereology analysis* such as microscope techniques; *intrusive methods* such as gas adsorption, mercury porosimetry; *nonintrusive methods* such as radiation scattering, wave propagation [2]. However, most of conventional porosimetries are hardly applicable to thin films because in general they have a small total pore volume and surface area.

During the last decade, few advanced techniques such as ellipsometric and X-ray porosimetries (EP [3, 4] and XRP [5], small-angle neutron and X-ray scattering (SANS and SAXS) [6–8] and positron annihilation lifetime spectroscopy (PALS) [9, 10] were successfully applied for evaluation of thin porous films. EP and XRP are based on vapor adsorption (intrusive). All these methods are based on different physicochemical ideas and each technique comes with own specific strengths and weaknesses. However, 'round robin' experiments have demonstrated that the results obtained by using all these methods are in reasonable agreement: the difference is in the range of physical uncertainty of porosity and pore size [11–13].

The purpose of this chapter is to review state of the art measurement methods of the pore structure in ILD candidate materials.

3.2 POSITRON ANNIHILATION SPECTROSCOPY

David W. Gidley, Hua-Gen Peng, and Richard Vallery

3.2.1 Introduction

The premise in using antimatter (positrons) to probe materials is that understanding the physics of matter—antimatter annihilation allows one to extract nanoscale materials information specific to the location at which the annihilation takes place. Both positrons and

positronium (Ps, the hydrogen-like bound state of a positron with an electron) tend to seek out and localize in vacancies/voids in metals and insulators. For this review of microelectronic dielectric films we will focus on Ps which readily forms by electron capture when positrons are injected into insulators. A number of spectroscopies have been developed to parameterize the annihilation process—generically called *positron* annihilation spectroscopy (PAS) even though the positron may be annihilating from the Ps state. The three main spectroscopies are in the time domain (how long the positron lives before annihilation), the energy of the annihilation gamma rays, and the momentum of the gamma rays (Doppler energy shifts and angular distribution). A complete review of PAS is well beyond the scope of this article. Moreover, these PAS were developed using radioactive beta-decay positron emitters that embed positrons deeply into materials—thin films demand low energy *beams* to control the positron implantation depth. Beam-based PAS methodologies in metal and semiconductor films and at interfaces have been comprehensively reviewed by Schultz and Lynn [14] and the reader is referred to this review for detailed discussions on depth-profiled PAS. We will focus attention on beam-based positron/Ps annihilation *lifetime* spectroscopy (beam-PALS or just PALS) because it has been the most informative annihilation spectroscopy in characterizing porous low-k films. An article with greater emphasis on the other PAS methods complementary to PALS can be found elsewhere [15]. A somewhat broader review of depth-profiled PAS in porous films is recently available [16].

Positronium annihilation lifetime spectroscopy (PALS) is a pore/void volume characterization technique whereby the shortening of the annihilation lifetime of Ps due to collisions with the pore walls is directly correlated with the pore size. Ps in vacuum will self-annihilate into gamma-rays with a lifetime of 140 ns, but in a pore its lifetime is shortened by the additional effect of the positron's annihilation with molecular electrons in the pore wall material. This is the essence of the PALS technique and it has been used for some 40 years to probe the sub-nanometer voids in bulk polymers [17]. It has been demonstrated that PALS has a good calibration for the deduced pore size vs. Ps lifetime [11, 18, 19] in the diameter range 0.3–30 nm, truly a probe of *nanoporous* materials. In addition, the diffusion of Ps within the pores of a sample can be used to determine the length scale over which pores are interconnected—a pore interconnection length (which, in turn, provides added information on the shape of the pores). Depth-profiling can reveal inhomogeneities below the film surface from such effects as pore collapse densification or pore filling by contaminants. Since PALS employs no solvents or absorbents it can probe pores hidden below perfect diffusion barriers as long as the barrier is not too thick to prevent positron penetration to the underlying dielectric. After brief overviews of the beam-PALS technique and Ps interactions with porous insulators we will discuss the current capabilities of PALS in low-k materials characterization and our expectations for future development.

3.2.2 Overview of the PALS experimental technique

A beam-PALS spectrometer is a small laboratory-scale device comparable in size to an electron microscope. In using PALS with thin films, an electrostatically focused (or magnetically guided [20]) positron beam of several keV is transported and focused on a target in a high vacuum system. The beam is usually generated using a sealed, commercially available, ^{22}Na radioactive beta-decay positron source (Figure 3.1), but other positron

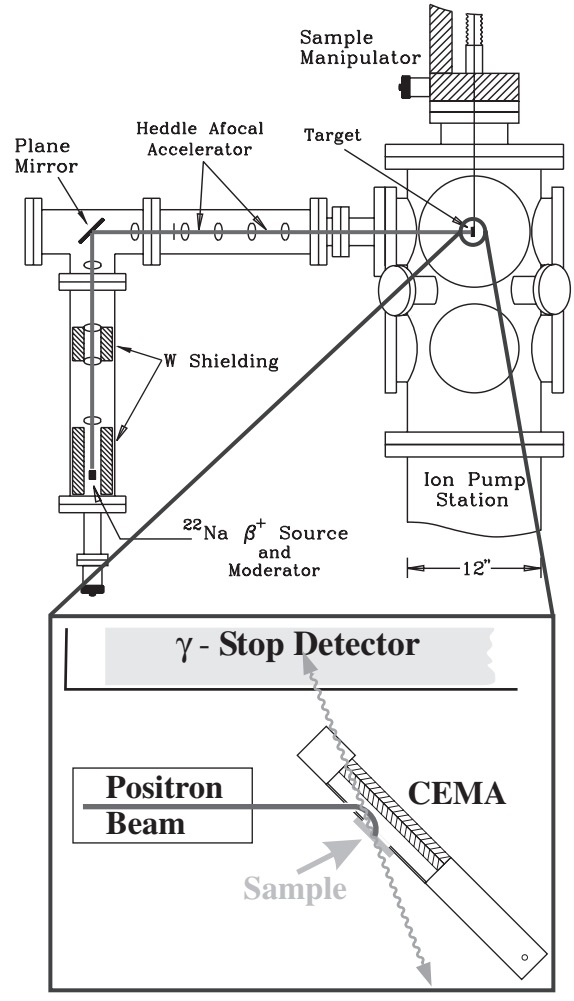

Figure 3.1 Schematic of the Michigan depth-profiled PALS spectrometer (Reprinted from *New Directions in Antimatter Chemistry and Physics*, page 154, C.M. Surko and F.A. Gianturco. Copyright (2001) with kind permission from Springer Science and Business Media)

generation schemes are available (e.g., pair-production by high-energy photons [21]). This beam is deflected onto a target sample as shown in the inset to the Figure 3.1 and forms Ps at a depth distribution within the film that is determined by the incident positron energy (0.1–10 keV). The beam spot on target is 3–5 mm in diameter and can be smaller for lateral resolution of millimeter-sized target fields on patterned wafers. Maximum sample size is currently governed only by vacuum system constraints, but this is not a fundamental limitation and PALS spectrometers capable of handling 300 mm wafers have been designed. Positrons striking the sample generate secondary electrons that are detected in a channel electron multiplier array (CEMA) and the Ps lifetime for each event is the time between this CEMA signal and the subsequent detection of annihilation gamma-rays by a plastic scintillator. Each positron annihilation event is individually timed and counted. For typical

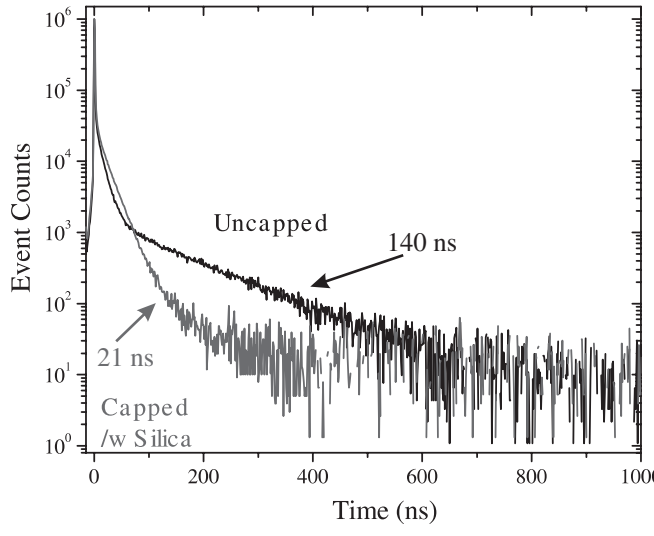

Figure 3.2 PALS spectra of an uncapped and capped porous MSQ low-*k* film of 22% porosity

data rates of 1–2 thousand events/s, each PALS spectrum currently requires roughly 30 min to reach 2 million total events for acceptable statistics. On the other hand, the beam-induced target damage that can be so significant in electron microscopes is highly negligible for such a 0.01 pA beam of 10 keV positrons. Projected technological improvements to enable PALS acquisition on full-sized wafers in <30 s/spectrum will be discussed in the section on future improvements of PAS capabilities.

A PALS spectrum is a lifetime histogram of all the annihilation events of the implanted positrons. It is a combination of several exponentially decaying lifetime components and may involve a continuum of lifetime components as well.

Figure 3.2 presents examples of typical lifetime spectra. Every beam-PALS spectrum contains at least two lifetime components: one is less than 0.5 ns, the prompt annihilation of positrons that do not form Ps (the peak marking $t = 0$ in the Figure 3.2); the other is the vacuum positronium lifetime of 140 ns. The pore sensing Ps lifetime components, typically one to three, are related to the voids of various sizes that may exist in the material. Spectrum fitting programs, such as POSFIT [22], are used to deconvolve the system's fast time resolution and determine the primary fitted data: the Ps lifetimes and their corresponding relative intensities. Further discussion of the fitting and interpretation of the lifetime spectrum will be presented in succeeding sections.

3.2.3 Ps in porous films

The formation of Ps in a porous insulator from an incident beam of positrons is depicted in Figure 3.3. The positron slows down through collisions in the material from its initial energy of several keV to several eV. It can either capture a bound molecular electron or recombine with free 'spur' electrons liberated by the positron's ionizing collisions to form the bound state of Ps. This Ps, which initially has a few eV of kinetic energy, begins to

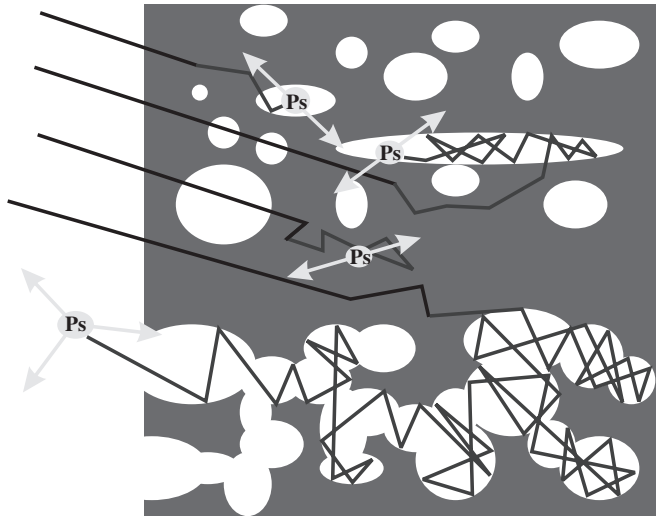

Figure 3.3 Positronium formation in porous materials (Reprinted from *New Directions in Antimatter Chemistry and Physics*, page 154, C.M. Surko and F.A. Gianturco. Copyright (2001) with kind permission from Springer Science and Business Media)

diffuse and thermalize in the insulator. In porous films it is energetically favorable for Ps to be attracted to and trapped in any voids where its binding energy is greater than in the dielectric medium. However, even when it is thermalized in the pores, Ps is still frequently colliding with the pore walls and the resulting Ps lifetime is shortened by enhanced positron annihilation with electrons in the material (i.e., electrons other than the one bound in Ps).

Ps may diffuse within the pores over long distances that can even be greater than the porous film thickness if the pores are *interconnected*. In Figure 3.2, the spectrum of the uncapped porous MSQ film presents a pronounced vacuum Ps component of 140 ns. Evidently, some Ps diffuse out of the film and into the surrounding vacuum as depicted in the lower half of Figure 3.3 (we estimate that Ps can make about 10^6 pore-wall collisions before annihilation). The observable effect is that escaping Ps annihilates with the vacuum lifetime of 140 ns, a tell-tale indicator that the pores in the film are interconnected. Any curtailment of Ps escape and hence any limitation in its diffusion length must be governed by the pore morphology and it is straightforward to deduce an average pore interconnection length from depth-profiling (to be discussed in Section 3.2.4). If the pores are highly interconnected, then to extract the average pore size (technically, the mean free path for Ps in the interconnected pores) it is necessary to deposit a thin diffusion barrier on top of the film to keep the Ps corralled in the porous network [23]. In the spectrum of the capped MSQ film in Figure 3.2, the pronounced vacuum Ps component is eliminated, replaced by a dominant Ps lifetime of 21 ns, corresponding to porogen-induced pores with a mean free path of 1.6 nm.

If the pores are closed (like Swiss cheese as in the upper part of Figure 3.3) then Ps should be trapped in a pore; no diffusion barrier is required. Furthermore, a distribution of Ps lifetimes occurs if there is a pore size distribution (PSD). Techniques have been developed for deducing a PSD from continuum lifetime fitting of the annihilation lifetime distribution [9] and will be discussed.

3.2.4 Pore characterization with PALS

Determination of pore size

PALS has the attractive feature of a direct one-to one connection between fitted Ps lifetime and pore size. The quantum mechanical model first developed by Tao [24] and Eldrup [25] in the early 1980s has been empirically used to calibrate Ps lifetimes of several nanoseconds with the sizes of micropores, such as those in polymers of ~0.6 nm diameter [26]. In this simple model Ps is localized in an infinitely deep potential well and annihilates with molecular electrons only when it is within a short distance of the pore surface. With only the ground state of Ps in the well being populated in this Tao–Eldrup model, it is insufficient for characterizing larger mesopores when the pore diameter approaches the thermal de Broglie wavelength of Ps (about 6 nm). Thermally excited states of Ps atoms in the pore must also be included in the calculation.

The Tao–Eldrup model has been extended in order to characterize both micro- and mesopores. To summarize the results [23, 27] it is assumed that the Ps atoms randomly sample all of the states in a rectangular well with a probability governed by the Maxwell–Boltzman distribution. At a given temperature, a lifetime vs pore dimension curve can then be calculated. It is useful to convert such curves from a model-specific pore dimension to a classical mean-free path, $l = 4V/S$, where V/S is the volume-to-surface area ratio of the pore. The mean-free path is a linear measure of pore size that is independent of pore geometry. Figure 3.4 shows lifetime vs mean-free-path curves at several different temperatures. The model includes only one universal fitting parameter that is determined by existing experimental data for l below 2 nm. For insulators this parameter is assumed to be material independent although, in principle, at some degree of material specificity would be expected. In the past 5 years the Michigan positron group has participated in many round robins

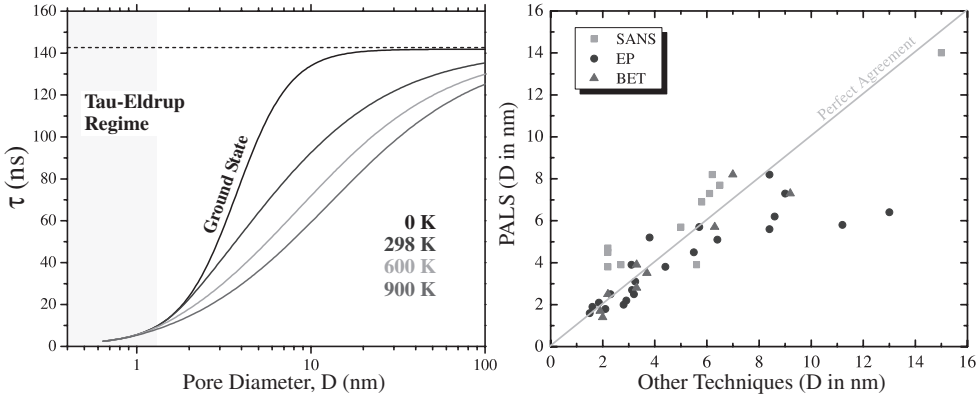

Figure 3.4 Pore size calibration calculated at different temperatures vs mean free path (left-hand panel). Recent round robin comparisons (right-hand panel) of PAS pore diameters with those measured by small-angle neutron scattering (PANS), ellipsometric porosimetry (EP), and gas absorption (BET) (Left-hand panel reprinted from *New Directions in Antimatter Chemistry and Physics*, page 154, C.M. Surko and F.A. Gianturco. Copyright (2001) with kind permission from Springer Science and Business Media)

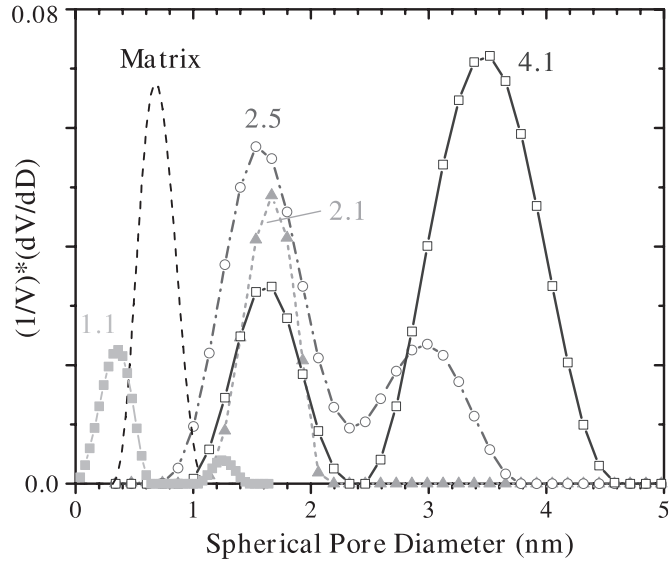

Figure 3.5 Plausible pore size distributions in a low-*k* film as a function of position beam energy (legend, in keV) determined from continuum lifetime fitting. This film has a complicated depth dependence on porosity

where a variety of film samples are shared by different groups in order to compare pore sizes measured with different techniques. PALS agrees quite well overall with other methods (Figure 3.4, right-hand panel). PALS tends to measure pore diameters that are slightly larger than SANS, slightly smaller than EP, and in excellent agreement with BET. The pore size calibration appears to be very reliable.

The discrete lifetime fitting of the lifetime spectra is a robust procedure that determines the *average* size of the pores in the material. However, this analysis can be complicated by multiple-lifetime spectra that occur when micropores and mesopores coexist and each may involve interconnected pores and/or a distribution of pore sizes. To further characterize the porosity of a film, pore size *distributions* (PSDs) are determined by fitting the decay spectrum to a continuum of lifetimes [28] which are then converted into fractional pore volume as a function of spherical pore diameter (or cylindrical diameter) [9]. PSD results acquired at several positron beam energies are shown in Figure 3.5 for a rather exotic dielectric film in which the pore structure is changing rapidly with depth below the surface. One limitation of PSD fitting [29] is the uniqueness of the fitting results (a common problem in continuum fitting). Thus, the continuum fits are typically referred to as 'plausible PSDs'.

Determination of film porosity

In the previous section it was shown how direct the physical interpretation of the fitted Ps lifetime is in regard to pore size. The interpretation of the fitted relative *intensity* in each Ps lifetime component in the spectrum in terms of film porosity is not as straightforward. Whereas the pore size calibration with lifetime is quite universal in insulators there are a

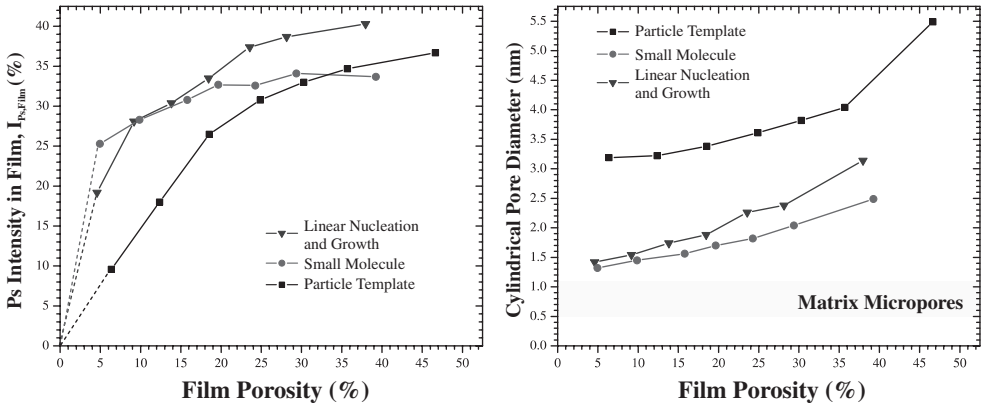

Figure 3.6 Plots of Ps intensity annihilating in the film and measured pore diameter vs porosity (determined using refractive index and the Lorentz–Lorenz equation) for films made with three different porogens. Together the intensity and diameter can be used as a measure of *relative* porosity in chemically similar films. Films supplied by R.D. Miller, IBM

number of factors that influence the relative intensity of Ps annihilating in the pores, not simply the porosity. The overall Ps formation fraction depends on the material chemistry of the insulator and can be significantly altered by additives and free radicals. Moreover, pore size affects the relative intensity of Ps annihilating in the pores, even for films of identical chemistry and porosity; thus the absolute porosity calibration must depend in a more complicated way on Ps intensity and pore size. This interdependence on pore size can be seen in Figure 3.6 for three films with distinctly different pore generators (porogens) in a common MSSQ matrix. The plotted intensity includes the sum of Ps annihilating in the mesopores and Ps that diffuses through the interconnected mesopores to escape into vacuum. Hence, $I_{Ps,film}$ is a total measure of how much Ps finds its way into mesopores and should be related to the porogen-induced mesoporosity. In these films there is a clear monotonic trend upward in $I_{Ps,film}$ with increasing mesoporosity (left-hand graph) and the rate of rise correlates well with the measured pore size (right-hand graph). At any given porosity the matrix 'wall' thickness between large pores is greater than that for small pores. For Ps to populate the mesopores it must be formed in the matrix and diffuse/hop through its micropores. As porosity rises *and/or pore size decreases* the wall thickness between pores shrinks, which favors the diffusion of Ps into the mesopores. As a result, $I_{Ps,film}$ increases at the expense of the Ps intensity annihilating in the micropores.

Despite the more complicated dependence of fitted Ps intensity on porosity, pore size, and film chemistry the curves in Figure 3.6 do indeed represent the *absolute calibration of porogen-induced mesoporosity*. This calibration relies on an independent measure of porosity and hence is not fundamentally a stand-alone measure, but this limitation might be quite acceptable in a production environment where the matrix–porogen system can be well calibrated. On its own, PALS fitting of Ps intensity and lifetime (pore size) is more effective in determining *relative porosity* in porous films with unchanged chemistry. With extensive study to determine the mobility of Ps in the matrix micropores (the Ps diffusion or hopping length) it is possible to better interpret the physical significance of the Ps intensity. However, this research approach does not lend itself to rapid turn-around in pore characterization.

While it is more challenging to use PALS as an absolute calibration of mesoporosity there is other significant information to be gleaned from the Ps intensity. The greater sensitivity of the fitted Ps intensity can be used as a warning of a change in film parameters. For example, comparisons between pristine and processed low-k films may show changes in Ps intensity that are not a result of a change in porosity, but rather a change in the chemistry of the film. This has been demonstrated in high pressure CO_2 cleaning studies [30] of low-k dielectrics and in Ta barrier deposition studies using atomic layer deposition with chemical precursors [31].

Depth profiling of films

Methodology. A particularly powerful feature of beam-based PALS is the ability to control the mean depth that positrons are implanted into the film by simply adjusting the energy that the incoming positrons strike the target. The implantation profile can be determined using a well-tested transmission model [14, 32] and is shown in Figure 3.7 for the Michigan positron beam. The mean positron implantation depth $\bar{Z}$ is given for normal incidence of the beam by $\bar{Z} = (40/\rho)E^{1.6}$ nm, where E is the positron beam energy in keV and ρ is the film density in g/cm^3. The implantation profile is roughly bell-shaped and ranges from the surface of the film to about twice the mean depth. Therefore, the best depth resolution occurs for low energy (shallow implantation). It should be noted that this positron implantation profile corresponds quite closely to the Ps *formation* depth profile (there may be several nm spreading due to the electron-positron correlation process to form Ps), but does not necessarily correspond to the Ps *annihilation* profile. If the pores are interconnected then the Ps may diffuse a long distance away from its formation location. Hence, the fitted Ps lifetime may reflect an average over a large region of the film, but even so the Ps formation *intensity* is still characteristic of the location of formation. Depth-dependent variations in this Ps intensity may reflect changes in porosity with depth. Of course, if the pores are isolated and trap Ps then the lifetime will also indicate any pore size variation with mean implantation depth as will be illustrated in the next section.

Pore interconnection length. By depth-profiling a porous material one is able to measure the length over which the induced mesopores are interconnected. Ps can diffuse through 1000-nm-thick films if the pores are fully interconnected, escape from the film, and annihilate in vacuum with the tell-tale lifetime of ~140 ns. Partially interconnected pores will result in a much smaller measured Ps diffusion length that is determined by the pore inter-

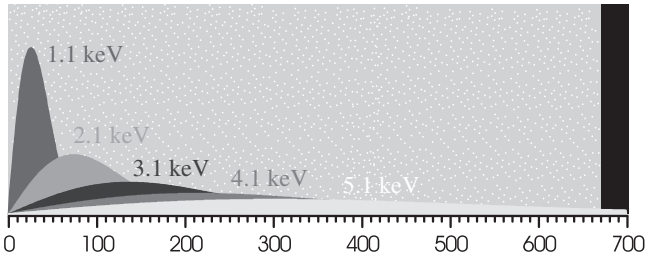

Figure 3.7 Porosity implantation profiles for several beam energies calculated for 45° incidence on a film of density 1 g/cm^3

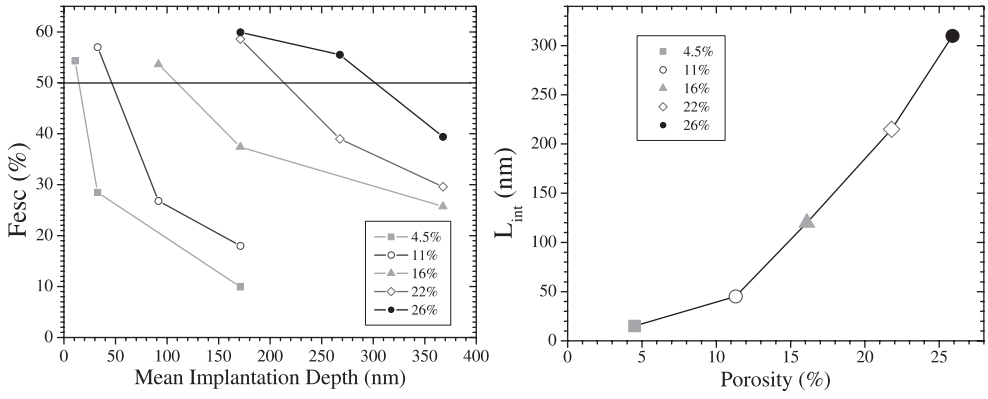

Figure 3.8 Plot of the Ps escape fraction F_{esc} as a function of mean positron implantation depth (left) used to calculate the mesopore interconnection length L_{int} (right) for films of increasing porosity. This film is a cyclodextrin-based porogen in a MSSQ matrix

connectivity. By straightforwardly measuring the fraction of Ps that escapes from the film F_{esc} as a function of mean positron implantation depth, as shown in Figure 3.8, we are able to deduce the *pore interconnection length* L_{int} of the mesopores. By applying a diffusion model to Ps in the film we are able to calculate L_{int} of the mesopores to be the mean implantation depth from which approximately 50% of Ps escapes from the film. The low-k films analyzed in Figure 3.8 are MSSQ hosts with pores generated by a degradable porogen. PALS depth profiling determines the average depth over which porogen-induced pores (mesopores) are connected to the surface, a physically simple and direct interpretation of pore connection. As evident in the left-hand plot, deeper implantation results in lower Ps escape as more Ps traps and annihilates in pores that are not connected to the surface. It has been noted that once Ps is in these mesopores it is energetically trapped from returning to the micropores of the MSSQ matrix [23, 33] and therefore Ps diffusion is governed solely by the *mesopore* morphology. As such, PALS might therefore be the ideal probe for studying the fundamental formation process, structural characterization, and evolution with porosity of the strategically introduced pores without the interference of the matrix microporosity! Moreover, as the porogen-induced porosity of the film increases the deduced value of L_{int} increases rapidly (right-hand plot in Figure 3.8) as porogen aggregation (not unexpectedly) produces pore clustering that will eventually lead to film percolation (pore interconnection throughout the film). Thus PALS is providing a very unique view of the film's *pre-percolation regime* where finite clustering of the porogen domains, and hence the pores, evolves towards percolation. This provides fundamental information on pore growth and pore shape, as will be discussed later.

Detecting porosity variations in film depth. In the previous section we indicated how routine depth-profiling can determine the pore interconnection length for a porous film that is homogenous in depth. What if the film is not homogenous, the porosity and/or pore sizes are changing with depth? What if the porous dielectric is buried beneath a diffusion barrier or etch stop? What if one simply wants to isolate a particular dielectric layer in a multilayer stack? Positrons can be implanted at controlled depths to form Ps underneath a surface layer(s) that might normally inhibit absorption in solvent-based porosimetries. Thus beam-based PALS can study hidden porosity beneath diffusion barriers, dense or capping layers,

and multilayer films. The diffusion barriers of any material can be tested for integrity, minimum critical thickness, and thermal stability on any underlying low-*k* film that has interconnected pores [34, 35]. PALS is well suited to test diffusion barriers and advanced sealing strategies such as plasma surface densification on blanket and patterned films. Additionally, depth-profiled PALS investigates inhomogeneities present in as-deposited or processed low-*k* films. For example, plasma densification (pore collapse) can result from exposure to plasmas in microchip processing [31, 36]. This type of 'integration damage' can severely compromise the dielectric constant reduction by a low-*k* material [31].

A good example of the capability of PALS depth profiling was recently demonstrated in the study of a plasma-enhanced chemical vapor deposited (PECVD) SiCOH film [37]. The depth-dependent pore size distributions have already been introduced in Figure 3.5 and they present indication of strongly increasing pore size and porosity with film depth. A multilayer model for the pore structure of this film that is consistent with the depth-profiled spectra is shown in the sketch of Figure 3.9. (Depths in this profile are determined using the average density of the film—more (less) dense regions will be proportionately thinner (thicker) than shown). The top 30 nm of this film appears to be dense (not even microporous) followed by another 30 nm of film which is microporous only. When the film is probed more deeply, 1.5 nm mesopores begin to reveal themselves at depths of 60–170 nm. Even more surprising, at depths greater than 170 nm another layer is discovered where 3.5 nm diameter pores dominate the porosity. Simple PALS depth-profiling alone cannot determine whether the large pores in this *buried* layer are interconnected because the tell-tale escape of Ps into vacuum has been curtailed by the upper layers. The solution was to etch off the upper layers

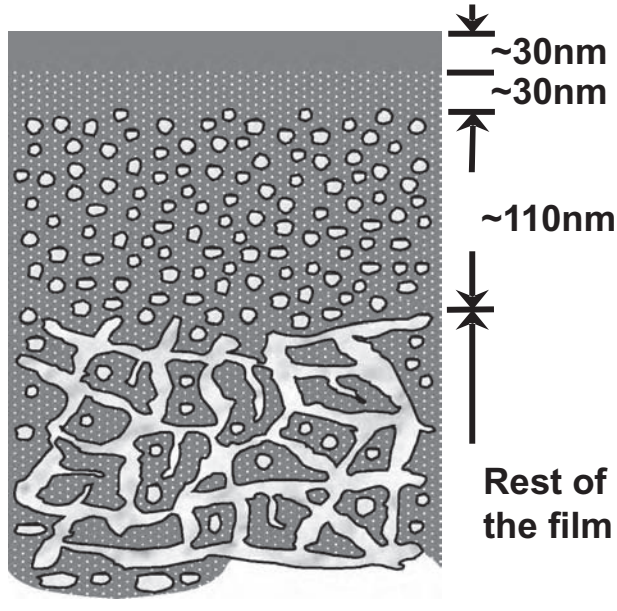

Figure 3.9 Schematic of the porosity in a PECVD low-*k* film derived from depth profiling with PALS (Reused with permission from Hua-Gen Peng, William E. Frieze, Richard S. Vallery, David W. Gidley, Darren L. Moore, and Richard J. Carter, Applied Physics Letters, 86, 121904 (2005), American Institute of Physics.)

to effectively move the film surface down to the layer with the 3.5 nm pores. PALS then confirmed [37] that these large pores are indeed highly interconnected. This layer of large, interconnected pores is precisely located where SEMATECH observed trench wall bowing and voids when they etched 350 nm deep trenches into this dielectric [38]. This integration damage is almost certainly caused by the open pore structure hidden deep in the film.

Depth-profiling of films using beam-based PALS is a critically important aspect of PAS characterization. It is fundamental to deducing pore interconnection length and searching for and revealing hidden inhomogeneities in pore morphology. It will prove to be vitally important in studies of integration processing effects on porous dielectric films and correlating changes in electrical properties with porous structure.

Pore shape and growth

Developing an understanding of how pores grow in films and their resulting structure is critical for the implementation of controlled pore design. For instance, the chemical role that functional groups of the porogen play in guiding the aggregation of porogen domains in the matrix material is not always clear and may have unexpected results. Straightforward imaging, if possible, provides only a basic understanding of the shape of the pores. Other traditional techniques of studying interconnected pores in thin films rely on the film being percolated, i.e., the pores will completely penetrate the films. However, studies of pore structure and evolution in the pre-percolation regime, where there is finite pore clustering, are more difficult. PALS, with its ability to simultaneously characterize the size and interconnection length of the induced pores as a function of porosity, can be enlightening with regards to the growth of the pores in the film [39]. By studying the evolution of both the pore size and the pore interconnection length one can begin to deduce the shape of the pores and delineate the relative strength of the porogen–porogen interaction with respect to the porogen–matrix interaction.

A recent study of the growth of pores in the pre-percolation regime was made by using PALS on films with several cyclodextrin (CD) and calixarene (CA) porogens with various functional groups in a modified MSQ host matrix [40, 41]. Results for the pore diameter and L_{int} for films prepared with tCD (CD with methoxyl functional groups) sCD (CD with trimethoxysilyl functional groups) and CA are shown in Figure 3.10. The sCD porogen system produces pores with constant Ps lifetime (hence constant mean free path), but with interconnection lengths much longer than the pore size for all porosities. To have interconnected pores at the lowest porogen loading fraction implies that pores are templated from at least several interconnected porogen molecules. As the loading fraction is increased, the pore diameter remains *constant* while the interconnection length continues to *increase*. Therefore, rather than aggregating in three dimensions, where the pore diameter would be expected to increase, the pores grow linearly. Apparently the trimethoxysilyl functional groups of sCD are such that they can form Si–O–Si linkages after hydrolysis into silanol groups, and therefore covalently bonded linear chains of sCD molecules are readily formed, producing longer (more interconnected) pores of constant cross section. This growth in the cylindrical (or tubular) length is strikingly clear in Figure 3.10.

In the tCD system the methoxyl functional groups are known to have a weaker van der Waals interaction, so the aggregation of the porogen domains is expected to be more three-dimensional and random. As seen in Figure 3.10 at low porosity (≤8%) the pores are isolated

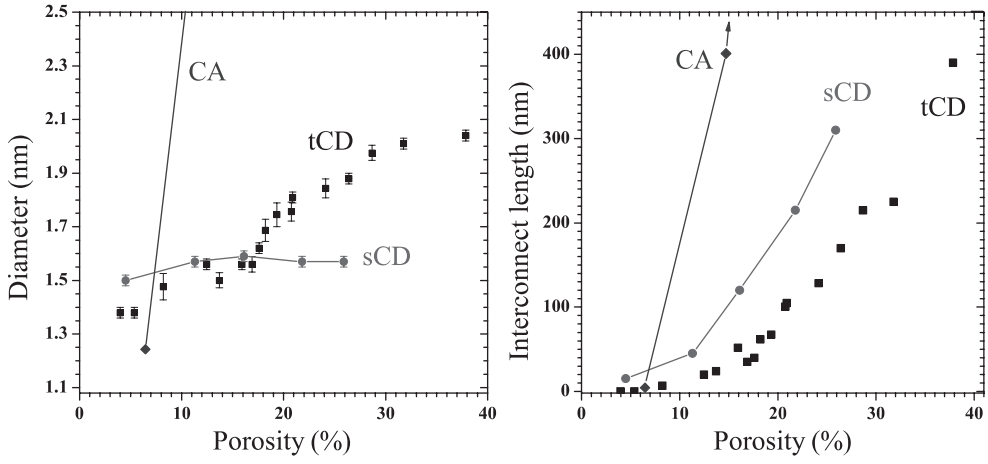

Figure 3.10 Plots of pore diameter (left) and pore interconnection length (right) as a function of porosity for MSSQ films made with three different porogens. The growth modes for the porogens are dramatically different (Reused with permission from Hua-Gen Peng, Richard S. Vallery, Ming Liu, William E. Frieze, David W. Gidley, Jin-Heong Yim, Hyun Dam Jeong and Jongim Kim, *Applied Physics Letters*, 86, 121904 (2005), American Institute of Physics)

with a diameter consistent with a template of a tCD molecule. They then gradually increase in pore size and interconnection length as the porosity is increased. This trend is consistent with uniform random population of pores in the matrix, which leads to three-dimensional growth of the pores. The CA system is unique in that PALS shows explosive growth between 7 and 15% porosity. The pore diameter jump drastically from a closed-pore diameter of ~1.2 nm, consistent with the size of the templated molecule, to an effectively percolated pore with a diameter of 3.5 nm. Therefore CA, being amphiphilic, appears to act like a surfactant, which should promote large micelle growth beyond some critical concentration.

These results nicely demonstrate three different porogen aggregation modes with concentration to create nanoporosity—from isolated pores to interconnected network. It is a key demonstration of the usefulness of PALS in untangling the fundamental pore structure and its evolution in porosity. Such results provide critical feedback to chemists designing the functional group chemistry that will *control* the pore structure. PALS results are monitoring the role of functional groups on the CDs and CAs in determining the resulting pore structure evolution (size and interconnection length) vs porosity.

3.2.5 Future improvements in PAS capabilities

As a research tool for pore characterization PAS, and PALS in particular, offers many attractive porosimetry features with no apparent limitations through the 22 nm technology node. There is no practical limit (~0.2–0.3 nm diameter) on the minimum pore size. Pore interconnection lengths can be deduced and pore size distributions can be fitted, even if the dielectric layer is buried under a diffusion barrier. Lateral resolution of several millimeters is typical as is the depth resolution of about 10 nanometers. The positron beam and spec-

trometer are compact, uncomplicated devices with rather straightforward analysis methodology. Radiation damage to the film is negligible—the technique is nondestructive, except that samples are presently cut to centimeter size from wafers. Cutting wafers and acquiring data for 30 min–1 h are quite acceptable nuisances in a materials research laboratory environment, given the valuable information derived.

Near-term improvements in PALS are expected to address three issues: positron rate, lateral resolution, and sample size. The goal is to develop the capability to perform PALS:

1. On a 1-mm diameter spot;
2. Located on a full 300 mm wafer;
3. In 10 s acquisition and analysis time.

To develop the capability to achieve these goals an intense positron beam is under construction at the North Carolina State University Pulstar Nuclear Reactor in Raleigh, NC [42]. This positron beam based on pair-production in the intense gamma flux near the reactor core is designed to be the centerpiece of a national center for nanoporosity characterization, including the latest generation of PALS spectrometers for depth-profiled dielectric film characterization. A prototype beam has already achieved 3×10^7 positrons/s [42], two orders of magnitude more intense that typical lab-scale beams currently in use. The full-scale beam should deliver a factor of 100 higher rate, insuring sufficient beam to explore the *maximum* data rate in PALS fast-coincidence timing (limited by timing system deadtime) while focusing and limiting the beam to ~1 mm diameter. The PALS spectrometer positron optics has been designed to test small-spot analysis on a full wafer. This facility within the Nuclear Engineering Department at NCSU should allow fast, convenient, and inexpensive access to PALS/PAS analysis and expertise for materials researchers and engineers in both industry and academia.

Achieving the three PALS performance goals listed above using a nuclear-reactor-based intense positron beam, while providing unprecedented access to the technique, would appear to eliminate the advantage of a lab-scale beam with commercial potential and perhaps the potential for process control in mass manufacturing. This conclusion is not necessarily true. At least one company is pursuing commercialization of a lab-scale positron beam-PALS [43] spectrometer that should also come quite close to achieving these three goals [44, 45]. If such a beam is developed, companies and institutions can then decide whether they desire their own in-house PALS device, comparable to purchasing an electron microscope. With its fast turn-around this compact device would also open up the question of whether PALS is compatible/suitable for in-line mass manufacturing process control. It is not yet clear that porosimetry in general is a critical metrology in production [46], but a compact, fast-turnaround, non-destructive, vacuum-compatible pore characterization tool such as this should not be excluded from consideration.

3.2.6 Conclusion

Beam-based PALS is a powerful porosimetry technique with broad applicability in characterizing low-*k* films. Pore sizes in the 0.3–30 nm range are derived directly from fitted

Ps lifetimes. Plausible distributions of pores can also be determined. Depth profiling of films with PALS has proven to be an ideal way to measure the interconnection length of mesopores, allows us to search for inhomogeneities in the pore structure in low-*k* films, and is capable of exploring porosity hidden beneath dense layers, capping layers, and diffusion barriers. PALS has demonstrated its usefulness in characterization of multilayer films with a complex pore structure and in investigating the evolution of pore shape and structure with porosity.

Positron researchers are continuously working to improve PALS and PAS techniques to have a broad impact in the development of future low-*k* films. While the current PALS technique is sufficient to support the microelectronics industry through the 22 nm technology node, these improvements will extend the capabilities of the technique. A reactor-based PALS nanophase characterization facility is under construction which will ultimately have a factor of 100 higher data rate that will permit a spectrum to be acquired on a sample in 10 s. In addition we are working toward implementing the capacity to study whole 300 mm wafers, reducing the spot size of the beam for improved lateral resolution, and increasing the depth range we are able to study. The impact of PALS is not limited to low-*k* dielectric films. The technique has proven to be useful in studying hardmask materials, SiN and SiC barriers, photoresists, and should be useful in exploring a wide range of porous materials and barriers.

Acknowledgments

We would like to thank Robert Miller and Qinghuang Lin of IBM, Richard Carter of LSI Logic, Todd Ryan of AMD, Jin-heong Yim of SAIT, and Ayman Hawari of NCSU for their collaborations. The continuing support of the Low-*k* Dielectric Program of Sematech International is gratefully acknowledged. We thank other members of the Michigan Positron Group, Mark Skalsey, Ming Liu, and William Frieze for dedicated support.

3.3 STRUCTURE CHARACTERIZATION OF NANOPOROUS INTERLEVEL DIELECTRIC THIN FILMS WITH X-RAY AND NEUTRON RADIATION*

Christopher L. Soles, Hae-Jeong Lee, Bryan D. Vogt, Eric K. Lin, and Wen-li Wu

3.3.1 Introduction

The structure characterization of nanoporous interlevel dielectric (ILD) thin films is challenging because of the small sample volumes and nanometer dimensions of the pores. In this chapter, we review characterization methods for porous ILD materials using X-ray and neutron radiation sources. These methods include X-ray reflectivity (XR), small-angle X-ray scattering (SAXS), small-angle neutron scattering (SANS), and X-ray porosimetry (XRP).

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XRP, in particular, shows promise as a general laboratory characterization method that provides detailed structural information of nanoporous ILD thin films. In XRP, changes in the critical angle for total X-ray reflectance provide a sensitive measure of mass uptake of a condensate into the film. Current porosimetry absorption/desorption models can then be used to determine structure parameters such as porosity and the distribution of pore sizes. Further, XRP data can be used to determine pore structure as a function of depth in non-uniform thin films. Detailed comparisons of XRP results with those from SANS are shown and discussed.

3.3.2 Thin film density by X-ray reflectivity (XR)

High-resolution specular X-ray reflectivity (XR) is a powerful experimental technique to measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and the depth profile of density can be determined with a high degree of precision.

X-ray reflectivity measurements were performed at the specular condition with identical incident and detector angles, θ. In the examples discussed in this chapter, the equipment used was a θ–2θ goniometer with an angular reproducibility of 0.0001°, and a fine-focus copper X-ray tube as the radiation source. The reflected intensity is measured at grazing incidence angles ranging from 0.01 to 2°. The incident beam is conditioned with a four-bounce germanium (220) monochrometer. The beam is further conditioned before the detector with a three-bounce germanium (220) crystal. Conditioning of the beam with these crystals decreases the wavelength spread in comparison to instruments with collimating slits. The resulting beam has a wavelength λ of 1.5406 Å, a wavelength spread $\Delta\lambda/\lambda = 1.3 \times 10^{-4}$, and an angular divergence of 12 arcsec. This instrument has the precision and resolution necessary to observe interference oscillations in the reflectivity data from films up to 1.5 μm thick.

In Figure 3.11, the XR curve is shown for typical porous dielectric film; plotting the logarithm of the reflected intensity (I/I_o) as a function of q (where $q = 4\pi/\lambda \sin\theta$). At low q values, the X-ray beam is completely reflected from the film surface ($I/I_o = 1$). As q

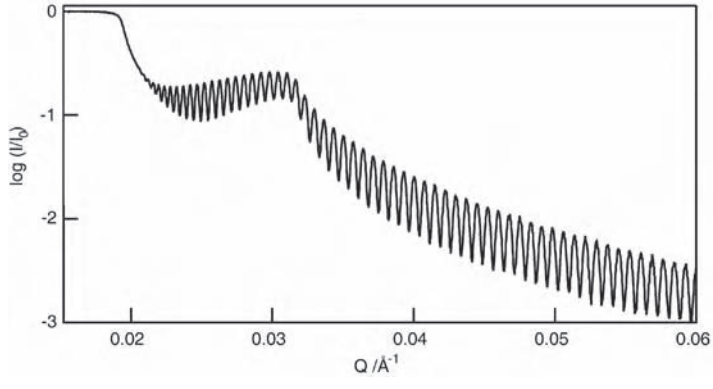

Figure 3.11 X-ray reflectivity profile from a typical low-*k* film

increases, the reflectivity dramatically drops at two separate critical angles θ_c, the first at approximately $q = 0.019\,\text{Å}^{-1}$ and the second at approximately $q = 0.03\,\text{Å}^{-1}$. Each value of θ_c is related to the electron density of different layers in the sample. The critical angle is defined as the grazing angles below which total reflectance of an X-ray beam occurs. This critical angle, θ_c, depends upon the electron density ρ_e (and thus mass density) of the film through:

$$\theta_c = \lambda(\rho_e r_e/\pi)^{0.5} \tag{1}$$

where λ is the X-ray wavelength and r_e is the classical electron radius. In Figure 3.11, the first critical angle at $q \simeq 0.019\,\text{Å}^{-1}$ arises from the electron density of the porous thin film and the second critical angle arises from the silicon substrate electron density. The oscillations that appear in the reflectivity curve between these two critical angles arise from a waveguiding mode that is very sensitive to both the thickness and electron density depth profile of the film. Given the elemental composition, the average electron density of the porous thin film can be converted into an average mass density of the film. The average mass density of the film in Figure 3.11 is $0.87 \pm 0.01\,\text{g/cm}^3$, this includes contributions from both the matrix and the voids. The porosity and matrix density of the film are directly related to this average density (ρ_{avg}):

$$\rho_{avg} = \rho_w(1 - P) \tag{2}$$

where ρ_w is the density of the matrix or wall material and P is the porosity of the film. At this point, an assumption of the matrix mass density can provide a numerical estimate of the film porosity. However, no information about the pore size can be obtained from this single XR measurement.

In addition to the average mass density of the film, the film thickness can be determined from more detailed analysis of the reflectivity data or through the periodicity of the oscillations in the reflectivity profile. The oscillations beyond the critical edge of silicon ($q > 0.03\ \text{Å}^{-1}$) result from the destructive and constructive interference of the X-rays reflected from both the air/film interface and the film/silicon interface. The electron density depth profile of the porous thin film can be determined by fitting the reflectivity data with a model profile. The model profile consists of several layers described by their thickness, electron density, and roughness. In the case of the data in Figure 3.11, the reflectivity can be described by two layers corresponding to the porous film and the silicon substrate. From this electron density profile, the X-ray reflectivity profile is calculated using established methods [47]. The individual layer thicknesses, electron densities, and roughnesses are then numerically varied to minimize deviations between the model reflectivity calculation and the reflectivity data. However, this model profile is not a unique solution because of lost phase information. In contrast, the thickness of the film can be uniquely determined from the periodicity of the reflectivity data. At higher q values, the oscillations in the reflectivity curve are generally free of multiple scattering contributions and a Fourier transform enables a model free determination of the film thickness [47]. The film thickness in Figure 3.11 is determined to be (7530 ± 10) Å, independent of the method used to extract the thickness: Fourier transform or model fitting. This sensitivity to thickness, for example, enables the measurement of the coefficient of thermal expansion (CTE) of very thin films by measuring the film thickness at different temperatures.

3.3.3 Small angle X-ray/neutron scattering

A single XR measurement of a porous dielectric film yields the average film density, but the porosity of the film cannot be determined without assuming the matrix density. This assumption can be avoided by obtaining another measurable quantity also related to both the porosity P and matrix density, ρ_w. One complementary experimental technique that fulfills this requirement is small-angle neutron scattering (SANS), which has been applied in transmission to thin porous dielectric films [6]. With two measurements that depend on ρ_w and P in different functional forms from XR and SANS, one can solve for the values of ρ_w and P experimentally.

SANS results provide information related to the pore size because the SANS intensity is sensitive to density fluctuation correlations. Neutron scattering is not practical in the long term for characterization of porous film due to the limited number of neutron sources. Similar to neutron scattering, small-angle X-ray scattering (SAXS) with a wavelength less than 0.1 nm can also be used to provide the same structure information. The short wavelength is needed because the X-ray energy is such that transmission experiments through silicon wafers are possible. The physics describing the scattering from SANS and SAXS is identical, but there are differences in the details. In particular, silicon is virtually transparent to neutrons and a stack of more than ten low-k films supported on silicon substrate is often used in SANS in order to increase the scattering volume and the neutron scattering signal. In contrast, X-rays have limited penetration power through silicon due to a significant absorbance and a single film is used for SAXS. The small scattering volume, weak scattering of most porous dielectrics for ILDs, and high absorbance of the silicon necessitates a high intensity X-ray source. At present, a synchrotron source is needed to obtain a large enough flux for transmission SAXS measurements with sufficient signal. Another X-ray scattering alternative is grazing incident small angle X-ray scattering (GISAXS). In a GISAXS measurement, the scattering volume can be increased by two orders of magnitude over the normal incident geometry.

3.3.4 Pore wall density and pore structure

Many of the porous films for the low-k application consist of a solid film with a high volume of randomly packed nanopores. A model to describe the scattered intensity from such a structure was introduced by Debye *et al.* [48] $\gamma(r) = \exp(-r/\xi)$ where ξ is the correlation length. The average dimension, or the chord length, of the pores is $\xi/(1-P)$, and the average dimension of the wall between the pores is ξ/P. The scattering intensity based on this model is:

$$I(q) = \frac{8\pi P(1-P)\Delta\rho_n^2\xi^3}{\left(1+q^2\xi^2\right)^2} \tag{3}$$

where $\Delta\rho_n$ is the neutron scattering length contrast or the electron density difference between two phases for SANS and SAXS, respectively. For porous uniform film, this value is simply the neutron scattering length or the electron density of the matrix material between the pores because the scattering length of the pores (voids) is zero. This quantity is linearly

related to the mass density of the matrix and the proportionality constant can be easily determined, provided the atomic composition of the sample is known. Besides the Debye random two-phase model presented by Equation three, there are many other structure models depending on the sample morphology. This equation requires that both the SAXS or SANS intensity must on an absolute intensity scale to measure the pore structure quantitatively. Figure 3.12 shows SAXS and SANS data from a methylsilsesqioxane (MSQ)-based nanoporous film that was fitted with a polydisperse hard-sphere (PHS) model. The general shapes of these two scattering results are similar to each other whereas the intensity scales are very different; the X-ray intensity scale is more than an order of magnitude greater than that of the neutron intensity. Despite the large difference in absolute intensity between the SAXS and SANS results, the structural parameters are in relatively good agreement as shown in Table 3.1.

Depending upon the type of porous material, SAXS and SANS data may not necessarily yield identical structure information from the same scattering model. The SAXS and SANS results are equivalent only under the condition that the porous material can be modeled with a two-phase structure, i.e., a void phase and a matrix phase. When the matrix is not homogenous, e.g., if hydrogen is preferentially located at the surface of the void, the contrast

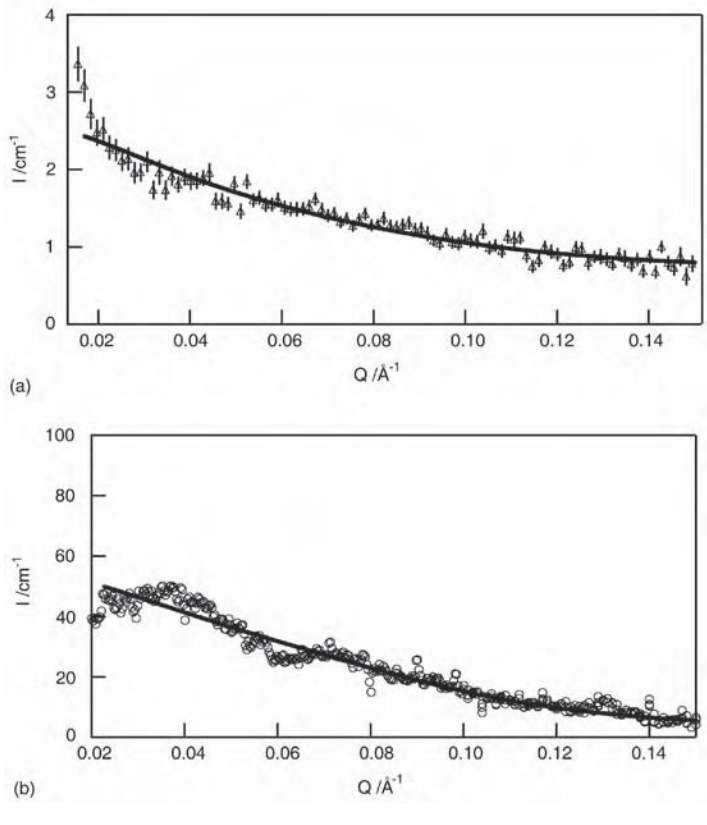

Figure 3.12 (a) SANS results of a MSQ-based nanoporous film supported on silicon wafer; (b) SAXS results of the same MSQ based nanoporous film. The shape of the scattering is similar between SAXS and SANS, but the absolute magnitude of the scattering is not of the same order

Table 3.1 Structure information of a MSQ-based nanoporous film reduced from SANS and SAXS results. Result from X-ray reflectivity (XR) was used complementally to determine the structure results

SANS					SAXS			
Fitting model	Film density from XR (g/cm^3)	Wall density (g/cm^3)	Porosity (%)	Pore diameter (Å)	Fitting model	Wall density (g/cm^3)	Porosity (%)	Pore diameter (Å)
PHS	0.965	1.568	38.4	20.3	PHS	1.48	34.6	29.6

factors for X-rays and neutrons can change and yield different structure parameters. Hydrogen is a special case because of the very different scattering cross-section for neutrons. For this case, a three-phase model was developed to accommodate this type of structure [49]. Direct observations of a heterogeneous matrix in nanoporous films have been made with contrast match SANS [5].

For many nanoporous film applications, well-defined and ordered pores are advantageous [50]. Of particular interest has been the evolution of new mesoporous materials created using sacrificial templates since the discovery of MCM-41 [51]. (MCM-41 (Mobile Crystalline Material) is an ordered mesoporous material, displaying a honeycomb-like structure of uniform mesopores (3 nm in diameter) running through a matrix of amporphous silica.) The pore size and space group of these materials can be controlled through the choice of self-assembling template material [52] for a variety of metal oxide frameworks [53]. Slight modification of this versatile approach has been used successfully to create mesoporous films with regular packed pores [54].

To control pore orientation, methods have been developed for the directed growth of orientated mesoporous films from solution [55]. The orientation of these self-assembled nanostructured materials is similar to those observed in block copolymer films [56, 57]. Due to preferential wetting of a component of the templating agent to the free surface and/or substrate [58], film interfaces provide local orientation sites [54]. The depth of the orientation is typically determined from cross-sectional scanning electron microscopy (SEM) or transmission electron microscopy (TEM) images [59]. XR has been applied successfully to determine the depth of this surface orientation and SANS has been used to determine the packing order of the voids [60].

An alternative to transmission SAXS measurement is GISAXS. Unlike transmission SAXS, which requires a high-intensity, low-wavelength X-ray source, the GISAXS geometry, where the scattering signal is collected at the thin-film side, can increase the scattering volume by two orders of magnitude. The X-ray beam does not penetrate the silicon substrate, but is reflected from the surface. Consequently, X-rays from a typical copper source can be used for this measurement. Experimental techniques have been developed and demonstrate the capability of collecting GISAXS data within a time period less than 60 s. However, the quantitative analysis of GISAXS data remains a challenge because of the difficulty in decoupling the scattering intensity from both the nanopores and the surface/interface roughness. Before this difficulty in GISAXS data analysis is resolved, either transmission SAXS or SANS must be used for quantitative structure characterization, particularly for ordered structures.

The difficulty in obtaining access to SAXS and SANS sources for ILD porous dielectrics has led to a need for more accessible methods for the determination of both the porosity and matrix density. One potential solution to this issue is XRP.

3.3.5 X-ray porosimetry

The characterization of bulk porous materials, porosimetry, is a well-established field. Both total porosity and pore size distribution are determined by measuring the pressure dependence of liquid or gas infiltration into the porous materials [61, 62]. There are several techniques, such as gas adsorption, mercury intrusion, mass uptake, and others, capable of characterizing pores significantly smaller than 100 nm. However, these methods lack the sensitivity to quantify porosity in thin porous ILD that are typically several hundred nanometers thick. The film mass is less than a few milligrams, meaning that the usual observables (i.e., pressure drop in a gas adsorption experiment or mass in an gravimetric experiment) exhibit exceedingly small changes as the pores are filled with a condensate. The porosimetry of thin ILD films requires measurement probes of condensate infusion with extraordinary sensitivity.

EP [3, 4] was developed to address this need. EP measures the refractive index and thickness of the film before and after being filled by condensate. Monitoring the amount of adsorbed condensate as a function of the partial pressure defines a physisorption isotherm, the basic starting point for any number of analytical interpretations. However, to deduce porosity from the refractive index, approximations such as additive polarizabilities are required. This porosimetry measurement can be improved by avoiding these assumptions and approximations.

XRP is very similar to EP, but the film density is directly measured from the critical angle, provided the film composition is known [63]. Exposing the film to a partial pressure of condensable vapors changes the film density profile and potentially the film thickness, both of which are measured independently with XR. The change in film density can be directly related to the amount of adsorbed condensate, and thus porosity, if the density of the condensed fluid is known or assumed to be bulk-like. XRP directly measures the average porosity, average film density, and average wall density of the material separating the pores. The average pore size and pore size distribution from the physisorption isotherm can be determined using existing porosimetry models. In addition, XRP is also capable of providing depth-resolved information on pore size distribution. The depth resolution is typically within a few nanometers.

Porosimetry fundamentals

Traditional forms of adsorption porosimetry rely upon weight gain due to the surface adsorption and/or condensation of vapor inside the porous media. The current status of the porosimetry field can be found in a number of texts [61, 62, 64]. Today, the most common form of porosimetry is the nitrogen physisorption isotherm and serves as a useful model for porosimetry concepts. In these experiments, the porous sample, usually a powder, is sealed in a vessel of fixed volume, evacuated, and cooled to liquid N_2 temperatures. The sample vessel is then dosed with a fixed volume of pure N_2 gas. The fixed volume of the

vessel combined with the known volume of gas defines the pressure. However, at low dosing pressures some of the N_2 condenses on the surface of the sample, resulting in a reduction of the 'predicted' partial pressure that can be measured with an accurate pressure transducer. By knowing the initial and final dosing pressures in the fixed volumes, the amount of adsorbed N_2 onto the pore surfaces can be calculated.

At higher partial pressures, after a few monolayers of the gas adsorb onto the pore walls, N_2 begins to condense inside the smallest pores, even though the vapor pressure in the system may be less than the liquid equilibrium vapor pressure. Zsigmondy [65] was the first to illustrate this effect and describe the process, using concepts originally proposed by Thompson (Lord Kelvin), as capillary condensation [66]. The classic Kelvin equation relates the critical radius for this capillary condensation r_c, to the partial pressure P, equilibrium vapor pressure P_0, liquid surface tension γ, and molar volume V_m through:

$$r_c = \frac{2V_m\gamma}{-RT}\frac{1}{\ln(P/P_0)} \tag{4}$$

where T is the temperature and R is the universal gas constant. This relationship demonstrates that the critical pore size for capillary condensation increases with the partial pressure, until the equilibrium vapor pressure of liquid N_2 is achieved and r_c approaches infinity; the vapor spontaneously condenses. In the porosimetry apparatus, capillary condensation leads to a noticeable pressure drop that can also be converted into the amount of adsorbed vapor. A more detailed description of these physiosorption isotherms can be found elsewhere [61, 62, 64].

These measurements become exceedingly difficult in thin, low-k dielectric films where there is limited sample mass. A typical low-k dielectric film is approximately 500 nm thick, with an average density of 1 g/cm^3 and a porosity of approximately 50% by volume. This means that on a 76.2 mm (3 in) diameter wafer there will be approximately 1×10^{-3} cm^3 of pore volume on top of several grams of Si. Traditional porosimetry techniques lack the sensitivity to register the pressure, mass, or calorimetric changes that occur when condensing such a small amount of vapor; metrologies with higher sensitivity are needed to quantify the porosity in thin low-k dielectric films. It is also desirable that the characterization be *in situ*, on the supporting Si wafer. This obviates sample damage and the errors that result from scraping large quantities of low-k material off multiple wafers, and further retains the possibility of on-line or process control checks in the fabrication or industrial lab settings.

X-ray porosimetry fundamentals

XRP combines specular XR measurements with capillary condensation where the needed sensitivity to mass uptake comes from the accuracy of thin-film density measurements with XR. If the environment surrounding the film is gradually enriched with an organic vapor, such as toluene, the vapor will condense in the pores with the radii commensurate with the critical radii for capillary condensation. This condensation increases the density of the sample. Recall earlier estimates that the density of a low-k film is of the order of 1 g/cm^3 with approximately 50% porosity (implying wall density on the order of 2 g/cm^3). Given that most condensed organic vapors also have densities of the order of 1 g/cm^3, complete

condensation leads to a significant (i.e., of the order of 50%) change in the total film density. This offers a very effective mechanism to monitor the vapor uptake as a function of partial pressure and obtaining physisorption isotherms.

All the above discussions have been focused on the characterization of blank or unpatterned porous ILD films. Upon plasma processing for pattern etching or photoresist ashing the porous structure will often be modified, in most cases densification at the film surface occurs. For some cases, a limited and controlled densification at the sidewall of the patterns is desirable since it may facilitate the deposition of barrier layer on the sidewall. This points to the need of additional metrology to quantify the extent of sidewall densification. Work is in progress to develop metrology to address this type of porous structure measurement need.

Fitting X-ray reflectivity data. A complete analysis of X-ray reflectivity data requires modeling the reduced data using well-established models and procedures. The equations needed to model specular reflectivity data are straightforward [47, 66, 67]. The basic procedure involves constructing a model electron density depth profile consistent with well-known scattering length density parameters for the material or materials of interest, solving a recursion formula for the expected X-ray reflectivity data, then iterating the model profile until a satisfactory fit is obtained with the experimental reflectivity curve. The greatest limitation in the analysis of X-ray reflectivity data is the need for a model profile to fit to the data. There are many different software packages available to fit X-ray reflectivity data using a recursion algorithm [47, 68].

For XRP, it is often sufficient to measure only the critical angle of the sample because changes in the amount of adsorption are proportional to the changes in the sample electron density. For more detailed analysis, it may become necessary to perform full data fits of the XRP reflectivity curves for situations, for example, where the film swell or the pore size distribution is depth dependent. The following sections show how the X-ray reflectivity data can be used to determine important information about the structure of nanoporous thin films.

Interpretation of XRP data. In this section, we illustrate how to interpret and analyze XRP with films from three different classes of porous low-*k* dielectric material. The films are characterized in terms of critical structural information, such as the average film density, average wall material density, porosity, and the pore size distribution. By way of introduction, the first class of material is a hydrogensilsesqioxane (HSQ) film prepared by the evaporation of a high-boiling-point solvent after gelling the HSQ resin [69]. The second is a MSQ film generated through a templated vitrification of low molecular mass siloxane oligomers [70]. The third material is deposited by plasma enhanced chemical vapor deposition (PECVD) from a mixture of an organic precursor (the porogen) and tetramethylcyclotetrasiloxane [71]. This last film will be referred to as porous SiCOH. The reported dielectric constants of the porous HSQ, MSQ, and SiCOH films are 2.20, 1.85 and 2.05, respectively. In light of the nominally similar dielectric constants, we compare and contrast the pore structures in these films because the structure also affects other critical properties such as the mechanical properties of the film. XRP is able to perceive differences in the pore structures of these otherwise similar low-*k* films. Later, the characteristics of the porous films obtain from XRP are also compared with similar data obtained through scattering, specifically SANS/XR techniques [5, 69, 72].

Figure 3.13 displays experimental XR data for the three porous low-*k* films both under vacuum and in the presence toluene-saturated air. The square of this critical angle is pro-

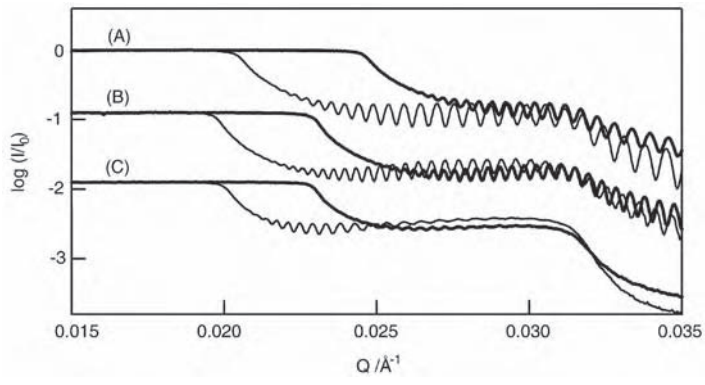

Figure 3.13 SXR curves of (A) porous HSQ, (B) porous MSQ, and (C) porous SiCOH thin films. The curves are offset for clarity. The standard uncertainty in $\log(I/I_0)$ is less than the line width. (Reprinted from *Journal of Applied Physics* **95**(5) 2355 (2004) with permission from the American Institute of Physics)

portional to average electron density of the thin film, as discussed previously through Equation (1), which is then used to calculate the average mass density from the atomic composition. For these films the elemental composition is determined experimentally via ion beam scattering, using the combination of the Rutherford backscattering, forward scattering and forward recoil scattering techniques discussed elsewhere [69, 73].

Comparing the reflectivity curves under vacuum in Figure 3.13 shows that q_c occurs at lower q for the films with lower k, qualitatively indicating that the density of porous thin film decreases with the dielectric constant. It is also clear that q_c shifts to higher q in the presence of the saturated toluene vapor. Capillary condensation of the toluene inside the accessible pores results in an appreciable increase of the density. A larger difference between q_c of the vacuum and the toluene-saturated curves indicates a greater uptake of toluene, and thus a greater porosity. From these two curves, one can calculate the total amount of toluene adsorbed, thus the total porosity P, as well as the density of the wall material ρ_{wall} separating the pores [63]. P and ρ_{wall} can be determined from two simple experiments: reflectivity under dry (evacuated) and toluene saturated environments. This leads to two equations based on a simple rule of mixtures:

$$\rho_{dry} = (1-P)\,\rho_{wall} \tag{5}$$

$$\rho_{sat} = P\rho_{liquid} + (1-P)\rho_{wall} \tag{6}$$

In addition to P and ρ_{wall}, ρ_{dry} is the total average density of the dry (evacuated) film, ρ_{sat} is the average density of the film in the presence of the saturated vapor, and ρ_{liquid} is the density of the condensed liquid. ρ_{dry} and ρ_{sat} are defined by the Q_c^2 values of the reflectivity experiments in the dry and vapor saturated environments, respectively, while ρ_{liquid} is assumed to be bulk-like for this calculation. The elemental composition of the low-k film, the elemental composition of the toluene condensate, and Equation (1) are used to convert the electron densities into mass densities. Knowing ρ_{dry} and ρ_{sat} leaves two equations that can be solved for the remaining two unknowns, P and ρ_{wall}.

It should be noted that Equations (5) and (6) do not account for pores that may be inaccessible to the condensing vapor; such porosity is folded into the average wall density of the material. Pores might not be accessible if they are isolated, unconnected to the surface, too small to accommodate the vapor molecules, or excluded because of an unfavorable surface energy. Our experience with a broad range of low-*k* dielectric materials indicates that toluene is able to access most pores, especially if the matrix (wall) material exhibits swelling in the presence of toluene. Toluene has low polarity and wets most low-*k* materials, which also have low polarity (i.e., low dielectric constant). Notable exceptions, however, include highly fluorinated materials that the toluene will not wet or penetrate the wall material. Solvent vapors other than toluene may be used if pore accessibility becomes an issue.

Equations (5) and (6) do not account for swelling of the low-*k* film by the condensate. XRP is well suited to address swelling because the XR data also provide an accurate measure of film thickness. Using toluene vapor, we rarely see evidence of film swelling greater than 1% in thickness for most nonorganic low-*k* materials. However, this is not the case for polymeric samples that can swell appreciably. In some respects, a small amount of film swelling helps the XRP measurement. If the condensate can gently swell the film, it is reasonable to assume that all pores are accessible because swelling shows that the condensate can diffuse through the wall material and is not dependent upon connected channels to the surface. In the presence of swelling, Equation (6) should be modified such that the porosity is given by:

$$P = \frac{\rho_{\text{sat}} t_{\text{sat}} - \rho_{\text{dry}} t_{\text{dry}}}{\rho_{\text{liquid}} t_{\text{dry}}} - \frac{t_{\text{sat}} - t_{\text{dry}}}{t_{\text{dry}}} \tag{7}$$

where t_{dry} and t_{sat} are the film thickness values of the dry and swollen films. This equation assumes that the volume of liquid toluene is conserved (rule of mixtures) upon absorption into the film and the wall material. Once P is determined, Equation (5) can be used to extract ρ_{wall} for the dry material.

The porosities obtained by this method (no swelling, using Equations 5 and 6) for the porous HSQ, MSQ, and SiCOH films are (46 ± 1)%, (34 ± 1)%, and (31 ± 1)%, respectively. (Certain commercial equipment and materials are identified in this paper in order to specify adequately the experimental procedure; in no case does such identification imply recommendations by the National Institute of Standards and Technology, nor does it imply that the material or equipment identified is necessarily the best available for this purpose.)

The resulting wall densities of the porous HSQ, MSQ, and SiCOH films are (1.83 ± .05) g/cm^3, (1.35 ± .05) g/cm^3 and (1.31 ± .05) g/cm^3, respectively. Notice that the porous HSQ film has the highest porosity, yet its dielectric constant is the largest. This apparent contradiction is resolved through the observation that the porous HSQ film also has highest wall density. It is also interesting that the porous MSQ and SiCOH films have similar average densities, wall densities, and atomic compositions, despite the fact they are prepared from very different techniques. The elemental composition, detailed structural characteristics, and standard uncertainties in the pore characteristics of the samples are summarized in Table 3.2.

The sensitivity and resolution of XR are sufficient to reveal subtle differences between the three films as the toluene atmosphere gradually varies from $P/P_0 = 0$ (dry air) to $P/P_0 = 1$ (toluene saturated) and toluene progressively infiltrates the pores. In terms of the

Table 3.2 A summary of the atomic compositions, dielectric constants k, and structural characteristics of different porous low-k films. The relative standard uncertainties of the atomic compositions Q_c^2, densities, porosities and pore radii are ±2%, 0.05 Å^{-2}, 0.05 g/cm^3, 1%, and 1 Å, respectively

Porous Film	Atomic composition (Si:O:C:H)	k	Q_c^2 ($\times 10^{-4}$ Å^{-1})	ρ_{dry} (g/cm^3)	ρ_{wall} (g/cm^3)	P (%)	Pore radius (Å)	
							XRP	SANS
HSQ	25:48:7:20	2.20	4.25	0.98	1.83	46	13	9
MSQ	15:25:19:41	1.85	3.95	0.89	1.35	34	15	10
SiCOH	10:20:28:42	2.05	4.04	0.91	1.31	31	5	3

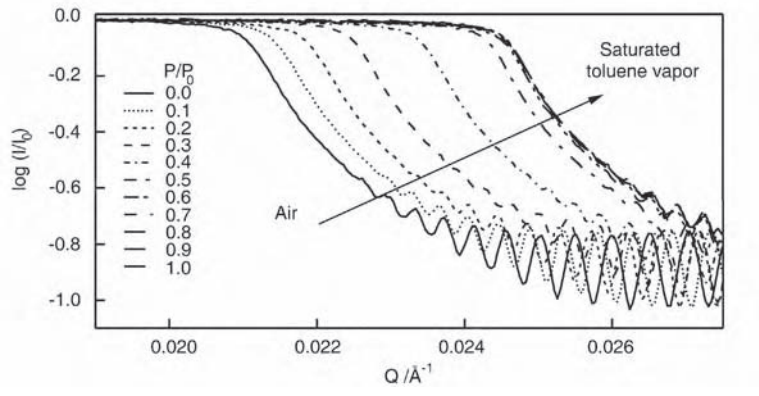

Figure 3.14 Critical angle changes for the porous HSQ sample as P/P_0 increases systematically from 0 (dry air) to 1 (toluene saturated air). Condensation of the toluene inside the pores results in an appreciable and measurable change in q_c^2. Reprinted from X-ray Reflectivity as a Metrology to Charaterize Pores in Low-k Dielectric Films in *ACS Symposium Series 874*: Polymers for Microelectronics and Nanoelectronics. Published 2004 American Chemical Society

reflectivity data, Figure 3.14 illustrates these changes in the porous HSQ film in the region of the q_c. By assuming that the mass density of adsorbed toluene is the same as the bulk fluid, the increase in q_c^2 above the vacuum level can be used to calculate the amount of toluene adsorbed into the film as a function of the relative partial pressure. These data are presented as physisorption isotherms in Figure 3.15.

In Figure 3.15, the porous SiCOH film shows a prominent uptake at low partial pressures that quickly levels off. There is also no hysteresis between the adsorption and desorption branches. This is characteristic of filling micropores (pores less than 2 nm diameter) [61, 62, 64, 74], indicating that the PECVD process generates a large population of small pores. In comparison, the porous MSQ film continues to adsorb over a broad range of larger partial pressures. There is also a pronounced hysteresis between the adsorption and desorption pathways for the porous MSQ film, consistent with the filling of larger mesopores. This indicates that the porogen in the PECVD film forms smaller domains than the spin-cast

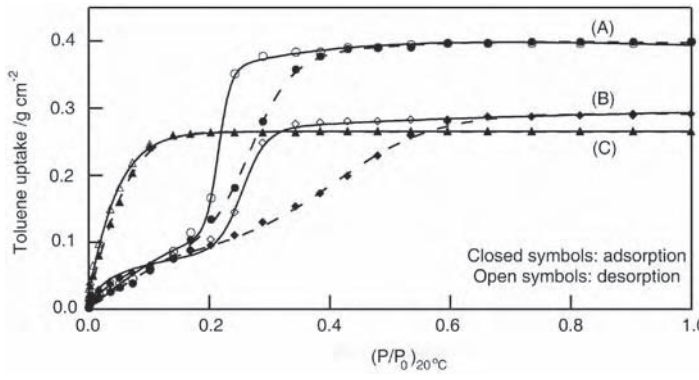

Figure 3.15 Physisorption isotherms for the porous (A) HSQ, (B) MSQ, and (C) SiCOH films. The lines are smooth fits using the cumulative sum of a sigmoidal and a log-normal function for porous HSQ and MSQ films, and the sum of a Gaussian and a sigmoidal function for porous SiCOH, film. (Reprinted from *Journal of Applied Physics* **95**(5) 2355 (2004) with permission from the American Institute of Physics)

MSQ film, leading to smaller pores in the porous SiCOH film. This is striking because the porous SiCOH and MSQ films are otherwise similar in terms of their atomic composition, total porosity, and wall densities; the primary difference is in their pore size distributions (PSDs).

At low partial pressures, the adsorption process in both spin-on-glass (SOG) films (porous HSQ and MSQ films) is gradual at first, but increases steeply at intermediate partial pressures due to capillary condensation in the mesopores. After these mesopores are filled, the adsorption isotherms level off. Note that capillary condensation and evaporation do not take place at the same partial pressures, i.e., there is an appreciable hysteresis. The hysteresis loop in the MSQ film is highly asymmetric (broad on adsorption, narrow on desorption), suggesting that pore connectivity (network) effects are important [75]. If larger pores can be accessed only through neighboring or interconnected narrow pores, the condensate in the larger pores is not free to desorb at the relative pressure corresponding to their critical capillary radius. The smaller pores block the desorption of the solvent from the larger pores in a manner that has been described as the 'ink-bottle' effect [61, 76]. The result is a simultaneous draining of both the small and large mesopores at a partial pressure corresponding to the critical radius of the smaller pores. Hence, the sharper drop in the desorption curve compared with the adsorption branch in Figure 3.15.

By comparing the general shape of the adsorption/desorption isotherms for the three different films, one can qualitatively arrive at the schematic pore structures depicted in Figure 3.16. The PECVD process creates the smallest pores, in very large quantities. The lack of a hysteresis loop confirms that the dimensions of pores are of the order of a few toluene molecules. These pores, as well as all the films studied here, are apparently interconnected since toluene freely diffuses into and out of the structures. The total porosity is, however, greater in the HSQ material, as indicated by the largest total toluene uptake in Figure 3.15. The pores in HSQ are also clearly larger than the PECVD material's pores. Like the pores in porous SiCOH, those in the porous HSQ are fairly uniform in their size distribution, as indicated by the symmetric and relatively narrow hysteresis loop. This is in

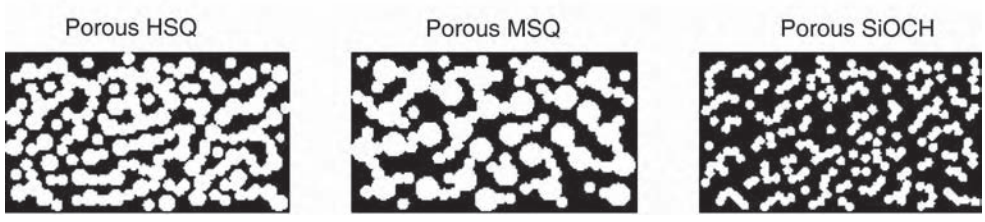

Figure 3.16 Schematic pore structures for the porous HSQ, MSQ, and SiCOH films. (Reprinted from *Journal of Applied Physics* **95**(5) 2355 (2004) with permission from the American Institute of Physics)

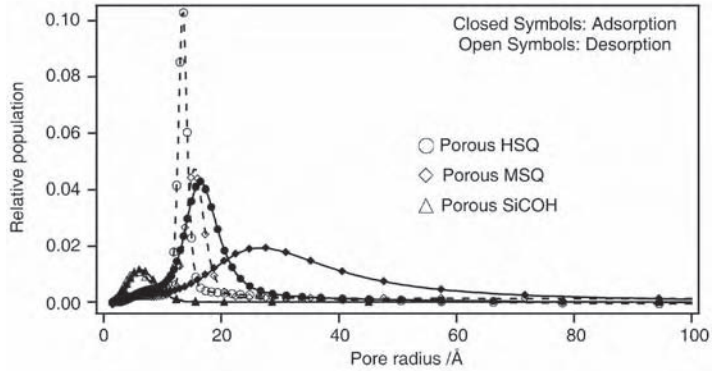

Figure 3.17 Approximate pore size distributions from the smooth fits through the physisorption isotherms in Figure 3.16, using Equation (4) to convert P/P_0 into a pore size. The distributions from the adsorption branch (solid lines) can be significantly broader and shifted to larger pore sizes than the corresponding desorption branch, especially in those materials (such as the MSQ film) with a large distribution of mesopore sizes

contrast to the MSQ film with its very broad pore size distribution and the largest average pore size (despite the lower porosity in comparison to the HSQ film). As discussed above, the sharp desorption branch of the MSQ film in contrast to the broad adsorption pathway indicates that pore blocking effects are significant.

This qualitative description can be quantified using equation to convert the partial pressures for capillary condensation in Figure 3.15 into pore radii. Plotting the relative toluene uptake as a function of the pore size establishes the pore size distribution (PSD). To illustrate this procedure we use the simplest example of the Kelvin equation (Equation 4) to convert P/P_0 into a critical radius for capillary condensation. However, we acknowledge that alternative expressions to Equation (4) are probably more appropriate. The Kelvin equation lacks terms that account for interactions of the condensate with the pore surfaces and is not well suited for situations where the pore size approaches the dimensions of the condensate molecule. Nevertheless, Figure 3.17 shows the resulting pore size distribution, with the total areas beneath the curve scaled to a value consistent with the total P for each film as reported in Table 3.2. It should be noted that the symbols in Figure 3.17 are not measured data; they are generated from the smooth fits in described in the caption of

Figure 3.15. Generally, we find that the increments of P/P_0 in experimental data of Figure 3.15 are not sufficiently fine for a point-by-point differentiation when using a Kelvin equation to generate Figure 3.17; significantly smoother and reasonable distributions are obtained by transforming the arbitrary fit function. As long as the empirical fit accurately parameterizes the physisorption data, this is a reasonable procedure.

In the literature, it is traditional to use the desorption branch of the physisorption isotherm to report the PSDs. The average pore radii in the porous HSQ, MSQ, and SiCOH films taken from the desorption curves in Figure 3.17 are approximately 13, 15, and 5 Å, respectively. However, this average is biased towards the minimum or constricting pore in regard to the ink-bottle effect; a more complete interpretation of the pore structure always results from analyzing both the adsorption and desorption branches. For example, in Figure 3.17 notice that there is a relatively large difference between adsorption and desorption pore size distributions for the MSQ materials. While the average pore radius on desorption was approximately 15 Å, the desorption branch leads to an approximate average pore radius of 27 Å. By contrast, the discrepancy is much less for the HSQ film (~13 Å on desorption and 16 Å on absorption) and nearly the same (no discrepancy) for the SiCOH film. This is consistent with the previous discussion of the isotherms in Figure 3.15 and the schematic pore structures in Figure 3.16.

3.3.6 Comparison of small-angle scattering and X-ray porosimetry

SANS is also capable of quantifying the average pore size in these low-*k* dielectric films, providing a useful comparison for the XRP data. The SANS measurements discussed herein were performed on the NG1 beam line at the National Institute of Standards and Technology Center for Neutron Research. SANS is collected with the sample under vacuum, like the XRP, and shown in Figure 3.18. These scattering curves can be fit with the Debye model (Equation 3) [48] to extract an average pore size. An increase in the scattering intensity corresponds to increase in the pore size and/or porosity. In Figure 3.18, the porous SiCOH

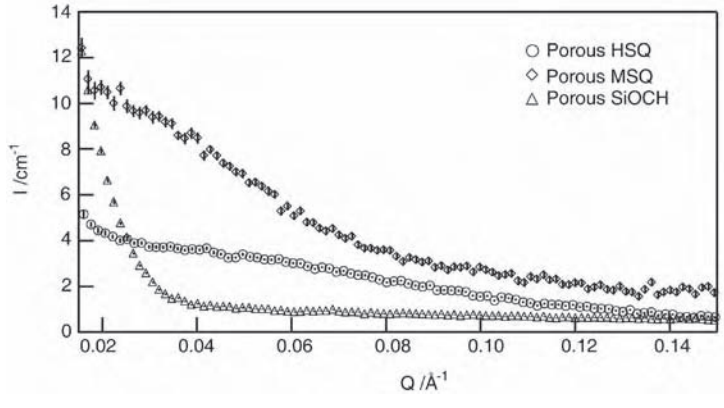

Figure 3.18 SANS data for the porous HSQ (circles), MSQ (diamonds), and SiCOH (triangles) films under vacuum. (Reprinted from *Journal of Applied Physics* **95**(5) 2355 (2004) with permission from the American Institute of Physics)

film shows noticeably weaker scattering than either of the porous SOG films, consistent with the smaller pore size and lower porosity. The greatest scattering intensities occur in the porous MSQ film, which is also consistent with the largest population of larger pores. For the porous HSQ and MSQ films, the Debye model gives reliable fits with average pore radii of 9 and 10 Å, respectively. The radii are comparable to the XRP pore sizes reported in Table 3.2. However, the SANS intensities in the porous SiCOH film are too low to reliably apply the Debye model; the scattering is not strong from this low porosity film. If the Debye model were applied the resulting pore radius would be approximately 3 Å. This result is unphysical in light of the implicit assumption in the Debye model that there is a distinct interface between the pore and the wall material; 3 Å is comparable to a single atomic radius, meaning that the model is not appropriate. Nevertheless, there is reasonably good agreement between the SANS and XRP data for the higher-porosity HSQ and MSQ film. However, we must also mention that there are examples, not reported here, where the SANS and XRP data do not yield consistent data. Recall the discussion above of the oversimplifications of the Kelvin equation; this was chosen as the simplest case example for demonstration. Likewise, analysis of the SANS data with the Debye model suffers from the two-phase approximation where the matrix or wall material is considered to be homogeneous. To a large extent, the agreement between SANS and XRP will depend on the consistency of the models chosen to analyze the pore size distributions.

XRP is a very sensitive form of porosimetry, especially for those materials with very small pores or low porosity supported on thick substrate. This is illustrated with the porous SiCOH film where SANS is unable to reveal the porosity in this film because the pores are too small, below the sensitivity of the technique. However, in Figure 3.13 there is still a very significant change in the raw XRP data as toluene condenses inside the pores.

One distinct advantage of XRP over other forms of porosimetry, including the ellispometric porosimetry technique, is the potential to vertically depth profile the density (and therefore porosity) through the thickness of the film. Recall that the reflectivity data can be fit using a multilayer model. In the preceding examples, the low-*k* films were modeled with a single layer of uniform density, both under vacuum and in the presence of toluene. However, Figure 3.19 shows an example of a low-*k* dielectric film that has a multilayer structure, with different porosities in the different layers. Figure 3.19(a) shows the reflectivity data for this film both under vacuum and in the toluene-saturated environment. The general shape of the reflectivity curves is noticeably different from the preceding examples. In addition to the high-frequency interference fringes that indicate the total film thickness, there are also lower frequency oscillations in the data as roughly indicated the lines and arrows. The low-frequency oscillations are due to a mutlilayer structure. Fitting the reflectivity data requires three distinct layers for the low-*k* film, as shown in Figure 3.19(b). The electron density of the layers as a function of distance into the film (starting from the free surface) is plotted in terms of Q_c^2. Near the free surface (layer 1) the density is noticeably larger than the rest of the low-*k* film, the consequence of a plasma treatment to the surface. The density appears lowest (layer 3) near the Si substrate (the physical origin of the lower density in layer 3 is not understood).

When this multilayer film is exposed to the toluene environment, two effects become obvious. First, the density increases in all three layers of the low-*k* film as toluene condenses in the individual pores. Second, the total film thickness swells by approximately 4.4%, meaning that Equation (7) most be used to extract the porosities. What may be less obvious is that each of the three layers in the low-*k* film absorbs different amounts of toluene.

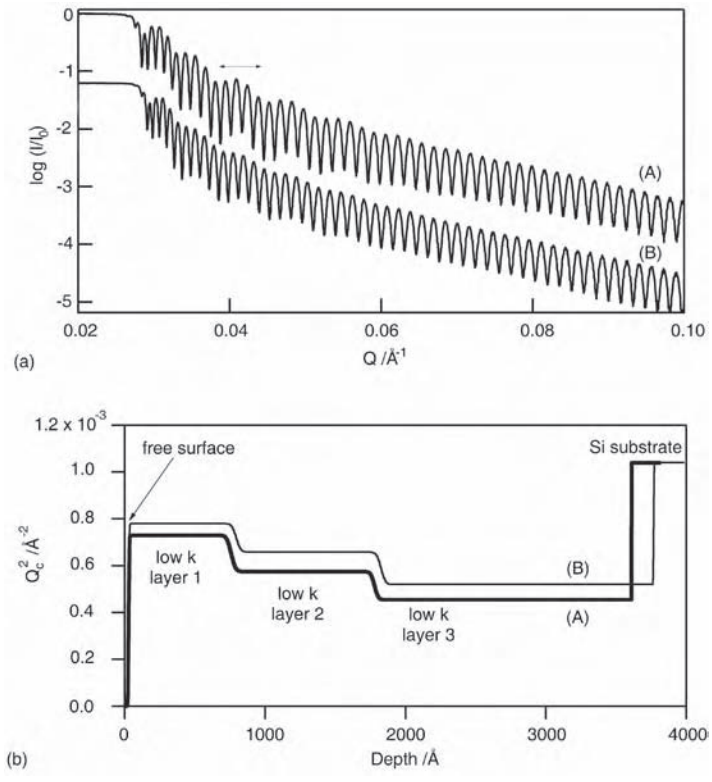

Figure 3.19 XRP data for a low-*k* film comprised of three distinct layers: (a) reflectivity data for the (A) dry and (B) toluene saturated films, revealing both a high-frequency periodicity due to the total film thickness and low-frequency oscillations due to the thinner individual layers; (b) real-space scattering length density profiles a function of distance into the film, revealing the thickness and density of the individual layers

Qualitatively, Figure 3.19(b) shows that layer 2 takes in the most toluene while layer 1 picks up the least. Equation (7) can be used to calculate the porosities in layers 1, 2, and 3 as approximately 13, 21, and 16%, respectively. Despite the lower overall electron density in layer 3, the greatest porosity is found in layer 2. This is because the wall densities are also greater in layer 2, offsetting the porosity effect in terms of the average film density.

3.3.7 Conclusions

The structure characterization of nanoporous interlevel dielectric (ILD) thin films is challenging because of the small sample volumes and nanometer dimensions of the pores. There are few characterization methods for porous ILD materials including PALS, EP, and those utilizing X-ray and neutron radiation sources such as X-ray reflectivity (XR), small angle X-ray scattering (SAXS), small angle neutron scattering (SANS), and X-ray porosimetry (XRP). XRP, in particular, shows promise as a general laboratory characterization method

that provides detailed structural information of nanoporous ILD thin films. In XRP, changes in the critical angle for total X-ray reflectance provide a sensitive measure of mass uptake of a condensate into the film. Current porosimetry absorption/desorption models can then be used to determine structure parameters such as porosity and the distribution of pore sizes. Further, XRP data can be used to determine pore structure as a function of depth in nonuniform thin films.

Acknowledgments

The authors are grateful for support from the Office of Microelectronics Programs at NIST and SEMATECH through its J-105 program.

3.4 ELLIPSOMETRIC POROSIMETRY

Mikhail R. Baklanov

3.4.1 Introduction

In ellipsometric porosimetry, the porosity evaluation is nondestructive and based on analysis of dielectric function that makes the results very suitable for microelectronics [77, 82]. The measurement of effective pore size and porosity is based on penetration and condensation of organic vapor in the pores and allows prediction of behavior of the porous materials during different technological processes including interaction of porous dielectric films with etch, strip, cleaning chemistries, chemical vapor deposition (CVD), etc. Additional advantage of EP is the possibility of evaluation of other properties important for integration such as mechanical properties, hydrophobicity, diffusion barrier, etc.

3.4.2 Fundamentals of ellipsometric porosimetry

The effective dielectric constant k_p of a two-component system depends on dielectric constants of the components k_1 and k_2 and their relative fractions V and $(1 - V)$ (Clausius-Mossotti equation):

$$\frac{k_p - 1}{k_p + 2} = \sum_i \frac{4\pi N_i}{3\varepsilon_0}\alpha_i = V\frac{k_1 - 1}{k_1 + 2} + (1 - V)\frac{k_2 - 1}{k_2 + 2} \tag{1}$$

In the case of porous materials one of the components is air ($k_1 = 1$) and

$$\frac{k_p - 1}{k_p + 2} = (1 - V)\frac{k_s - 1}{k_s + 2} \tag{2}$$

In these equations V is the relative pore volume (V_{pore}/V_{film}), $k_2 = k_s$ is dielectric constant of the film skeleton. N_i and ε_0 are number of molecules per volume unit (density) and

permittivity of vacuum, respectively. Therefore, the film porosity can be calculated if dielectric constants of the porous film and of the film skeleton (dense prototype) are known.

Porosity

The relationship between the optical characteristics and porosity can be described by effective medium approximation. One of such approximations is known as Lorentz–Lorenz equation. This equation is similar to Clausius–Mossotti equation (1) with the only difference that refractive index squared n^2 is used instead of the k value. Indices of refraction n of a nonmagnetic material are linked to the dielectric constant via a relation $\varepsilon = n^2$, which is a rather direct result of the Maxwell equation [1]. If n_s is the refractive index of the film skeleton and n_p is the measured refractive index of the porous film, the relative film porosity V is equal to [4]:

$$V = 1 - \left[\frac{(n_p^2 - 1)}{(n_p^2 + 2)}\right] \Big/ \left[\frac{(n_s^2 - 1)}{(n_s^2 + 2)}\right] \tag{3}$$

If all pores have been filled by a condensed liquid (adsorbate) with known refractive index n_{ads}, the effective index of refraction n_{eff} is given by

$$\frac{n_{eff}^2 - 1}{n_{eff}^2 + 2} = V\frac{n_{ads}^2 - 1}{n_{ads}^2 + 2} + (1 - V)\frac{n_s^2 - 1}{n_s^2 + 2} \tag{4}$$

Subtracting Equation (4) from Equation (3) we get an equation allowing calculation of the volume of the condensed liquid, which is equal to open (accessible) porosity:

$$V = \left(\frac{n_{eff}^2 - 1}{n_{eff}^2 + 2} - \frac{n_p^2 - 1}{n_p^2 + 2}\right) \Big/ \left(\frac{n_{ads}^2 - 1}{n_{ads}^2 + 2}\right) \tag{5}$$

This equation shows that the calculation of the open porosity does not need the value of skeleton refractive index. The parameters needed for calculation are refractive indices of the film with empty pores and pores filled by adsorptive, and the refractive index of the liquid adsorptive. The porosity value V obtained from Equation (5) are used for calculation of the skeleton refractive index in Equations (3) and (4). If the calculated refractive index of skeleton is smaller than the expected values (for instance, in the case of silica or silsesquioxane (SSQ)-based materials the skeleton refractive index is mainly defined by polarisability of Si–O bonds and is equal to 1.45–1.46), the difference reflects the presence of embedded (closed) micropores that are not accessible for the adsorptive.

Pore radius distribution

Calculation of pore radius distribution (PRD) is based on analysis of hysteresis loop that appears due to the difference in the curvature radius of condensed liquid menisci during the adsorption and desorption [4, 62]. The adsorptive vapor condenses in pores at pressure

P lower than the equilibrium pressure of a flat liquid surface P_0. The dependence of the relative pressure (P/P_0) on the meniscus curvature is described by the Kelvin equation:

$$\frac{1}{r_1}+\frac{1}{r_2}=-\frac{RT}{\gamma V_L \cos\theta}\ln\left(\frac{P}{P_0}\right) \tag{6}$$

where γ and V_L are surface tension and molar volume of the liquid adsorptive, respectively. θ is the contact angle of the adsorptive. The principal curvature radii r_1 and r_2 define pore size. Adsorptives with a θ close to 0 are preferable. In the case of cylindrical pores, $r_1 = r_2$ and

$$\left(\frac{1}{r_1}+\frac{1}{r_2}\right)=\frac{2}{r_k} \tag{7}$$

The radius r_k is a dimension characteristic of the capillary and is termed the Kelvin radius. If the radius of a cylindrical pore is r_p, then $r_p = r_k + t$, where t is the thickness of the layer already adsorbed on the pore wall. Values of t are obtained from the adsorption data of the same adsorptive on a nonporous sample having a chemically similar surface and is defined by the BET (Brunauer–Emmet–Teller) equation:

$$t=\frac{d_0 CK(P/P_0)}{[1-K(P/P_0)][1+K(C-1)(P/P_0)]} \tag{8}$$

where d_0 is the thickness of one monolayer, C is the BET constant, K is a coefficient satisfying to the requirement that at $P = P_0$, $t \leq 5$–6 monolayers [62]. Therefore, development of adsorption porosimetry needs the data on molecular characteristics of the adsorptive (molecular volume V_L, surface tension γ), and adsorption characteristics (constant C). The calculated t values are used for correction of the measured pore radius. This procedure is termed *t-correction*.

For *micropores* with width of the order of a few molecular diameters, the Kelvin equation is no longer valid. Not only would the values of the surface tension and the molar volume deviate from those of the bulk liquid adsorptive, but also the concept of a meniscus would eventually become meaningless. The simplest method to determine size and volume of micropores is the *t*-method of de Boer and its extensions [62]. Thermodynamic methods (Dubinin and Radushkevitch [78], Horvath and Kawazoe [79], Saito and Foley [80], etc.) are based on the change of the adsorption potential in micropores and are becoming more popular. To analyze pore size in thin microporous films, EP uses a method based on a theory developed by Dubinin and Radushkevitch (DR) [78, 81]. Adsorption potential A and characteristic adsorption energy E_0 are function of the micropore size and amount of adsorption W at the relative pressure P/P_0:

$$W = W_0 \exp\left[-(A/E)^n\right]$$
$$(n = 2;\ E = \beta E_0;\ A = RT\ln(P_0/P)) \tag{9}$$

Here, W_0 is the micropore volume, β is the affinity coefficient. The linear plot of $\ln W$ versus A^2 leads to W_0 and βE_0. E_0 gives the average pore size $w_0 = K/E_0$ where $K \simeq 12$ is

a coefficient slightly changing with E [62, 81]. The Dubinin–Radushkevitch analysis provides the essentially important parameters on the micropore structure such as the micropore volume and the average pore size. The EP software recognizes presence of misropores in the film by analysis of the adsorption and desorption isotherms and calculates both the mesopore and micropore characteristics such as their relative volume and size.

Specific surface area

Specific surface area is defined as accessible area of a solid surface per unit mass of material. The BET method for calculation of the specific surface area A involves two steps: evaluation of the monolayer capacity n_m from the adsorption isotherm, and conversion of n_m into A by means of the molecular area a_m (surface area occupied by one adsorbate molecule). To obtain a reliable value of n_m from the isotherm it is necessary that the monolayer shall be virtually complete before the build-up of higher layers commences. This requirement is met if the BET constant C is not too low.

This method can be applied in EP. However, in certain cases it is difficult to satisfy the requirement of large enough BET constant. For this reason, EP calculates *cumulative surface area* [62, 82]. The specific surface area of each small group of pores δA_i are calculated from the corresponding pore volume and pore radius as $\delta A_i = \delta V_i / r_i$ *(for cylindrical pores)*. By summing the values of δA_i over the whole pore system a value of the cumulative surface area is obtained.

3.4.3 Porosity characterization by EP

Choice of adsorptive

An important requirement in the adsorption porosimetry is the choice of appropriate adsorptives. Any new adsorptive must be calibrated against nitrogen with the aid of selected reference solids [83]. Among organic adsorptives for room-temperature porosimetry, benzene and toluene have been recognized as probes providing the best agreement with nitrogen porosimetry. Comparative evaluation of different porous films using conventional nitrogen porosimetry and EP supports this conclusion [11]. The simplest way to examine the adsorptive applicability is the so-called Gurvitsch test that is carried out using the same experimental tool. The idea of the Gurvitsch rule [84] is that the volume of a condensed liquid must be the same for all applicable adsorptives in a given porous solid. The pore size determined with different adsorptives must also be the same.

Data collection

The initial experimental data used for the calculation of thickness, refractive index, adsorption isotherms and pore radius are ellipsometric (polarisation) angles, Δ and Ψ [85]. These values are defined by a complex ratio ρ of the reflection coefficients R_p and R_s of light polarized respectively parallel and perpendicular to the plane of incidence on the sample, as

$$\rho = R_p/R_s = \tan\Psi \exp(i\Delta) \tag{10}$$

The EP software calculates the change of the film thickness and refractive index of the film during the adsorption/desorption cycle, PRD and cumulative surface area directly from the change of Δ and Ψ. Molecular characteristics necessary for the calculations have also been investigated for a number of suitable adsorptives.

In situ ellipsometric measurements are performed using a high-vacuum system designed for this purpose (Figure 3.20). The standard EP setup consists of an *in situ* spectroscopic ellipsometer (λ = 350–850 nm), a dry pumping system, pressure gauge (P) and sources of liquid adsorptives. The vacuum chamber is pumped down before an adsorptive is introduced into the chamber. Vapor of an organic adsorptive (toluene is standard) is introduced into the vacuum chamber using a precise and controllable valve (1). This step must be done as slowly as necessary to provide equilibrium between the adsorbed and the gas phase. The same requirement is applied during the desorption. For this purpose the system has an additional controllable valve in the bypass line (2). The measurement time depends on the

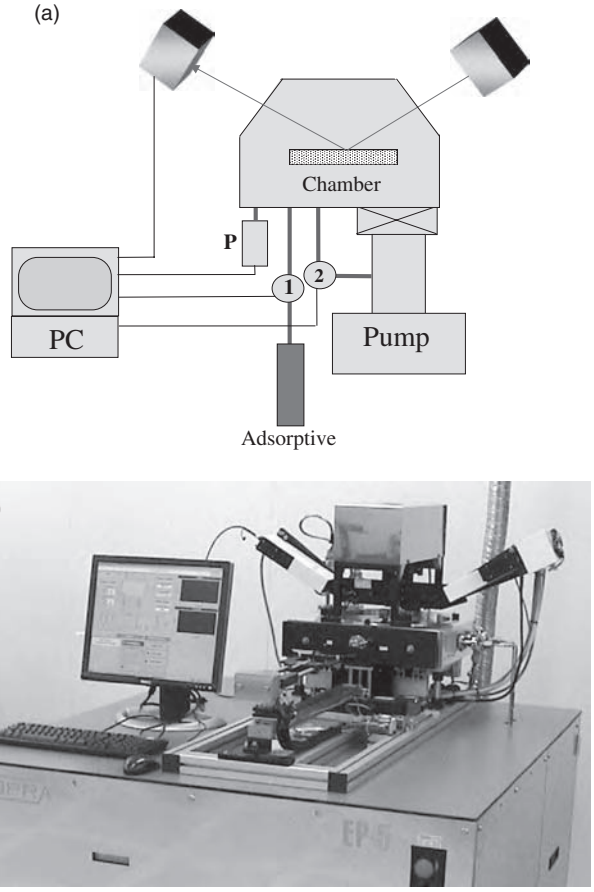

Figure 3.20 (a) Schematic of the IMEC ellipsometric porosimeter (Reproduced with permission from [4], Copyright (2004) American Institute of Physics.); (b) EP-5 developed by SOPRA

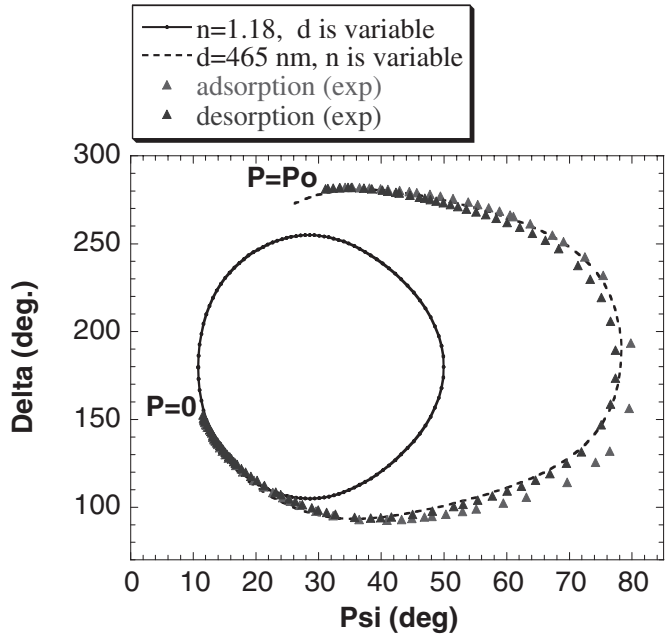

Figure 3.21 Change of ellipsometric angles Δ and Ψ during adsorption and desorption of the toluene vapor in 465-nm-thick mesoporous xerogel film with initial refractive index 1.18 at $\lambda = 633$ nm. (Reproduced with permission from [4], Copyright (2004) American Institute of Physics.)

pore size and the film thickness. For most of porous low-k films with pore size larger than 1 nm and thickness below 1 μm, the measurement time is about 1 h. In some cases, when the range of pore size is known and limited, a 'fast mode' may be used. The measurement time in the fast mode is about 10 min. A semiautomatic tool developed by SOPRA allows operating with small samples and wafers up to 300 mm and also equipped by video camera allowing visualize specific behavior of killer-pores during the adsorption (Figure 3.20b).

Figure 3.21 shows the typical behavior of the ellipsometric angles Δ and Ψ during the toluene vapor adsorption and desorption in a mesoporous 465-nm-thick xerogel film with initial refractive index 1.18. The initial point corresponds to the vacuum ($P = 10^{-6}$ Torr) and the final one to the relative pressure equal to unity ($P = P_0$, $P_0 \simeq 25$ Torr for toluene). All experimental data are well described by a model using the change of refractive index without change of the film thickness. Further analysis of these data gives open porosity equal to 60% and pore radius 4.5 nm. The open porosity is equal to the total porosity calculated using Equation (3). Therefore all the pores are interconnected.

Porosity and pore size distribution

Figure 3.22 demonstrates typical adsorption/desorption isotherms, pore radius distribution and SEM images of low-k dielectric films developed for microelectronic application.

Figure 3.22(a) shows results of porosity evaluation in a CVD low-k film with open porosity equal to 30%. The adsorption/desorption isotherms do not have hysteresis loop, which

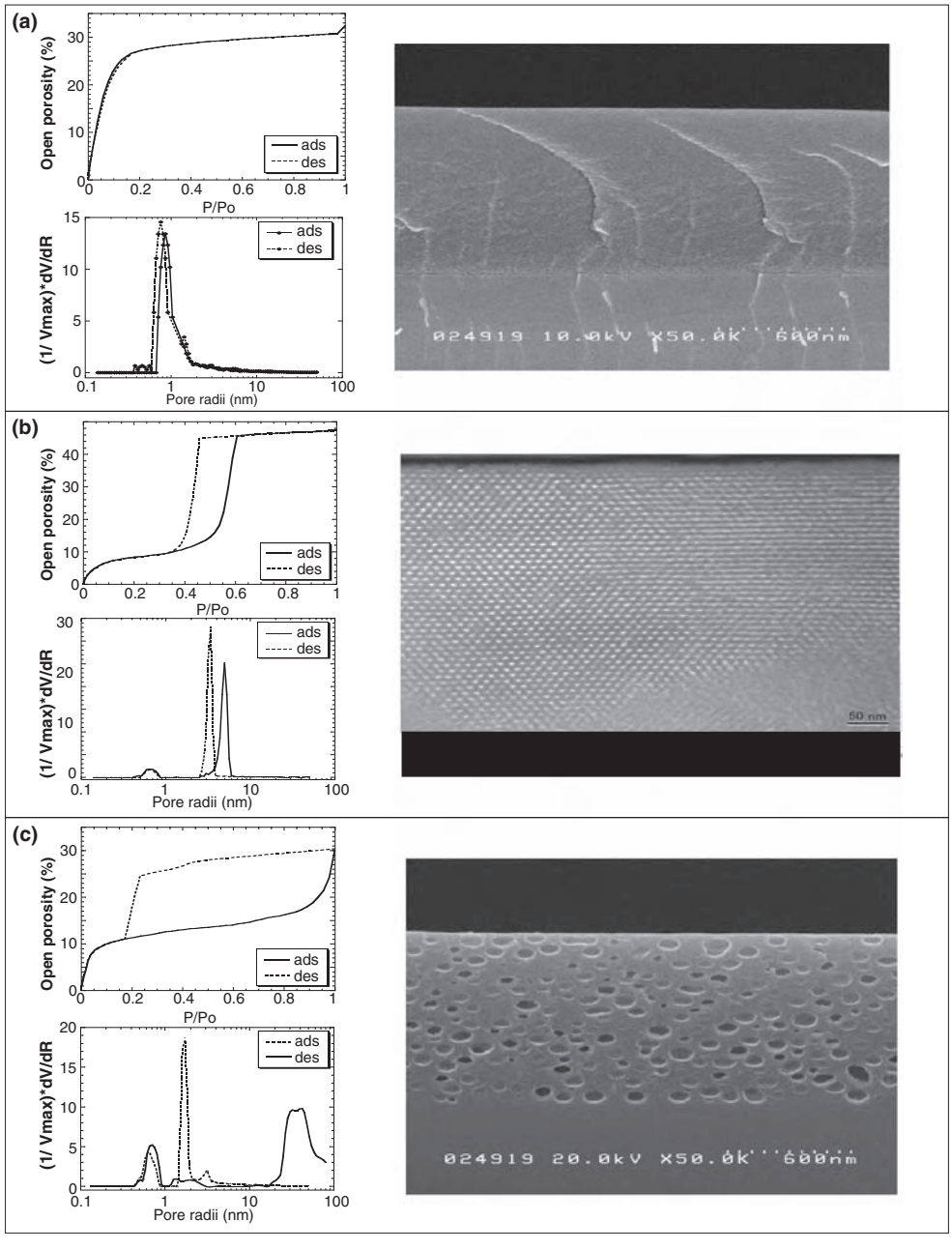

Figure 3.22 Adsorption/desorption isotherms, pore radius distribution and SEM pictures of three different types of low-*k* films: (a) CVD low-*k* film with open porosity equal to 30%; (b) porous SOG low-*k* films with ordered cylindrical pores and porosity 47%; (c) porous SOG low-*k* film with large quasi-closed cavities and porosity 30%. (Reproduced with permission from [4], Copyright (2004) American Institute of Physics)

is a characteristic feature of microporous films. CVD carbon-doped silica films (SiCOH) are typically microporous and the Dubinin–Radushkevitch method is used for the pore radius calculation. The micropores are not visible in SEM.

Figure 3.22(b) exhibits results obtained for porous films with ordered cylindrical pores. The pore geometry significantly affects thermodynamic properties of fluids, their adsorption, desorption and diffusion behavior. In the case of semi-infinite cylindrical pores, a cylindrical interface is formed between the adsorbed layer and vapor during the adsorption, while evaporation (desorption) is related to the formation of a hemispherical meniscus between the condensed fluid and vapor. Therefore, according to the Kelvin equation (6), in the case of infinite cylindrical pores the pore radius calculated from adsorption curve is twice the radius calculated from desorption curve and the width of hysteresis loop is defined by Equation (11)

$$(P_d/P_0) = (P_a/P_0)^2 \tag{11}$$

where P_d and P_a are critical pressures during the desorption and adsorption, respectively.

Figure 3.22(c) shows the results of evaluation of a porous film with large quasi-closed cavities [86]. This film contains small micropores (necks) interconnecting the cavities. The necks are not visible in the SEM picture. The pore radii calculated from adsorption and desorption curves differ by a factor more than two. A qualitative scheme of the processes occurring during the adsorption and desorption in such films is shown on Figure 3.23. First, all the pores and cavities are emptied in vacuum ($P = 0$). When the adsorptive vapour is introduced into the chamber, the necks are filled at $P = P_1$. However, the pressure is still not high enough for the condensation in the cavities and their filling starts at the critical pressure for spherical voids, $P = P_2$. When we drop below the same pressure $P = P_2$ during the pumping down, the cavities can't be emptied because they are blocked by the liquid plug in the necks that can be emptied only at $P = P_1$. Liquid in cavities is in a metastable stretched state. As soon as the necks are opened ($P < P_1$), the adsorbate immediately evaporates from the cavities. However, the desorption curves do not always reflect the neck size. If the neck size is smaller than a certain critical size, desorption from the cavities occurs via cavitation (spontaneous nucleation of a bubble). In this case, desorption occurs at a pressure P_{cav}, which is lower than the pressure of equilibrium evaporation from the pore neck (Figures 3.23b). The cavities are emptied by diffusion while the pore neck remains filled. In the case of cavitation, desorption pressure is not directly related to the neck size, but depends on the tensile stress limit of condensed liquid. Therefore, evaluation of the same material with different adsorptives might make it possible to separate the cavitation effect and equilibrium desorption.

Quantitative description of adsorption and desorption processes in spherical cavities connected through narrow cylindrical necks is given by the DBdB theory (Derjaguin [87], Broekhoff and de Boer [88]). The equilibrium thickness of the adsorbed layer h in a spherical pore of radius R_p is determined from the balance of capillary and disjoining pressures [89, 90]:

$$\Pi(h)V_L + \frac{2\gamma V_L}{R_p - h} = RT\ln(P_0/P) \tag{12}$$

where $\Pi(h)$ is the disjoining pressure of the adsorbed layer. According to this equation, the capillary condensation in a spherical cavity, which is connected with the neighboring cavi-

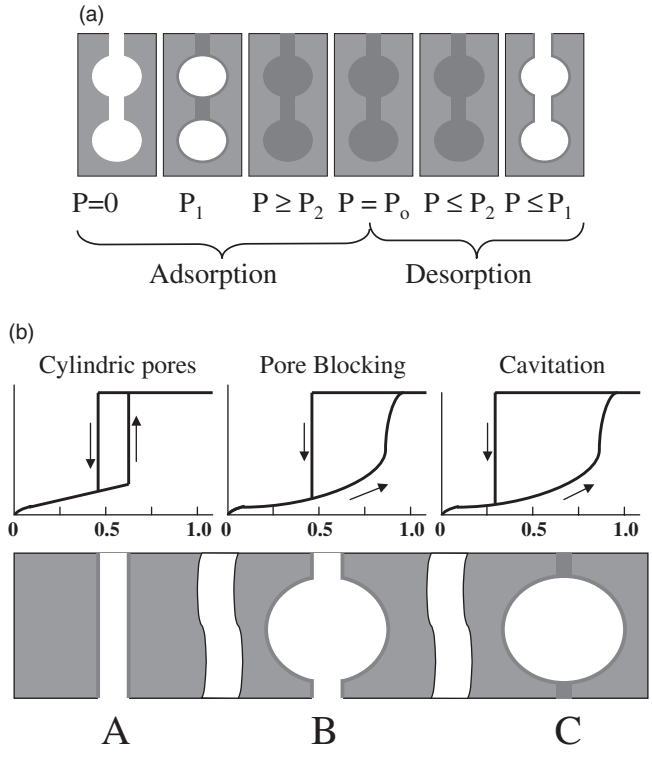

Figure 3.23 (a) Schematic illustration of adsorption and desorption in 'ink-bottle' pores; (b) equilbrium adsorption/desorption isotherm in cylindrical pores (A), pore blocking effect in ink-bottle pores (B) and effect of cavitation in 'ink-bottle' pores with ultra-narrow necks (C)

ties through narrow necks is always associated with a hysteresis larger than expected by Equations (6) and (11). During the adsorption, the isotherm traces a sequence of metastable states of the adsorption layer, and the capillary condensation occurs spontaneously when the layer thickness approaches the limit of stability. The critical thickness of metastable layers is determined from the condition

$$-\left(\frac{\mathrm{d}\Pi(h)}{\mathrm{d}h}\right)_{h=h_{\mathrm{cr}}} = \frac{2\gamma}{(R_{\mathrm{p}} - h_{\mathrm{cr}})^2} \tag{13}$$

Desorption from a cavity is delayed until the vapour pressure is reduced below the equilibrium desorption pressure from the neck, which leads to larger hysteresis effect in comparison with cylindrical pores. Thus, while the capillary condensation condition is determined by the size of cavity, the desorption condition is related to the neck size [91].

Mechanical properties

Ellipsometry allows separate determination of refractive index and thickness of the film. If the change of refractive index is related to the pore filling and allows calculation of

porosity, the change of thickness is related to the miniscule reversible film shrinkage during the capillary condensation of a liquid in the pores. The degree of shrinkage depends on capillary forces and the elastic modulus of the film. Therefore, EP can be used to extract the elastic modulus of porous materials from the same data that are used for the evaluation of the pore structure [92, 93]. By measuring the film thickness d as a function of the relative pressure (P/P_0) and fitting to

$$d = d_0 - k_{ep} \ln(P/P_0) \tag{14}$$

one can extract the constant k_{ep} from which the modulus E can be calculated using

$$E = \frac{d_0 RT}{k_{ep} V_L} \tag{15}$$

Here the molecular volume V_L of the adsorbate is the only molecular characteristic needed for determining the elastic modulus. The difference in the film thickness at $P/P_0 = 0$ and $P/P_0 = 1$ is related to the change of the film stress during the toluene adsorption.

Figure 3.24(a) shows a typical change of the film thickness during the toluene adsorption and desorption. The minimum thickness corresponds to the relative pressure when almost all pores are filled by toluene, but the menisci still exist (max capillary pressure). This P/P_0 value corresponds to the maximum in PRD curve. The final film thickness corresponds to the complete filling of all pores at $P/P_0 = 1$ when the liquid surface does not form a concave meniscus. Fitting the experimental curve by Equation (14) allows one to determine the coefficient k and to use it for calculation of Young's modulus. If the films are thick enough (>1 μm), The Young's modulus values measured by EP, surface acoustic wave spectroscopy, Brillouin light scattering and nanoidentation [92] are in good agreement. For thin films,

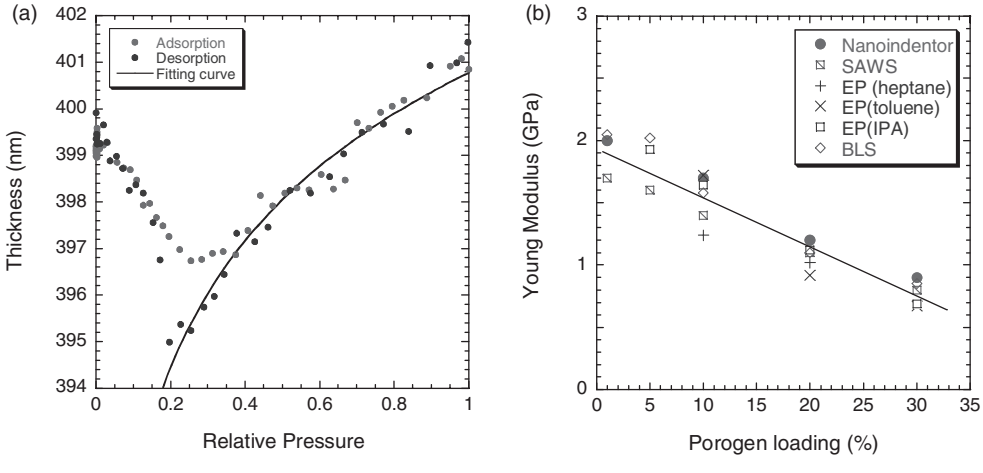

Figure 3.24 (a) Miniscule film shrinkage during capillary condensation of toluene in the pores; (b) comparison of EP Young's modulus with results obtained by nanoidentation, SAWS and BLS. (Reproduced with permission from [92] and [1], Copyright (2002) The Electrochemical Society (a) and (2003) American Institute of Physics (b))

the nanoidentation E values qualitatively follow the same trend with porosity, but the absolute values are 1.5–3 times greater. Nanoindeutation of soft films on stiff substrates is not well understood: current models are not applicable to this situation and the effect of substrate stiffening is not well corrected for. A possible error in Young modulus determination by EP is related to the surface roughness. In this case adsorptive condensation at $P/P_0 \leq 1$ gives an additional change of thickness and the E value can be underestimated.

Evaluation of diffusion barriers

EP is also used as a diffusion barrier integrity probe [94]. A continuous barrier deposited on top of a porous film prevents solvent vapor from penetrating into the porous film. As a result, no change of ellipsometric characteristics of a porous film is registered when the film is exposed to the vapor. On the other hand, a noncontinuous barrier allows vapor to penetrate into the film and change its ellipsometric characteristics. If the barrier is not continuous, change of ellipsometric characteristics allow calculation of the pore size in the bulk film under the barrier and also the size of voids in the barrier. An example of the ellipsometric response recorded during exposure of a 50% porous SSQ-based film with a PVD-deposited TaN barrier is shown in Figure 3.25. The noncontinuous barrier of 30 nm (Figure 3.25a) does not stop solvent from penetrating and experimental points follow the theoretical curve. When the thin film is continuous (Figure 3.25b) experimental points do not follow the theoretical curve, indicating there is no solvent adsorption inside the porous film. The small change in Ψ and Δ is attributed to solvent condensation on top of the TaN barrier. Similar results are obtained for barriers deposited on organic polymers [95].

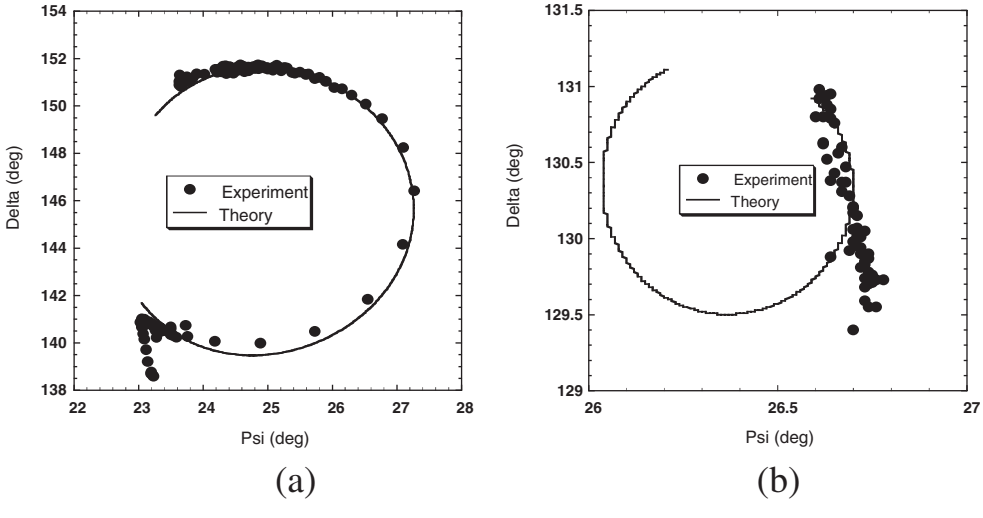

Figure 3.25 Ellipsometric angles Δ and Ψ recorded during exposure of a porous HSQ film with: (a) 30 nm TaN; (b) 60 nm TaN. Continuous curves represent calculated theoretical changes of Δ and Ψ supposing the barrier is porous. (Reproduced with permission from [94], Copyright (2003) American Institute of Physics)

The EP technique is also able to reveal low-density defects (killer voids). If the barrier has a limited number of large voids, solvent is trapped beneath such defects. If the distance between these voids is larger than the diffusion length of solvent inside the low-*k* film, the change of optical characteristics is local and these voids are quantified using an optical microscope and a special digital camera installed on top of the EP chamber. More detailed description of this methodology can be found elsewhere [82, 96].

Evaluation of hydrophilic properties

Hydrophobic properties of low-*k* materials are extremely important because even a small amount of adsorbed moisture drastically increases effective dielectric constant [1] and deteriorates their mechanical properties, important for integration [97–99]. Hydrophobicity of low-*k* materials is achieved by introduction of special hydrophobisation agents. These agents are normally hydrogen, methyl or other organic groups bonded to silicon atoms in a $SiO_{4/2}$ matrix [1]. Hydrophobization agents can be degraded during the technological processing, such as thermal annealing, plasma etch and cleaning, CMP and wet cleaning solutions, etc.

For instance, various plasmas are used in ULSI technology. The plasmas differ in reactants partial pressure, power and used for CVD deposition, pattern transfer into the films. The common plasma consequence is the carbon depletion of organosilicate or silsesquioxane films after etching and resist-ashing using O_2- and H_2-containing plasmas. Oxygen and hydrogen radicals react with the $Si–CH_3$ and the Si–H groups and form hydrophilic groups that induce the moisture uptake. The degree of damage increases with porosity, since the penetration of the radicals is deeper, as well as the absorption of water [100, 101]. The latter leads to dramatic degradation of dielectric and mechanical properties.

Different techniques are used for characterization of plasma damage. They are based on evaluation of change of chemical composition: Fourier transform infrared spectroscopy (FTIR), X-ray photoelectron spectroscopy (XPS), time-of-flight secondary ion mass spectroscopy (TOF-SIMS), energy filtered transmission electron microscopy (EFTEM) etc. and/or change of density X-ray reflectivity (XRR), surface acoustic wave spectroscopy (SAWS), spectroscopic ellipsometry (SE). It is assumed that the degree of carbon depletion directly correlates with the further change of hydrophilic properties. The density change also correlates with change of dielectric constant, but densification occurs simultaneously with the carbon depletion, making the situation even more complicated.

EP allows direct measurement of hydrophilic properties of low-*k* films using a standard EP system equipped with a special water source. The water pressure in the EP chamber is varied from zero to saturation values. The amount of adsorbed water is measured as a function of relative pressure (humidity). Comparative evaluation of pristine low-*k* materials shows that most of them are highly hydrophobic (Figure 3.26) and the amount of adsorbed water at room temperature does not exceed 1–3% at 100% humidity. Plasma damage drastically increases the amount of adsorbed water that correlates with the results obtained from TOF SIMS analysis [102] (Figure 3.27).

An important feature of the EP-based metrology is the possibility of quantification of hydrophilic properties. The pore radius in the Kelvin equation depends on the contact angle θ. Toluene was chosen because it has almost zero contact angle with silica-based low-*k* materials. When water is used as an adsorptive, the calculated radius is $R/\cos\theta$, where R

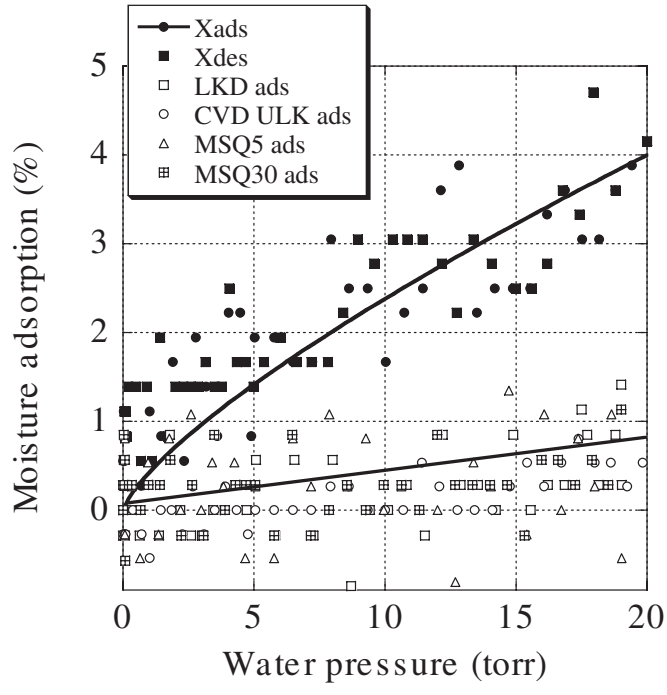

Figure 3.26 Adsorption/desorption isotherms in industrial low-*k* materials. Low-*k* film X that is more hydrophilic in comparison with others is a material with improved mechanical properties. (Reprinted with permission from *Microelectronic Engineering*, Vol. 83, M.R. Baklanov *et al.*, 2287–2291, Copyright (2006) Elsevier)

is radius calculated with a solvent having zero contact angle (toluene), the θ value reflects the effective contact angle of water for the internal surface of porous material (surface energy of damaged low-*k* material). Using the effective pore radii obtained by toluene and water adsorption, we calculate θ using equation

$$\theta = \arccos\left(\frac{R_{\text{toluene}}}{R_{\text{water}}}\right) \tag{16}$$

The calculated effective contact angle of internal surface is a unique characteristic reflecting internal surface energy of a damaged low-*k* material; to the best of our knowledge, no other technique as simple as EP allows one to measure it. Measurement of the contact angle on the external surface has a limited value because these characteristics can be significantly different.

It is also possible to estimate the depth of damage. In order to do it, we have to measure P_{w1} and P_{w2}, which are adsorbed water amount in pristine and damaged low-*k* materials, P_t (porosity measured by toluene) and the film thickness d_0. After that, the depth of damage (wetting) can be calculated using a simple formula

$$P_{w2}d_0 = P_t d + P_{w1}(d_0 - d) \tag{17}$$

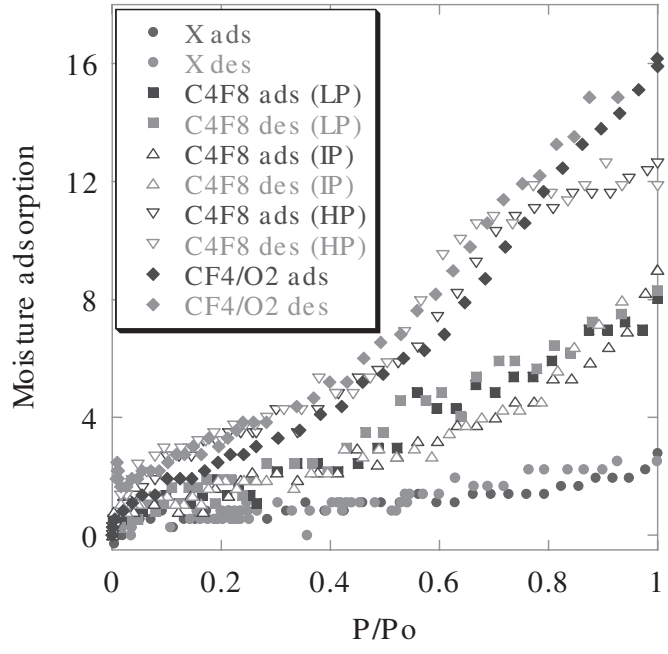

Figure 3.27 Adsorption/desorption isotherms of water vapor, demonstrating change of hydrophilicity after plasma etching. (Reprinted with permission from *Microelectronic Engineering*, Vol. 83, M.R. Baklanov *et al.*, 2287–2291, Copyright (2006) Elsevier)

Evaluation of plasma damage by ellipsometric porosimetry is very simple, fast and provides direct characterization of the hydrophilic properties of porous low-*k* dielectrics.

This method has also been applied for evaluation of moisture-induced degradation of low-*k* materials [103, 104], damaged by different technological processing.

3.4.4 Conclusions

EP is a new modification of adsorption porosimetry developed for evaluation of thin films. This method allows the measurement of pore size distribution at room temperature in thin films directly deposited on Si or any smooth solid substrate. Intermediate layers between the silicon substrate and the porous film do not create any problem for the measurements if their optical characteristics are known.

Experimental equipment and software for the PRD calculations from the ellipsometric measurements of the adsorption of the organic vapors in porous films have been developed. Round robin evaluations of various porous films and several different techniques such as EP, nitrogen porosimetry, PALS, SANS and SAXS have shown good agreement between the results of the analysis [11–13]. Industrial EP systems for nonstandard and 300 mm silicon wafers with a possibility of wafer mapping are in production by SOPRA (www.sopra-sa.com).

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4 Mechanical and Transport Properties of Low-*k* Dielectrics

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4.1 INTRODUCTION

4.1.1 Classification of low-*k* dielectrics

While Cu has proved to be the only viable solution as the new device generation's metal [1], the search is still on to find the viable solution for the new interlayer dielectric (ILD) material [2, 3]. A good summary of a leading candidate low-*k* ILDs is given in Table 4.1 and good reviews are available [4–6]. The candidate materials can be broadly classified into three areas on the basis of their backbone chemistry: polymeric or organic, hybrid organic/inorganic, or inorganic coatings. In each category, the materials can be split into

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Table 4.1 Leading ILD candidates (modified from rs [5, 6])

k	Organic polymers	Hybrids	Inorganics
4–4.2			SiO_2
3.0–4.0		HSQ/FOX™	Fluorinated silica (SiO_xF_y)
2.4–3.0	FLARE™	MSQ/HOSP™	
	PAE	Aurora™	
	Polyimide	Coral™	
	BCB	Z3MS™	
	SiLK™	Black Diamond™	
		Polyset™	
		Dendriglass™	
		Orion™	
2.0–2.4	Porous SiLK™	NCS™	Nanoglass™
	Parylene	LKD™	
		XLK™	
		Zirkon™	
$k < 2.0$	PTFE	. . .	Xerogel
			Aerogel

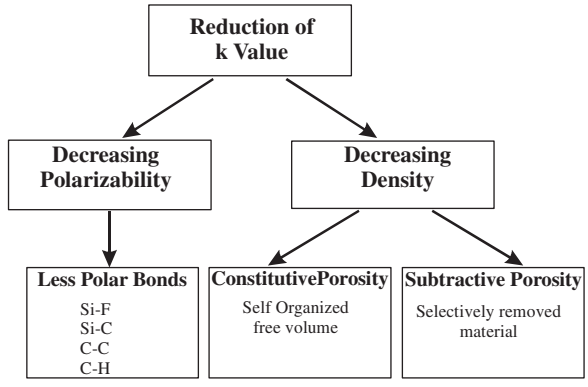


Figure 4.1 Methods to achieve lower dielectric constant value [7] (Reprinted from Materials Today, Vol. 7, Issue 1, Shamiryan D., Abell T., Iacopi F. and Maex K., Low-*k* Dielectric Materials, 34–39, Copyright (2004), with permission from Elsevier)

two additional types, porous and nonporous. Introducing porosity in these materials is the most popular approach to achieve dielectric constants below 2.0 (except for Teflon). Consequently, porous materials have started to arouse considerable interest among researchers in this field.

Another way to separate low-*k* dielectrics would be to classify the materials based on the methodology used to achieve a low dielectric constant (Figure 4.1). Generally, the *k* value can be lowered by introducing low polarizability bonds or by making the material porous. A material can be made porous by either constitutive porosity or subtractive porosity

[7]. Constitutive porosity refers to porosity introduced by the self-organization of a material. After manufacturing, such a material is porous without any additional treatment. Constitutive porosity is relatively low (usually less than 15%) and the pore sizes are small, ~1 nm in diameter. Subtractive porosity involves selective removal of part of the material or incorporation of a sacrificial material. The material is removed via thermal annealing, supercritical extraction, or by selective etching. Subtractive porosity can be as high as 90% and pore sizes may vary from 2 nm to tens of nanometers. In general, the porosity in porous materials can be either open-pore or closed-pore in structure. Closed pores are isolated from one another whereas open pores have a large degree of interconnectedness. Most subtractive porosity materials have an open-pore structure.

Organic polymers

Organic polymers represent the largest class of potential low-*k* materials and Maeir [8] presents a review of many of them. A brief description of some of the more well-known are given below.

Poly(aryleneethers) (PAE) and fluorinated poly(aryleneethers) [9–12]. Several polymers from this class have been studied extensively [9]. Allied Signal's FLARE™ is an example. The first generation of this polymer is shown Figure 4.2. Typically dielectric constants of 2.8 are achieved. Recently porous PAE films have been prepared where abietic acid is used as sacrificial solvent [10, 11] to make them porous.

Parylene N and Parylene F. Parylene N ($k \sim 2.7$) is a poly(1,4-xylylene) while Parylene F ($k \sim 2.4$) is a perfluorinated version where all the methylene units are replaced with difluoromethylene units. The parylene family of materials were developed in the 1950s and used for coatings and electrical insulation in 'hostile environments'. Parylene has excellent gap-filling capability and also gives conformal, pinhole-free films with excellent moisture and vapor barrier properties. The structure of Parylene F is shown in Figure 4.3.

Polyimides and fluorinated polyimides [9]. These polymers have been used for a long time as an interlayer dielectric, but generally in larger structures where the dielectric constant was not an issue. They have been revisited more recently as candidate low-*k* materials.

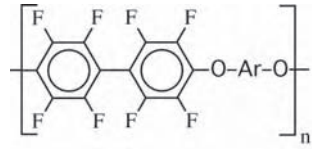


Figure 4.2 Presumed structure of first-generation FLARE™

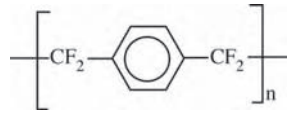


Figure 4.3 Structure of Parylene F

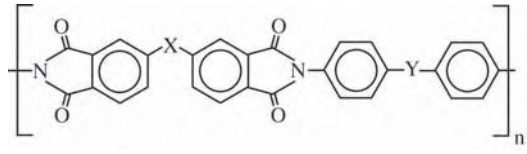


Figure 4.4 Structure of a polyimide

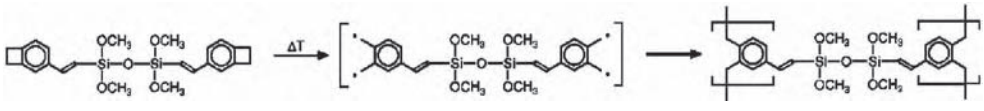


Figure 4.5 Structure of BCB

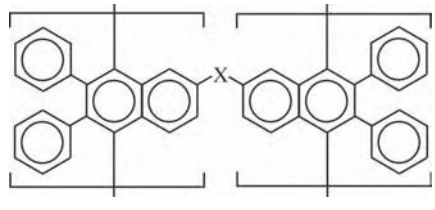


Figure 4.6 Structure of one member of the SiLK™ family

They exhibit a low-k (2.6–2.8), a relatively high glass transition temperature (≥350°C), minimal moisture absorption, and high thermal stability. Their main problem is that they are inherently anisotropic and the in-plane and out-of-plane dielectric constants, mechanical, and thermal properties can be very different [9]. Dupont's Kapton™ was the first material of this class commercialized and is shown in Figure 4.4.

Bisbenzocyclobutene (BCB) [13, 14]. These polymers were developed by Dow Chemical in the 1980s and offered under the commercial name, Cyclotene™ (Figure 4.5). They have been studied quite extensively and their dielectric constants are in the 2.65 range. Nierynck *et al.* [13] have demonstrated integration capability of BCB with copper. However, the thermal stability of BCB is not sufficiently high to withstand the high-temperature process steps encountered in actual chip fabrication. BCB is successfully used in processes with less stringent thermal stability requirements, such as in packaging, and in GaAs integrated circuit interconnects [14].

SiLK™. SiLK™ [14, 15] (short for silicon application low-k material) is a spin-on, cross-linkable, aromatic polymer from Dow Chemical with good thermal stability (up to 475°C), a wide process window, a high glass transition temperature (490°C), and a low dielectric constant ($k \sim 2.65$). The material has been made porous using a sacrificial dopant technique, and has been integrated with Cu in a single damascene structure [16]. However, the dense material has a rather low thermal conductivity [17] and low elastic modulus [18]. The structure of one member of the SiLK™ family is shown in Figure 4.6.

Amorphous fluorocarbons [19, 20]. These are Teflon-like materials deposited by chemical vapor deposition processes using fluromethanes as precursors [19]. Porosity has been

introduced using a sacrificial dopant technique to produce films with a very low dielectric constant [20]. The concerns regarding the fluorine substituents are basically the same as those attributed to fluorinated oxides.

Teflon AF [21, 22]: Teflon™ films can be deposited either by spin-coating [21] or chemical vapor deposition [22]. The spin-coated films are deposited from an emulsion containing sub-20 nm polytetrafluoroethylene (PTFE) particles and a suitable surfactant. Regardless of the deposition mechanism, the dielectric constant is around 1.9; the lowest available for a dense, organic material. The drawbacks of Teflon™ are its advantages in other uses, including poor adhesion to virtually any other material, and low glass transition temperature, which causes material to slowly creep over time, even at room temperature.

Inorganic materials

Fluorinated oxides (SiOF) [23–25]. Fluorinated oxides are essentially silicon dioxide films deposited by chemical vapor deposition using fluorine-containing precursors. The result is a glass that contains from 2–10 at.% fluorine. The strong electron withdrawing ability of F lowers the dielectric constant to 3.7–3.0. Since the material is amorphous, special care must be taken during processing to insure that the fluorine is sequestered and will not react with or diffuse into adjacent layers. Diffusion and reaction issues have been addressed adequately in recent years, and fluorinated oxides are now used routinely as an interlayer dielectric.

Porous silica Materials [26–37]. Porous silica materials are variants of dense silicon dioxide (silica) that have been made porous by one of a variety of methods. The porosity can range anywhere from less than 10% for Vycor-type glasses to as high as 99% or more in silica aerogel materials. Since the dielectric constant of silica is around 4, introducing porosity is the only viable way to achieve dielectric constants much below 2.0.

Porous materials are divided into two main types, depending on whether their porosity can be considered as an open- or closed-pore. Open-pore materials exhibit an interconnected pore structure and examples include silica xerogels (also called Nanoporous Silica™ [26] or mesoporous silica films [27–31]). These materials are formed from alkoxysilane monomers by sol–gel processing followed by removal of the solvent or solvents used along with any other additives introduced. The internal surface of these porous silicates contains a great number of OH groups left over from the sol–gel reactions and so the material must be chemically modified to be hydrophobic. The surface modifier introduces some organic character to the material, and for this reason, porous silica is technically a hybrid, inorganic/organic material.

Porosity can be introduced by a variety of templating procedures. The most common approach uses a low-volatility solvent as the templating agent [26, 32, 33], but templated approaches can use surfactants, polymers, or nanoparticles [27–31], as the templating agent to produce a more ordered array of pores. Using nonvolatile templating agents require dissolution or calcination techniques to remove the template. Following calcination in particular, a surface modification step is required to restore the material's hydrophobicity. Most templating approaches yield open-pore materials. Closed-pore films are synthesized by burning or dissolving an organic component from the silicate matrix [31], but there is a limit (percolation threshold) to the porosity (~20–25%) above which the structure becomes open-pore. There is still some debate on whether closed-pore films can ever be produced using a sacrificial templating technique.

Mesoporous silica films are prepared from microemulsions by the condensation of a silicate network around surfactant micelles. The pores are introduced when the surfactant micelle is burnt out. Bruinsma *et al.* [27], Fan *et al.* [29], Zhao *et al.* [34] and many others have used this technique to produce not only low-k materials, but porous materials for catalysis as well [35]. In general, these techniques are relatively costly since the starting materials are costly. Birdsell *et al.* [36] reported on the fabrication of porous silica films prepared from commercially available colloidal silica and potassium silicate. In their work, as prepared films can have porosity in excess of 85% and a dielectric constant $k < 2.0$. this technique uses relatively inexpensive ingredients, but using potassium silicate as a precursor requires leaching the films prior to electrical testing to eliminate alkali ion impurities. Porous silica zeolite low-k films have also been prepared [37]. Zeolites are highly ordered, crystalline systems with precisely defined pore structures. The zeolite films are reported to have ordered structures and very high modulus and hardness, though they take much longer than standard porous silica films to fabricate.

Hybrid materials

The physical property constraints for an interlayer dielectric are stringent and it is likely that neither a purely organic nor a purely inorganic material will exhibit the optimal combination of properties required. Thus, attention has focused on hybrid (organic–inorganic) materials that offer a compromise in properties between those of organic and inorganic materials. If the organic component is grafted onto an inorganic network, the mechanical properties of the inorganic matrix and the chemical properties of the organic modifier are achieved. This type of material is quite versatile and can be made highly hydrophobic. Alternatively, specific chemical functionality or reactivity can be added, without changing the matrix or other essential material properties. By incorporating organic material into the inorganic, usually silica-based matrix, the overall material properties can be tailored between those of pure glasses or ceramics and those of silicones [38]. Some synonyms used for these hybrid matrix materials are ormosils (organically modified silicates), nanocomposites, and ceramers (ceramic polymers). There are some advantages to introducing the organic as part of the network rather than as a stand-alone pendant group. Organic components reduce the overall dielectric constant, hence they can achieve comparable dielectric constants to porous inorganic materials, but at reduced levels of porosity. Since many physical properties scale with porosity in the form of a power law, reducing the porosity is often beneficial to the performance of the material. Adding organic content also tends to make the material more abrasion and chemically resistant and so less apt to degrade during chemical–mechanical polishing.

Organosilicate glasses (OSG) [39, 40, 42, 43]. These are the hybrid materials discussed above. They can be made by spin-on (liquid-phase) or gas-phase processes. Vapor-deposited systems are generally nonporous, carbon- or methylene-doped SiO_x films (SiOC), such as Applied Material's Black Diamond™ or Novellus's Coral™ dielectric. Both materials achieve dielectic constants in the 2.7 range and are deposited by chemical vapor deposition using tetramethylsilane or trimethylsilane precursors. These films are inherently hydrophobic, and due to their hybrid nature, etching, stripping and cleaning processes must be precisely tuned to keep the material hydrophobic [39] and to etch the material uniformly. OSG films can also be made porous if two chemical constituents are vapor deposited

simultaneously and one of them is later burnt or leached out to leave behind porosity in the film [40].

Most hybrid materials, that are designed to be porous are deposited by wet, sol–gel type processing. Sol–gel–deposited materials are inherently porous due to the use of a solvent, though the materials can be densified by sintering at high temperature. The internal surface of porous, sol–gel–based materials can be chemically modified easily using silane coupling agents. Several types of these materials will be discussed in more detail below.

Researchers at IBM Almaden Research Center [31, 41, 42] developed Dendriglass™, a nanophase-separated, closed-pore, inorganic–organic family of hybrid polymers with k below 3.0 for use as ILD materials. These materials were prepared from reactively functionalized poly(amic ester) derivatives and substituted oligomeric silsesquioxanes. They are thermally stable to at least 400°C and comparatively tougher than organically modified spin-on glasses without significantly affecting other important polymer properties of the silicates. To prevent phase separation on a macroscopic scale, the thermoplastic polymer (a three-dimensional dendritic molecule) was chemically incorporated into a growing silicate, during condensation. This approach toughens the silicate network and prevents shrinkage and cracking during drying [43]. After burning out the dendritic polymer, it is claimed that small (<5 nm) closed pores (till about 20–25% porosity) are generated (Figure 4.7). Yang *et al.* [44] have formed porous silsesquioxanes with ultralow dielectric constants ($\simeq$1.5) by using triblock copolymers as templates and tailoring their microphase separation.

Silsesquioxanes (T-resins) [45–47]. these materials are similar in some ways to Dendriglass™. The synthesis route starts with sol–gel materials having a stoichiometry $(RSiO_{1.5})_n$. The silsesquioxanes are obtained by hydrolytic condensation of trifunctional silanes, such as $RSiCl_3$, or $RSi(OMe)_3$ which can then be futher condensed to form a three-dimensional network. There are basically two types of silsesquioxane materials that have been extensively used and tested. The first are hydrogen silsesquioxanes (HSQ) shown in Figure 4.8(a). These materials contain little or no carbon, exhibit dielectric constants $k \approx 3$, and have high glass transition temperatures, much like pure nanoporous silica. One commercial example is the FOX™ dielectric by Dow Chemical. The other major family of silsesquioxanes are methyl silsesquioxanes (MSQ, spin-on glass) shown in Figure 4.8(b). Here, the hydrogen is replaced by a methyl group and MSQ-based materials have a methyl group covalently bonded to each silicon atom. These materials have a ladder-type structure, dielectric constants, $k < 2.7$, exhibit good gap-fill properties, high thermal stability and good

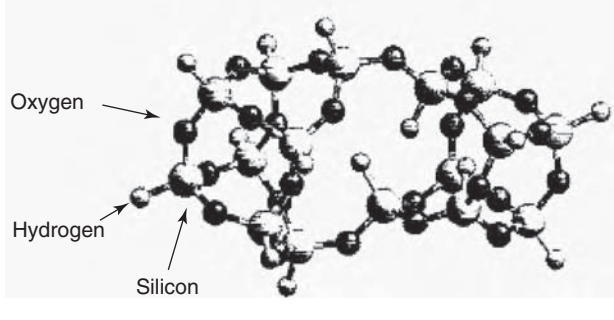


Figure 4.7 Proposed structure of porous MSQ, DendriGlass™

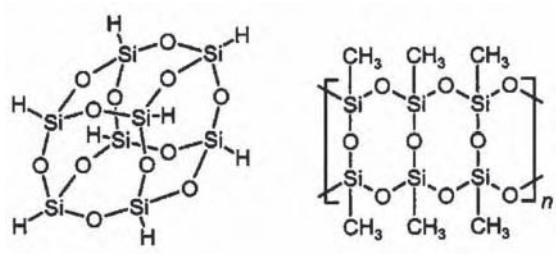


Figure 4.8 (a) Hydrogen silsesquioxane; (b) methyl-silsesquioxane

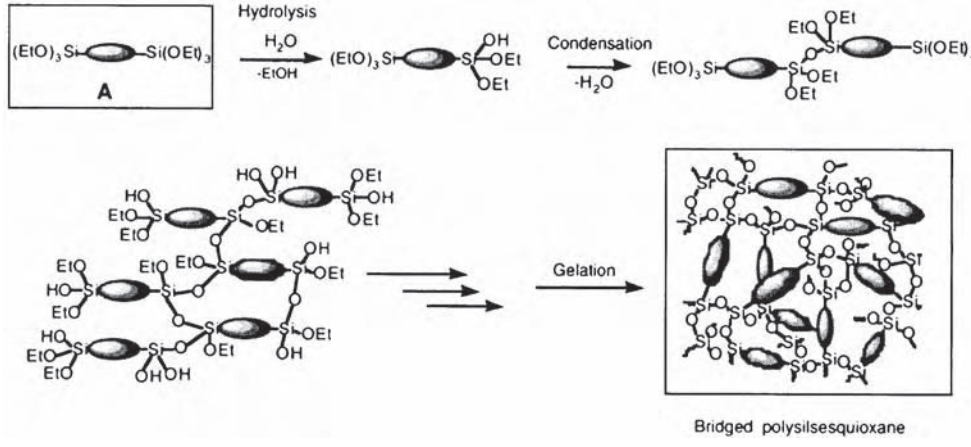


Figure 4.9 Formation of bridged polysilsesquioxanes (Reproduced with permission from the *Materials Research Society Bulletin*) [48]

resistance to the type of harsh chemical environments encountered in post-etch cleaning and CMP [46]. A commercial example of this material is Honeywell's HOSP™ with $k = 2.6$.

To achieve lower dielectric constants, porous versions of silsesquioxanes are now available. JSR LKD™ is an example of a porous HSQ with $k \sim 2.2$. Variants of MSQ-based materials from Dow Chemical and Shipley are XLK™ and Zirko™ repsectively. Aoi [47] reports on the synthesis of porous films by addition of a triphenylsilanol (TPS) moiety to a commercially available spin-on glass. Pore formation occurs due to the steric hindrance of the TPS moieties. The TPS moieties are burnt out to leave pores about 8 nm diameter and $k \sim 2.3$.

Bridged polysilsesquioxanes [48]. These materials can be made porous or nonporous and have more organic content and hence slightly lower intrinsic dielectric constant than MSQ. They each contain an organic group that bridges two trialkoxy groups in each monomer unit [48]. The materials are hexafunctional and so gel faster than MSQ_n- or HSQ-based materials and there is better control of organic incorporation (in the monomer). Bridged silsesquioxanes containing organic dyes have been prepared for waveguide, nonlinear optics, laser applications, and optical storage (photochromism) [38, 48]. An example is shown in Figure 4.9.

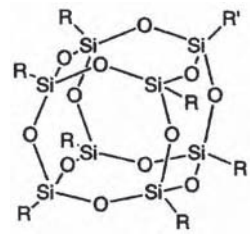


Figure 4.10 An example of POSS monomer

Polyhedral oligomeric silsesquioxanes (POSS) [49]. these are a new class of materials with rigid, cage-like cyclic siloxane monomer units. They offer more spatial control of the monomer structure than MSQ for example. Monomers with various functional groups are now commercially available for testing [49]. One use for these materials is as pendant units to organic polymer chains. This would reinforce the polymer to improve overall processing of the material and to improve the mechanical properties of the purely organic polymer matrix.

The problems associated in the integration of low-*k* ILD materials with copper are being addressed with great effort. The chief concerns with regards to the integration of these materials as ILDs include chemical stability (moisture absorption, etch selectivity, etc.) mechanical properties (adhesion, elasticity, hardness, etc.), thermal stability (high thermal conductivity, low thermal coefficient of expansion, etc.) and electrical stability (prevent interdiffusion of metal as well as barrier layers) [50–52]. Previous works have evaluated the issues of moisture adsorption, mechanical strength, thermal and electrical stability of a particular class of low-*k* materials, viz. porous materials [53–55]. This review concentrates on the compatibility issues of porous dielectric materials with contiguous metal and barrier layer materials. The integrity of the different contiguous layers depends strongly on the underlying substrate in addition to the layer's own properties. The disparity in material properties between the metal-barrier-dielectric give rise to driving forces that attempt to change the configuration of the thin-film stack.

4.2 MECHANICAL PROPERTIES

4.2.1 Introduction

The mechanical properties of low-*k* materials depend upon the material's composition, its microstructure and its processing history. At the present time, the failure of these materials to achieve mechanical properties sufficient for their use in dual damascene fabrication schemes represents the major obstacle to their incorporation in integrated circuits. This is especially true for nanoporous materials.

An excellent introduction to the mechanical properties of low-*k* materials, especially nanoporous, low-*k* dielectrics, is given in the text *Interlayer Dielectrics for Semiconductor Technologies* [5]. This section basically serves as an update to that earlier work.

4.2.2 Modulus

The elastic modulus is the basic property used to assess the mechanical strength and process compatibility of interlayer dielectrics. While other properties such as fracture strength, flexural strength, and fracture toughness are important, if the elastic modulus cannot meet a minimum standard, the material cannot be used in dual damascene processing. This brief section will be divided into two parts, a discussion of models used to predict and correlate mechanical strength, especially of porous materials and a discussion of recent experimental data for low-*k* materials.

Models for generic porous materials

First principles models predicting the elastic modulus of pure materials are not well developed. While molecular simulations can be used to predict the mechanical properties of materials, these are still too complicated to be used as assessment tools in the semiconductor industry. Thus for dense solids, rules of thumb such as crystalline materials having higher moduli than glassy materials and for polymers, the elastic modulus increasing with increasing levels of crosslinking are more useful.

For porous materials, there is more predictive capability available from the continuum modeling perspective. Several classes of models have been introduced, some of them simple enough to be used for screening and rough predictions. These will be discussed briefly below.

(a) Exact/fundamental models. The micromechanics [56] method has been used to predict what happens when a single inclusion or low volume of inclusions is incorporated into a matrix. Work has been done to extrapolate from these results and extend the results to higher volume fractions of spherical or ellipsoidal pores [57]. Since these are generic methods, the exact microstructure of the solid corresponding to a particular formula for the elastic modulus is not precisely known. Thus for any given porous solid, multiple formulae may actually fit the experimental data. The models also consider only a continuous matrix that can be viewed as a homogeneous material and so no predictions can be made when the microstructure of the matrix is comprised of incompletely sintered grains, which is a common morphology in porous ceramics. Theoretical bounds [58] exist to predict the elastic properties of composites, but since porous materials have no lower bound to their elastic properties, these lose their predictive power when the upper bound does not provide a good estimate.

(b) Cellular models. Cellular models view the composite system to be of high porosity and having a microstructure similar to a soap bubble foam. The porous material is built up of thin walls framing the surfaces of a hollow cell. Figure 4.11 shows a typical unit cell for an open-cell foam. The corners of one cell rest upon the midpoint of adjacent cells. While this structure is not the best physical representation of a foam, it does capture many of the important characteristics is a useful correlative tool for predicting how a material should behave is porosity is introduced [59]. The relative density of a foam is defined as:

$$\frac{\rho}{\rho_{\text{dense}}} \propto \frac{V_{\text{material}}}{V_{\text{cell}}} \propto \left(\frac{t}{l}\right)^2 \tag{2.1}$$

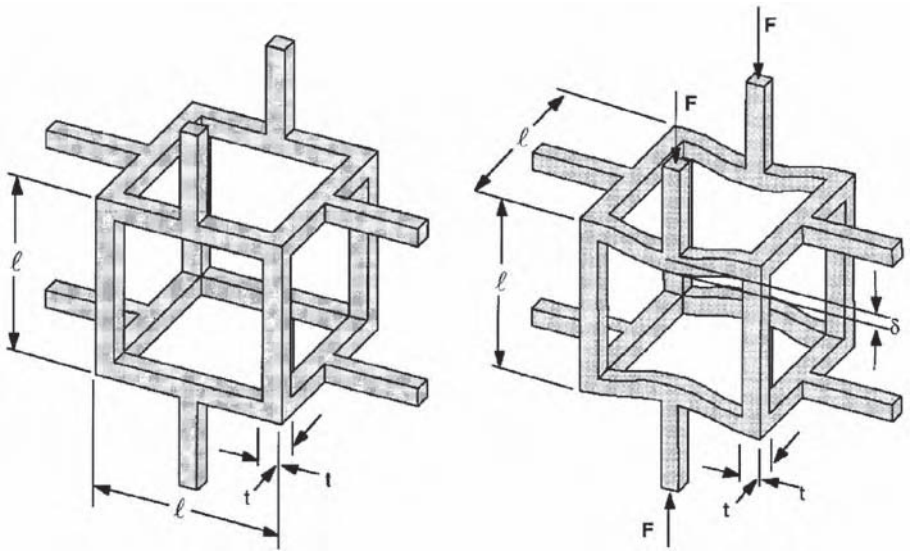


Figure 4.11 Unit cell for an open-cell foam showing what happens during loading (Reproduced with permission from the Cambridge University Press) [59]

To connect the structure of the foam to its elastic modulus, a uniaxial stress is applied to the foam so that each cell edge transmits a force F. Since the whole solid behaves in a linearly elastic way, the deflection of the structure as a whole is proportional to F and the Young's modulus for the foam can be related directly to the relative density.

$$\frac{E}{E_{\text{dense}}} = C\left(\frac{\rho}{\rho_{\text{dense}}}\right)^2 \tag{2.2}$$

where C is constant. Since a foam is not composed of a completely uniform cell geometry and size, it is more appropriate to determine the value of C by fitting it to data, instead of solving it analytically. Gibson and Ashby [59] fit equation (2.2) to the modulus measurements of a variety of materials and found $C \approx 1$.

(c) Minimum solid area (MSA) models [60–62]. This approach uses purely geometrical reasoning to predict the elastic modulus based on the weakest points within the structure. The minimum solid area is defined as that fraction of two-dimensional space occupied by solid in a packed particle or packed pore array. This model assumes that all solid properties have the same dependence on porosity and ties the evolution of the MSA and the considered property to the porosity. For the porosity range 0 to 1/3–1/2 P_c, the variation of the MSA (or property) with porosity can be described by:

$$\frac{S}{S_{\text{dense}}} = \exp(-bP) \qquad \text{for} \quad 0 \le P \le 1/3 \text{ to } 1/2P_c \tag{2.3}$$

where S (e.g., modulus, toughness or thermal conductivity) is the property of the porous material, S_{dense} is the corresponding property for the dense material, b is a characteristic

parameter of the pore stacking, and P_c, corresponds to the percolation limit of the solid phase and is characteristic of the porous structure. It is defined as the volume fraction at which the solid phase is no longer connected.

MSA models are empirical fits. These models cannot represent the entire porosity range with a single type of stacking geometry and so multiple packings are required for any given material. The transition from one kind of packing to other is not well defined and so the phase inversion cannot be accounted for directly. Axial extension is the only form of deformation mechanism, which is not justified for most materials. Wang [63] has shown that bending and shear effects are also important and tend to reduce the modulus. While useful over a rather limited range, MSA models are too empirical to be used as a predictive tool.

(d) Computational models. These are basically finite element simulations of deformation assuming the solid matrix material is well known. Roberts and Garboczi [64] employed three different microstructural models that broadly covered the types of morphology observed in porous materials. The models were based on randomly placed spherical pores, solid spheres, and ellipsoidal pores. The results of the simulations, which were expressed by two- (or sometimes three-) parameter relations, correspond to a particular microstructure and explicitly show how the properties depend on the nature of the porosity [65, 66]. One drawback was that these simulations were only valid for low porosities. The cost of the calculation increased significantly as porosity was increased so beyond a porosity of 50%, the simulations were not cost effective to run.

(e) Percolation theory. Percolation theory can be used to define an analogy between a gel and a percolation cluster [67]. Such an analogy leads to a power-law dependence of elastic modulus or other properties as a function of reduced density, or probablility that a site is occupied by solid. This theory produces an equation similar to that for the cellular solids.

$$E \propto (P - P_c)^{\tau} \tag{2.4}$$

Here P is the probability for a site to be occupied (or a bond to be created), P_c is the percolation threshold (defined as the magnitude of P above which an infinite cluster exists) and τ is a critical exponent that is characteristic of the physical property (e.g., elastic modulus). The choice of a physical variable that can replace the unknown mathematical variable P_c is difficult. In the straightforward gelation/percolation analogy, the gel fraction (and thus the density) is associated with the percolation probability, (the probability for a site to belong to the infinite cluster) and scales with an exponent, β. Therefore $E \propto \rho^{\tau/\beta}$ or $E \propto \rho^{m}$. The exponent m has been found from literature and computer simulation to be ~9 and is about a factor of two too high.

Modulus measurements

The modulus of a thin film is most often measured by nanoindentation [68, 69], but other measurement techniques exist, including beam bending, surface acoustic wave, and Brillouin scattering. Discrepancies between the techniques are common [70] and published data over a full range of porosity is rare. However, each technique is useful to compare one material against another.

A number of investigators have reported on the measurement of E for several silica-based, hybrid and polymeric materials, which are in contention as low-k materials. Figure 4.12 shows the reported E values for a variety of these low-k materials compared with data for xerogel films processed using ethanol or ethylene glycol as a solvent and for xerogel films that had been sintered following fabrication. The modulus of porous silicates is the highest in the group and the modulus of sintered xerogel extrapolated to $\Pi = 0$ approaches that of dense oxides (CVD or thermal). The modulus of sintered xerogels, templated silica ($k = 2.4$, $\Pi = 55\%$) [71], Vycor glass [72], and the dense oxides [73–75] obey the same power law relationship. This supports the hypothesis that all these materials have continuous solid matrices made up of nearly pure SiO_2. E values for xerogel films made with ethylene glycol are comparable to the elastic modulus of methylsilsesquioxane (MSQ) [76–78] and bridged hybrid silsesquioxane materials [79]. The modulus of xerogel films made with ethanol is similar to that of hydrogen silsesquioxane (HSQ) [73]. HSQ also has a random structure made of cages and ladders. The moduli of dense polymeric low-k materials [80] such as benzocyclobutene (BCB) [81, 82], SiLK™ [83], polyarylene ether (PAE) [80, 84], polynorbornene [85], polyimide [86, 87], and Teflon [88] are scattered and depend on the cross-link density, the free volume of the polymer, and any density differences that can cause effects similar to the introduction of porosity. Thus Figure 4.12 shows clearly that families of porous materials can be identified, all based on the composition and defect structure of the matrix materials. The moduli of amorphous porous dielectric materials depend on the process history and the properties of the solid phase.

Sintering was shown to affect the properties of nanoporous silica, healing defects in the silica matrix and increasing the elastic modulus. Curing of materials using ultraviolet (UV) radiation has been proposed to accomplish similar strengthening [90–92]. By and large the curing process is used to help cross-link polymeric materials, thereby enhancing their mechanical properties, but if the materials or the underlying substrate absorbs significantly in the UV region of the spectrum, absorptive heating can anneal a sample similar to thermal

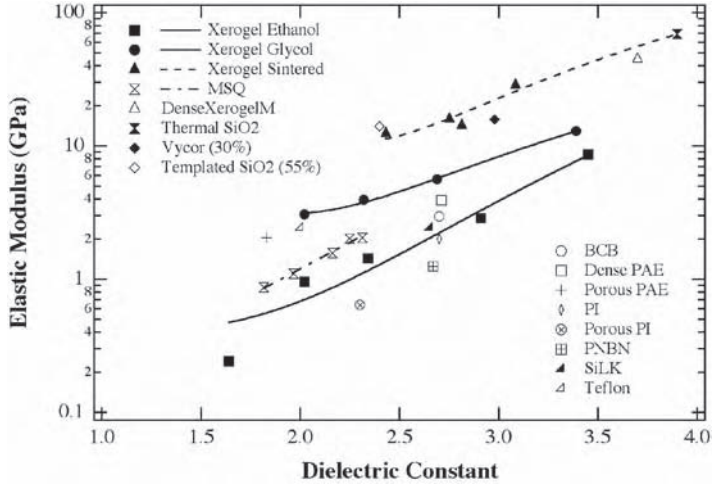


Figure 4.12 Elastic modulus for a number of popular low-k materials. Solid lines are power-law fits for xerogel films made using different processing techniques (expanded and updated from Jain *et al.*) [89]

processing. The UV process has some advantages in that the overall system is exposed to low temperatures, specific regions of the sample can be cured independently of one another, and depending on the absorptivity of the material, only the surface need be affected. UV curing is a promising technology, but much more work is needed to assess its effectiveness and usefulness in a production setting.

4.2.3 Interfacial properties

To insure device operation and reliability, thin-film configurations must resist changes in shape, i.e., be morphological stable over the device lifetime. Shape changes may occur in response to physical interactions such as gravity, van der Waals forces, electrostatics, capillarity (surface tension), and applied or intrinsic stresses, etc. [93]. The earliest study describing these changes was by Lord Rayleigh who considered capillary driven instabilities [94]. Since that time, the field has grown tremendously.

At thermal equilibrium, neither the surfaces of solids nor the interfaces between phases are perfectly flat. Thermal fluctuations roughen the regions between two materials. The driving force for shape change is a reduction in the overall free energy ΔG of the system. The microscopic origin of this excess free energy may be attributed to; the atoms at a free surface having 'missing bonds'; a metallic grain boundary containing 'free space' and hence not having the optimal electronic density; an incoherent interface containing dislocations that cost strain energy; and the ordering of a liquid near a solid–liquid interface, causing a lowering of the entropy and hence an increase in the free energy [95] (Figure 4.13). The final thermodynamically stable film–substrate configuration has the minimum free energy. However, this may or may not exist, depending upon the feasibility of kinetic pathways that lead from the initial state to the final state [96]. One needs to evaluate the contributions of each of the component free energies for a particular film–substrate combination.

Measurement techniques

Measurements are undertaken to determine the temperature and time associated with the onset of the instability (temperature and time) and the nature of the instability, whether it is an agglomeration-type failure leading to islanding, or whether it is a buckling-type failure leading to a loss of adhesion. The key quantitative parameters of interest are the activation

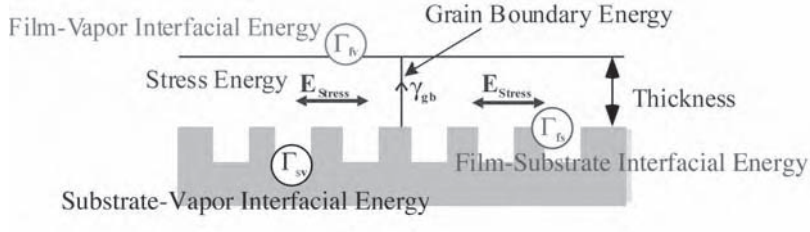


Figure 4.13 Final energy description of the metal film–porous substrate combination

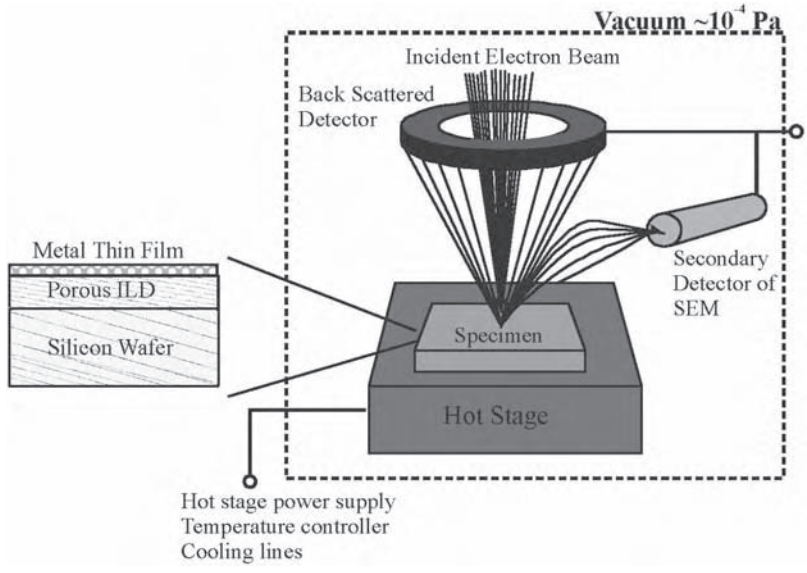


Figure 4.14 A schematic of hot-stage set-up for *in situ* SEM observations

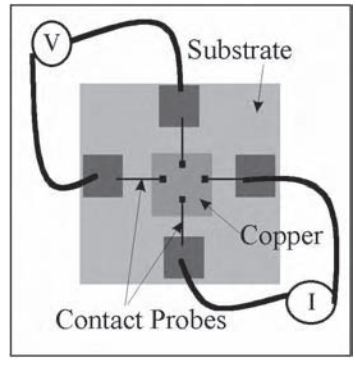


Figure 4.15 Four-point resistivity probe system

energy for the agglomeration instability and the fracture energy for the buckling instability.

In situ scanning electron microscopy (SEM) has been used to assess both instability mechanisms. The generic set-up is shown in Figure 4.14. Films can be heated at a varying ramp rate and images of the film analyzed to determine the spacing and height of islands or the height, width, and wavelength of buckles. Atomic force microscopy and profilometry are also useful tools to verify SEM measurements.

The onset and the activation energy of the agglomeration instability are most precisely determined by looking at the increase in resistivity of the film using a four-point probe. An example of such a configuration is shown in Figure 4.15. A voltage is applied and the current registering through the film is measured. The resistance is calculated from the voltage, the

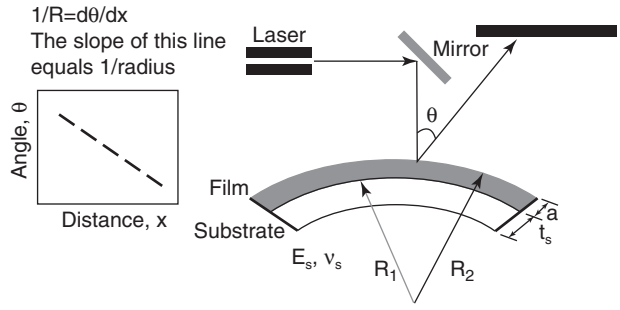


Figure 4.16 A schematic of the Flexus FLX-2320 system to measure film stress

current, and the known thickness of the film. Agglomeration occurs once the resistance increases dramatically, indicating that the continuous circuit path has been destroyed.

Stress levels in thin films are often assessed by measuring the curvature change of the substrate before and after the thin film has been deposited (Figure 4.16). This difference in curvature is used to calculate the stress using Stoney's equation [97]:

$$\sigma = \frac{E_s}{6(1-\nu_s)}\left(\frac{t_s^2}{a}\right)[K_{\text{after}} - K_{\text{before}}] \tag{2.5}$$

where $E_s/(1\text{-}\nu_s)$ is the substrate biaxial modulus, t_s and a are the substrate and the film thickness, and K_{before} and K_{after} are curvatures of the substrate before and after deposition respectively. The convention for curvature is such that if one follows the film's surface in Figure 4.16, starting from the left edge and moving to the right, the curvature will be positive if the concave side of the film lies to one's left and negative if the concave side of the film lies to one's right. Curvature is measured by directing a laser beam, with a known spatial angle, at a surface. The reflected beam strikes a position-sensitive photodiode and the geometry of the film is recorded by scanning the surface. In this way, the stress versus time or temperature can be obtained.

The adhesive or fracture energy of an interface can also be determined using four-point bending. Samples of interest are sandwiched between two elastic silicon substrates (350 μm thick) using epoxy. The samples are notched by using a low-speed diamond saw with notch depths near half of the silicon substrate thickness. These notches assist in initiating cracks used in determining the fracture energy. A load is applied to the specimen, as shown in Figure 4.17, at a constant strain (displacement) rate of 0.25 μm/s. The characteristic features of the load (stress) vs displacement (strain) curve are illustrated in Figure 4.18. Initially, the sample is crack-free and the load increases linearly with displacement. This linear relationship corresponds to the sample body stiffness. At a sufficiently high load, a crack originates from the notch and moves to the weakest interface in the stack. The crack then grows at a steady state rate at the interface. Between the inner loading points, the conditions are such that the moment stays constant. Consequently G, the energy release rate, is independent of crack length and the plot shows a plateau region. However, when the crack reaches the inner loading points, the load starts increasing again with a lower slope. This slope corresponds to the body stiffness of the cracked sample. The critical energy release rate for equal moduli and equal thicknesses as computed by Charalambides *et al.* [98] is given by:

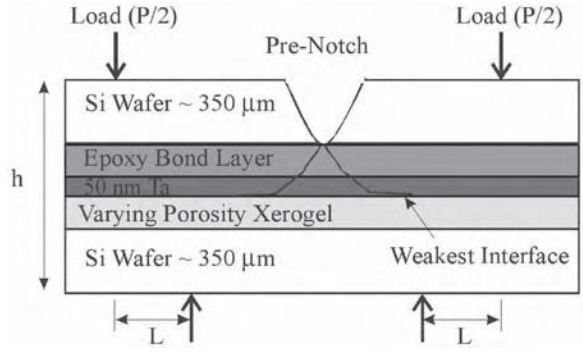


Figure 4.17 Sample geometry during four-point bending flexure test

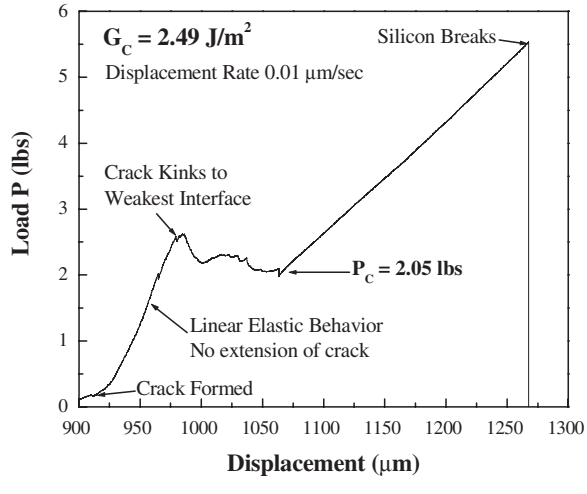


Figure 4.18 A typical load vs displacement curve during four-point bending. The fracture energy is calculated using the load plateau, which in this case is at 2.05 lb

$$G_c = \frac{21(1-\nu_s^2)P_c^2L^2}{16E_sB^2h^3} \tag{2.6}$$

where, ν is the poisson ratio, P_c is the critical load, L is the distance between the inner and outer loading points, E is the Young's modulus, B is the specimen width and h is the total thickness of one specimen ($h_1 + h_2$).

Experimental results: agglomeration

Thin metal films on solid substrates 'de-wet' or 'agglomerate' at elevated temperature and this behavior may lead to interconnect failure over time. The thermodynamic and kinetic

aspects of film agglomeration have been studied for a number of films on solid substrates [99, 100]. Agglomeration begins with the formation of a void in a continuous film. A critical void size exists, above which the void will grow to form disconnected islands. Heterogeneous nucleation by grain boundary grooving has been determined as the main cause of void formation [101]. Mullins [102] showed that a grain would groove to an infinite depth with time for an idealized planar geometry. Assuming a more realistic microstructure for grains, Nolan and Sinclair [103] showed that there exists an equilibrium grooving depth. Small grain sizes, low grain boundary energies and high film surface and interfacial energies were shown to promote resistance to agglomeration. Tensile stresses promote agglomeration while compressive stresses prevent grains from grooving, but lead to the formation of hillocks [104] instead.

Jain *et al.* [105] and Alford *et al.* [106] evaluated the stability of copper and silver films deposited on different underlying substrates upon heat treatment. They speculated that the underlying substrate morphology and chemistry could lead to the difference in observed behavior. Substrate roughness increases the effective interfacial area for the film and may affect the tendency toward agglomeration. A model for grain grooving on rough substrates was developed by Palasantzas [107] to assess this effect.

Dewetting is generally initiated by heterogeneous void formation [108] during annealing, and is driven by excess energy due to the presence of grain boundaries [109, 110], interfaces and surfaces [111–113], or due to residual stresses [114, 115] (see Figure 4.13). The mechanisms driving de-wetting and agglomeration have been addressed theoretically by a number of authors [108–116]. Experimental measurements of Au and Ag film agglomeration kinetics during annealing [117–121] have also been done.

One of the earliest studies on the kinetics of metal dewetting on glass substrates was undertaken by Kane *et al.* [117] using *in situ* resistance measurements coupled with *ex situ* scanning electron microscopy (SEM). They mapped the morphological changes in 6- to 8-nm-thick Au films encapsulated by graded layers of ZnS–CdS and calculated the activation energy of Au film breakup as 1.8 eV, corresponding to Au lattice diffusion. Jiran and Thompson [118, 119] using *in situ* transmission electron microscopy (TEM) and *in situ* laser scattering film reflectivity measurements, found two different activation energies for Au breakup on SiO_2, depending on whether the film was 40 or 90 nm thick. They attributed an activation energy of 1.2 eV to void nucleation, and 1.1–1.9 eV to void growth. The variation in activation energy was explained using an empirical model where the void growth rate was postulated to vary inversely with the cube of the film thickness a^{-3}. This model yielded an effective activation energy of 1.4 eV, implying that Au surface diffusion on the Au–SiO_2 interface was the rate-limiting mechanism. A similar activation energy dependence on film thickness has been observed for 35–165 nm Ag films by Presland *et al.* [120]. They reported a cubic dependence of incubation time on film thickness and activation energies of 0.64 eV for void nucleation and 0.71 eV for void spreading in a 118-nm-thick film. Following Presland *et al.*, Kim *et al.* [121] used a similar approach to obtain an activation energy of 0.32 eV for 35–70 nm Ag film de-wetting on SiO_2. These values are consistent with Ag migration at the at the Ag–SiO_2 interface being the kinetically limiting mechanism for film dewetting.

Due to the importance of Cu in microelectronic applications, morphological instabilities in nm-thick films of Cu on different dielectric substrates have been studied recently [122–124]. These studies have addressed the importance of substrate morphology and chemistry on Cu film de-wetting, but no attempt has been made to quantify the kinetics and underly-

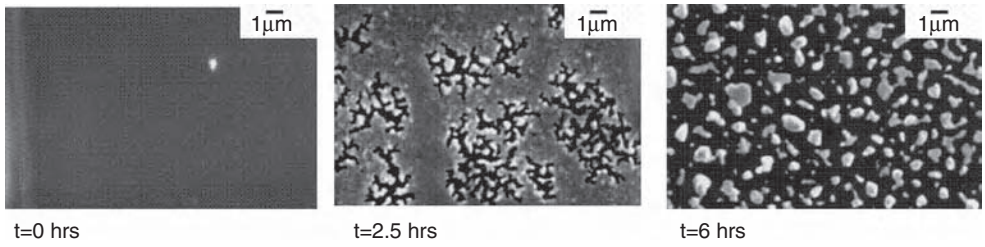


Figure 4.19 Different stages of annealing of a 50 nm copper film on PECVD oxide at 450°C with time. An initially flat film grooves and forms voids ($t = 2.5$ h) which grow to form separated islands ($t = 6$ h) (Reproduced with permission from Elsevier) [124]

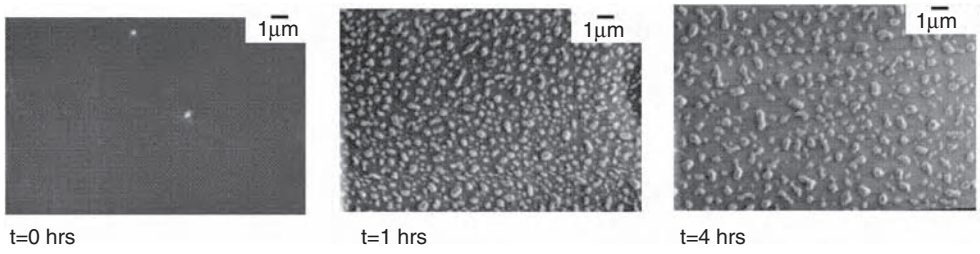


Figure 4.20 *In situ* annealing observations of void formation in a 20 nm copper thin film on PECVD oxide substrate. The film is annealed at 500°C for the times shown (Reproduced with permission from Elsevier) [124]

ing atomistic mechanisms governing break up. Efforts to model Cu film break-up have also suffered from a lack of experimental. The only model comparison was shown by Wong *et al*. [116] using the data of Jiran and Thompson [118, 119]. This model was successful at predicting the dependence of growth velocity on film thickness, but treated much thicker films than those of interest here.

Little data for Cu stability exists on porous substrates. As a thin film of Cu film on porous substrate is annealed, it goes through a series of changes in its shape as shown in Figure 4.19. Following an incubation time, voids start appearing in the film. This incubation time is believed to be the time required for the grain boundary to groove and reach the substrate forming a void. Thus, the incubation time is directly proportional to film thickness and inversely proportional to processing temperature (Figure 4.20).

Introducing porosity in the substrate leads to a rougher film–substrate interface and changes the available interfacial area for the film. The model for grain grooving on rough substrates proposed by Palasantzas [107] was used to correlate the behavior of Cu on nanoporous silica by Saxena *et al*. [124]. Using the values of interfacial energies and other model parameters for a Cu–SiO_2 (Table 4.2), a plot of the critical grain size to thickness ratio for the xerogel substrates is shown in Figure 4.21. The two surface area plots from atomic force microscopy (AFM) scans and ellipsometric porosimetry (EP) pore size distribution analysis imply that a copper film on a porous substrate should be more stable than on a solid substrate as can be seen in Figure 4.22 [124]. The AFM results predict a region of maximum stability very close to what is observed experimentally while the EP results over-predict the observed

Table 4.2 Model parameters used in calculating critical grain size to thickness ratio's and elastic energy contribution

Model Parameters	Value
γ_i for Cu/SiO_2	$0.43\,J/m^2$
γ_s for Cu/vapor	$1.2\,J/m^2$
γ_b for Cu grain boundary	$0.408\,J/m^2$
γ_{sv} for SiO_2/vapor	$0.1\,J/m^2$
E (Elastic modulus of copper)	110 GPa
ν (Poisson ratio of copper)	0.35
a_0 (Inter atomic spacing for SiO_2 used for area calculations)	0.3 nm

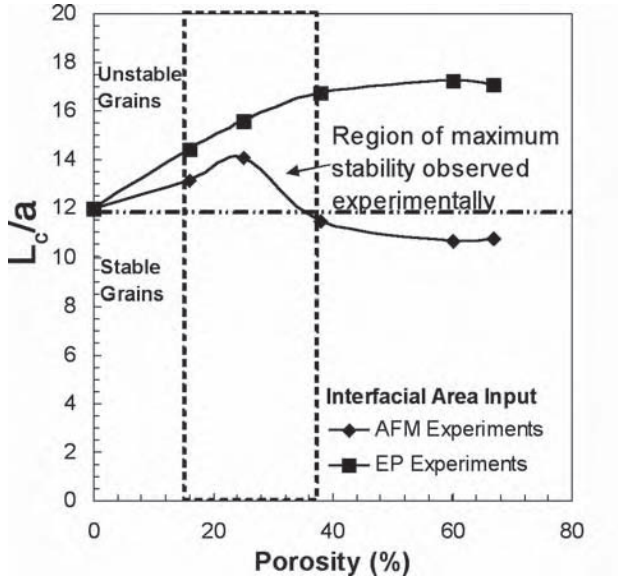


Figure 4.21 Critical grain size to thickness ratio calculated from experiments. The EP results over-predict the observed stability behavior, while the AFM slightly under-predicts (Reproduced with permission from Elsevier) [124]

stability maximum. A true surface area picture would require combining the surface profiles obtained from both AFM and EP and this might compare more favorably with experimental observations since the AFM results slightly under-predict what is observed experimentally.

Characterization of the substrates indicates that grooving is impeded for higher micro-roughness, which occurs for lower porosity substrates. Thus, porous substrates offer an increased stability towards grain grooving than for films on solid substrates due to an increased film–substrate interfacial energy. Stress does not govern the interactions in our

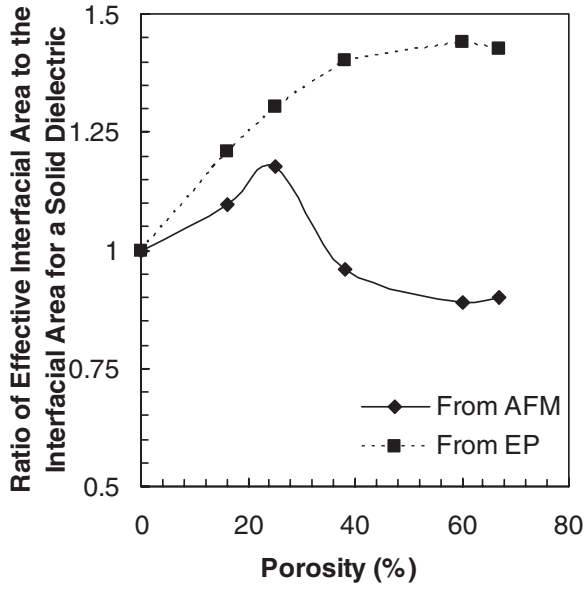


Figure 4.22 Ratio of effective interfacial area calculated using the two different methods from experimental data and parameters in Table 4.2 (Reproduced with permission from Elsevier) [124]

experimental system as the stress energy is an order of magnitude lower than the surface/interfacial energies.

These experimental results do not address the kinetics of the instability and so are of limited utility in trying to determine the lifetime of an interconnect. The kinetics of Cu agglomeration on a porous material are unknown, and even for Cu on solid SiO_2, there are no good quantitative data. The kinetic issues on solid SiO_2 have been recently addressed by Saxena *et al.* [125]

In this work, sub-60-nm-thick Cu films, deposited on solid SiO_2 were annealed at temperatures ranging from 300 to 600°C. De-wetting was observed using *in situ* electrical resistance, *ex situ* scanning electron microscopy and atomic force microscopy measurements. Resistivity versus temperature and scanning electron micrographs for the dewetting films are shown in Figures 4.23 and 4.24.

Two critical temperatures, T_{c1} and T_{c2}, were observed for thinner films and only one, T_{c2} for the thicker films. Analysis of this temperature behavior led to the assertion that sub-60-nm Cu films on silica de-wet by two different pathways, depending upon the film thickness. Films that were thinner than 20 nm de-wet in a sequence of two distinct steps: void nucleation by grain boundary diffusion (activation energy 1.2 eV) followed by void growth and islanding by Cu surface spreading (activation energy 0.7 eV). The activation energy determinations are shown in Figure 4.25(a,b).

For thinner films, the step of void growth by surface spreading is the rate-controlling step because grooves rapidly extend to the Cu–silica interface, after which the intergranular voids grow via Cu atom transport on the silica surface, leading to islanding. In thicker films the rate-limiting step for de-wetting is grain boundary grooving (activation energy 1.2 eV). By the time the grooves initiated at the film surface and the Cu–silica interface merge and

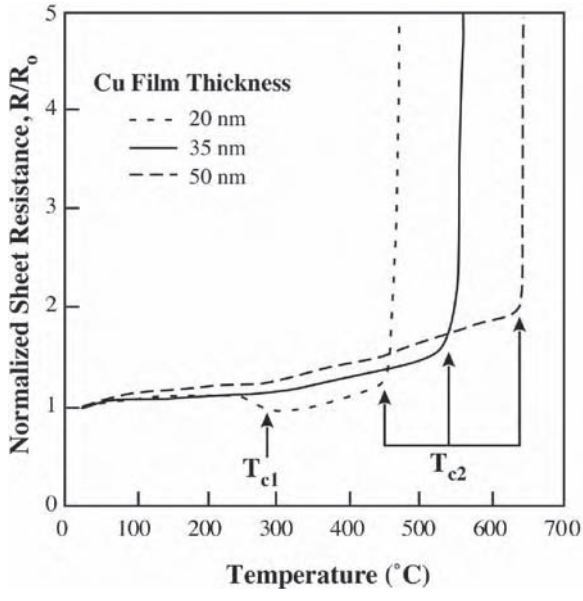


Figure 4.23 Normalized sheet resistance of thin, Cu films deposited atop an SiO_2 substrate. Steep increase in resistance vs temperature indicates the loss of film continuity and onset of islanding (Reproduced with permission from the American Physical Society) [125]

span the film thickness, the lateral spatial extents of the voids is already large, and separate Cu islands are essentially formed. Thus, in addition to the well-known grain boundary grooving mechanism, surface diffusion of Cu at the Cu–SiO_2 interface can serve as an additional de-wetting pathway if the grooving process occurs across a short length scale, i.e., in thinner films. An important consequence is that de-wetting can be suppressed in ultra-thin films if surface diffusion at the film–substrate interface is curtailed, e.g., by enhancing the bonding interactions at the interface via substrate surface modification and processing [126, 127].

Experimental results: buckling

Films under compressive stress tend to fail by a buckling mechanism. In general, diffusion barrier materials are often deposited with significant compressive stresses and hence fail by buckling. Tantalum and tantalum-based films are commonly used as diffusion barriers and adhesion promoters in the current Cu interconnect technology. While much effort has been made to characterize the phase stability and diffusion barrier properties of these barrier layers [128–130], few studies have focused on their adhesive and fracture properties [131–135]. In particular the adhesion of barrier layers to porous dielectric substrates has not been studied in detail [136–139].

Adhesion is defined as the total energy required to separate an interface, measured in terms of a critical value of the debond strain energy release rate or an interface debond

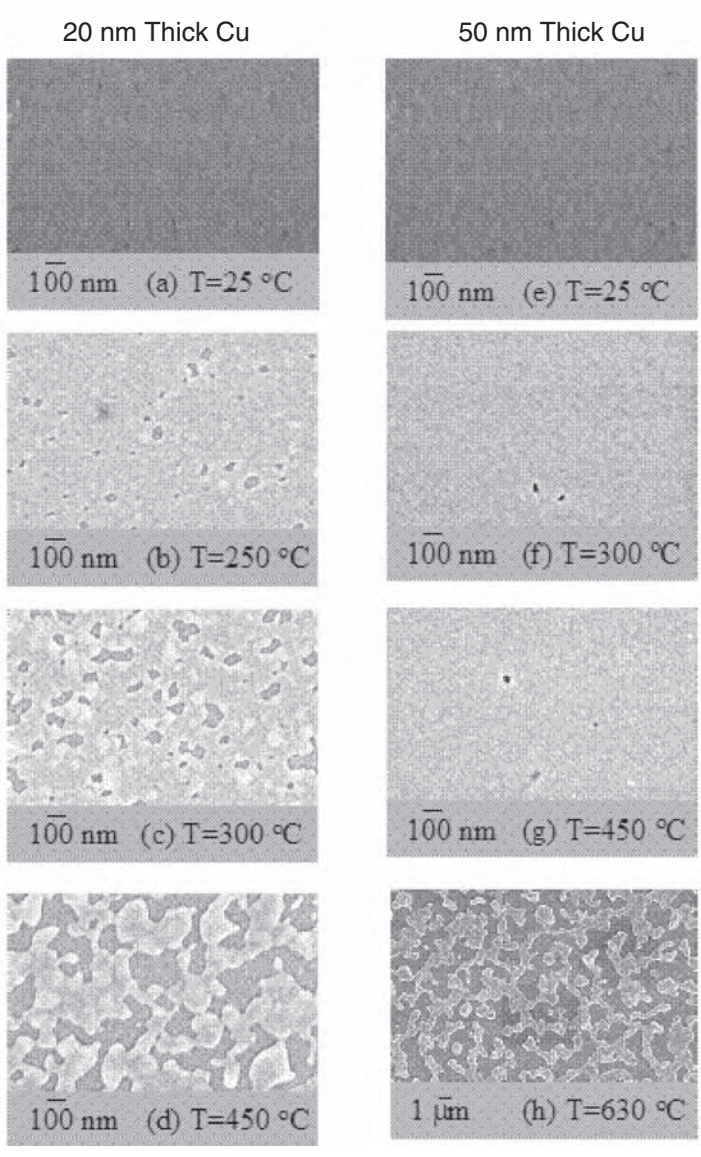
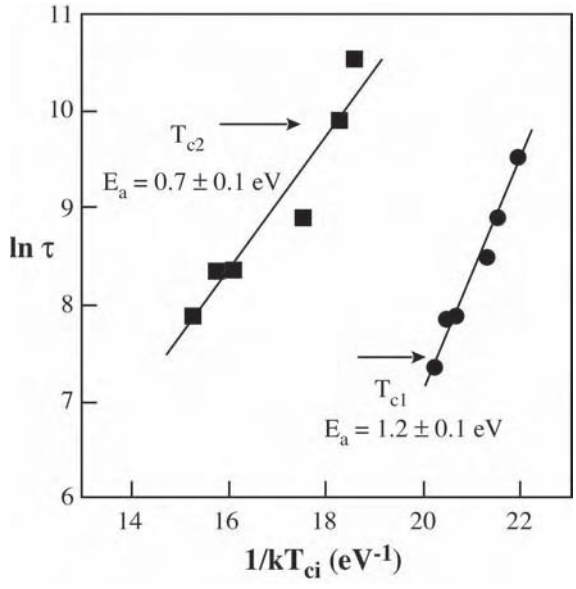
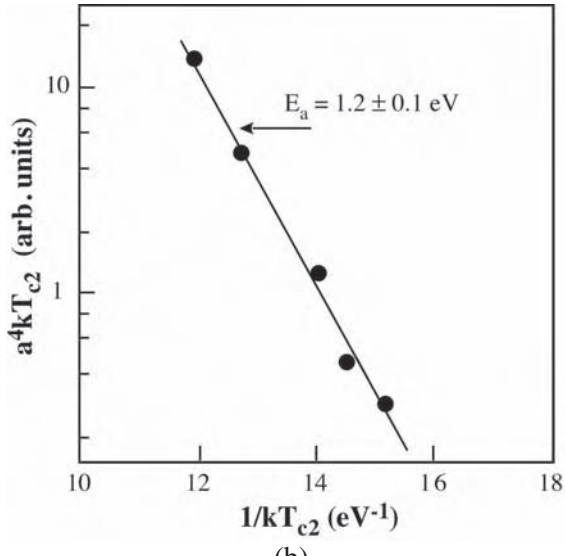

20 nm Thick Cu
50 nm Thick Cu
100 nm (a) T=25 °C
100 nm (e) T=25 °C
100 nm (b) T=250 °C
100 nm (f) T=300 °C
100 nm (c) T=300 °C
100 nm (g) T=450 °C
100 nm (d) T=450 °C
1 μm (h) T=630 °C

Figure 4.24 Representative SEM micrographs depicting the morphological change in 20- and 50-nm-thick Cu films. The images were captured from samples annealed to the indicated temperatures, and cooled to room temperature (Reproduced with permission from the American Physical Society) [125]

energy, G_c (J/m^2). This energy includes the breaking of chemical bonds across the interface and plasticity in any adjacent ductile layer. Energy dissipation in debond wake processes (such as a frictional contact zone) must also be considered [140, 141]. A variety of methods exist to measure adhesion between thin film interfaces. Volinsky *et al.* [142] and Lane [143] provide good reviews of the techniques applicable to the IC industry. Delamination is



(a)



(b)

Figure 4.25 Activation energy determinations for thin films: (a) Arrhenius plots for thermally activated processes characterized by temperatures T_{c1} and T_{c2}. The characteristic times τ were obtained for different ramp rates between 0.5 and 10°C/min for a 20 nm-thick Cu film on SiO_2; (b) plot using the modified Mullins model [102] to determine the activation energy of the thermally activated process characterized by T_{c2}, measured for films with different thicknesses at the annealing rate of 6°C/min (Reproduced with the permission of the American Physical Society) [125]

intentionally induced in most tests to measure adhesion and hence these measurements are error prone. They are fairly easy to do and relatively quick.

A systematic investigation of the dependence of barrier layer interfacial adhesion on the porosity and average pore size of the dielectric substrate has not been undertaken. Most studies [136–139] have looked at only a very limited range of porosity and pore size. The difficulty in obtaining the data arises both in the preparation of material with controlled internal properties and also in the testing methodology. No real correlation has been obtained between a film's mechanical properties and substrate porosity in previous work. In the paragraphs below we will discuss some recent work.

Deposited barrier films (Ta and TaN) delaminate from low-k substrates beyond a certain critical thickness h_c, where the elastic energy stored in the film exceeds the critical fracture energy at the interface. The delamination pattern observed depends upon the underlying dielectric type, the dielectric's porosity and the film thickness. Several types of patterns are shown in Figure 4.26. Cords generally start from an imperfection within the film or from edge delamination (Figure 4.26a). The tip of the cord is parabolic. The wavy pattern associated with the telephone cord develops behind the tip as it propagates. In addition to telephone cords, straight-sided blisters (Figure 4.26b) are also observed in some films. Here we will concentrate our observations (but not limit) to the telephone cord geometry in Figure 4.26c.

Cross-sectional views of the films taken using scanning electron microscopy illustrate that the film delaminates from the substrate, but is clamped at the edges (Figure 4.27). To obtain the critical thickness h_c, many different thicknesses of Ta were deposited on different substrates. The film–substrate combination was left under ambient conditions for a day before taking observations. Three different cord parameters were measured: the height of the buckle δ, the half-width of the buckle b and the wavelength of the cord λ. These were obtained using a combination of optical microscopy and profilometry. The different cord parameters and the critical film thickness for a number of nanoporous silica interlayer dielectrics and MSQ are listed in Table 4.3.

For a thin film of critical thickness h_c, subject to a equi-biaxial compressive stress σ, the stress relief mechanism results in a straight sided buckle with the film displacement δ, normal to the surface and a buckle width of $2b$. This is a one-dimensional approximation to the actual two-dimensional telephone cord buckle. The critical stress for buckling in this approximation is given by [144]:

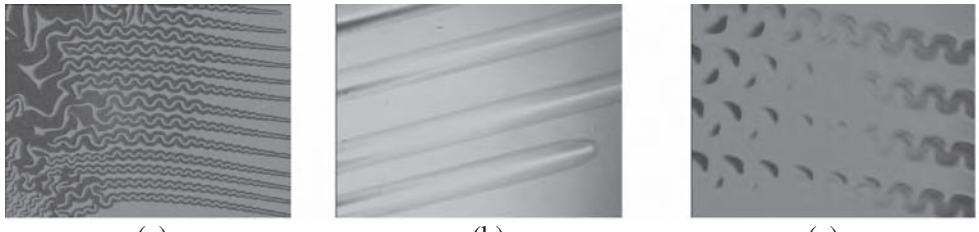


Figure 4.26 Telephone cords (t-cords) for Ta on MSQ of 35% porosity: (a) semi-developed telephone cords; (b) straight buckles across the film; (c) fully developed telephone cords used for characterization

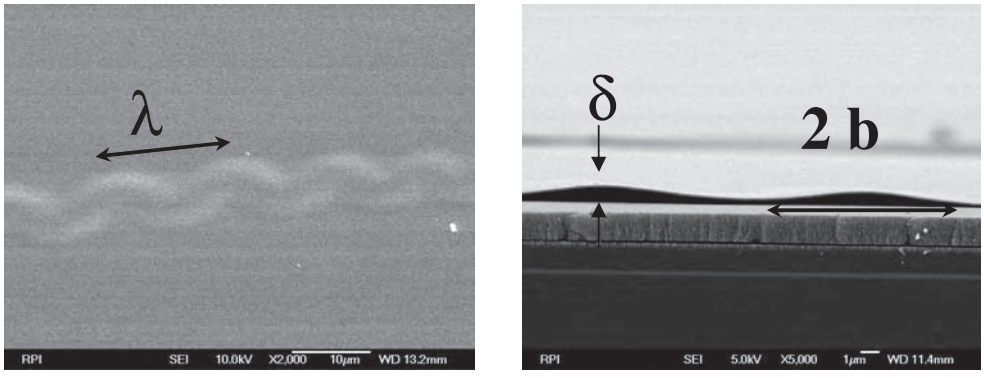


Figure 4.27 The different cord parameters observed on 50 nm TaN on 60% xerogels

Table 4.3 Parameters for fully developed telephone cords of Ta on different ILD materials

Sample Porosity (%)	Width $2b$ (μm)	Wavelength λ (μm)	Height δ (μm)	Critical thickness h_c (μm)
As-deposited nanoporous silica				
32	176	188	7.18	1.2
48	106	101	4.38	0.75
58	27	26	1.08	0.3
Sintered nanoporous silica				
36	342	273	14.39	1.8
54	58	61	2.65	0.6
61	52	46	2.19	0.45
MSQ (methylsilsesquioxane)				
35	55.2	55	2.42	0.6

$$\sigma_c = \frac{\pi^2 E}{12(1-\nu)}\left(\frac{h_c}{b}\right)^2 \tag{2.7}$$

where E and ν are the Young's modulus and Poisson's ratio of the film, respectively. This is essentially Stoney's equation. The residual stress in the film after buckling is given by:

$$\sigma_r = \sigma_c\left[\frac{3}{4}\left(\frac{\delta}{h_c}\right)^2 + 1\right] \tag{2.8}$$

Using these parameters, the interfacial fracture energy is given by:

$$G_c = \left(\frac{1-\nu^2}{2E} h_c\right)(\sigma_r - \sigma_c)(\sigma_r + 3\sigma_c) \tag{2.9}$$

The generally accepted testing procedure for measuring the fracture energy is the four-point bending test. The load is applied to the specimen, at a constant displacement rate of 0.25 μm/s. The critical energy release rate for equal moduli and equal thicknesses as computed by Charalambides *et al.* [145] is given by:

$$G_c = \frac{21(1-\nu^2)P_c^2 L^2}{16 E_s B^2 h^3} \tag{2.10}$$

where P_c is the critical load, L is the distance between the inner and outer loading points, B is the specimen width and h is the total thickness of one prepared specimen.

Using the telephone cord parameters and Equation (2.9) the calculated fracture energies are shown in Figure 4.28(a) as a function of substrate porosity. The fracture energy of the Ta–Porous dielectric interface decreases with an increase in porosity for all types of films tested (as-deposited, sintered and MSQ). The fracture energy was also calculated using four-point bending and the results are shown in Figure 4.28(b). Fracture energy decreases with increasing substrate porosity as was observed with telephone cord measurements.

While the trends in fracture energy are the same for both four-point bending and telephone cord analyses, the magnitude of the fracture energy is different and in some cases the porosity range that can be assessed is different. Interfacial adhesion is characterized by the critical strain energy release rate G_c, which varies as a function of the phase angle Ψ, according to:

$$\Psi = \tan^{-1}\frac{\sigma_{22}}{\sigma_{12}} \tag{2.11}$$

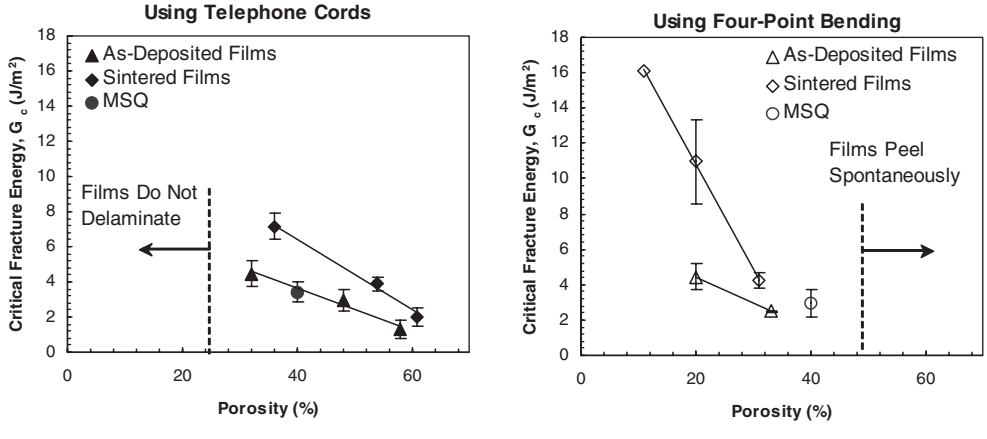


Figure 4.28 Fracture energy calculated for different types of films from: (a) telephone cord observations using a one-dimensional model; (b) four-point bending analysis

As the ratio between in-plane shear stress σ_{12} and the normal stress σ_{22} at the crack tip increases, the critical energy release rate increases and reaches a maximum at $\Psi = 90°$. Thus, it is important to interpret adhesion results with respect to the specific loading geometry and samplestacking configuration employed [146]. The two tests, four-point bending and telephone cords, employ different geometries and hence different phase angles. This could be one possible reason for the different values obtained. The phase angle for the four-point bending geometry is 42°. There is some discrepancy in the literature regarding the phase angle for telephone cord tests. Gioia and Ortiz [147] reported a phase angle of 52° and maintained that this was constant as the blister spread. However, a recent article by Lee *et al.* [148] reported a phase angle of −89°. Lee *et al.* claimed that as the telephone cord blister grows, the crack front takes on an increasing mode II component and makes the interface effectively more fracture resistant.

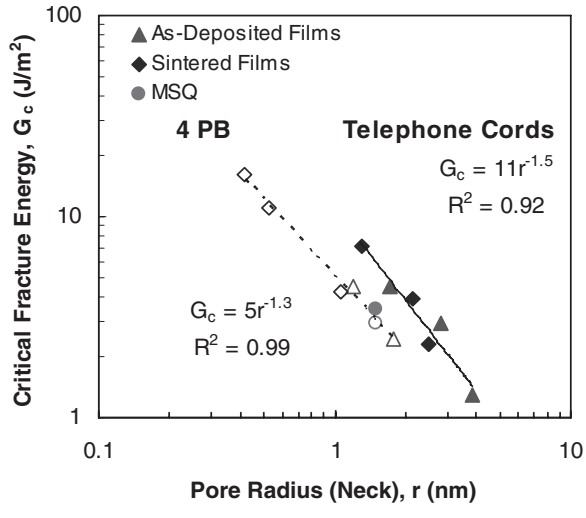
The data reported in Figure 4.28 for Ta films on 35% porous MSQ substrates give values of $2.96 \pm 0.77\,J/m^2$ and $3.43 \pm 0.6\,J/m^2$ for four-point bending and telephone cords, respectively. For the same interface, the telephone cord tests yield a higher value of fracture energy confirming that they do have higher mode II contributions. Lee *et al.* [148] compared the four-point bending and telephone cord tests by using a phenomenological model for interface fracture energy as a function of mode mixity [140]. The interface fracture energy $G_c(\Psi)$ for a given mode mixity phase angle of Ψ is given by:

$$G_c(\Psi) = G_{1c}\{1 + \tan^2(1-\lambda)\Psi\} \tag{2.12}$$

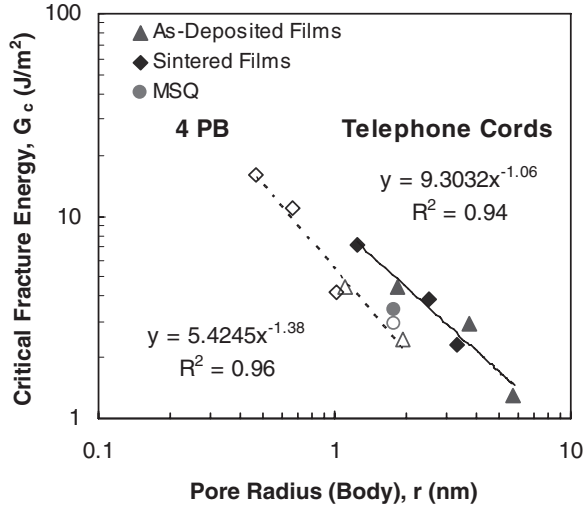
where G_{1c} represents the mode I interface fracture energy and λ is a mode sensitivity parameter obtained from fitting the experimental data. λ is commonly set at 0.2–0.3 for most experimental systems. Using Equation (2.13), Lee *et al.* [148] reduced the four-point bending fracture energy from a phase angle of 43° to −89° to compare with the telephone cord tests. Although, they got a good comparison between the two tests, the phase angle for telephone cord tests is still not known unambiguously.

Another comparison of the two tests can be made on the basis of the fracture efficiency parameter [149, 150]. The fracture efficiency parameter for self-delaminating telephone cord tests is calculated to be 0.5 and is independent of the phase angle, while for four-point bending tests, the efficiency parameter is 0.1, indicating that the telephone cord tests are more efficient. Even though the values of fracture energy obtained from the two tests are different, the trend is the same. The two tests corroborate the results of fracture energy for different samples tested, thus conforming that the internal properties of the porous dielectric are related to the energy release during the delamination of contiguous Ta films.

The major difference between the types of substrates tested is their porosity and pore size distribution. The MSQ substrate varies slightly in terms of chemistry compared to the sintered and as-deposited films. The pore size distributions of the different porous substrates were previously measured [151]. Using the pore size information, the critical fracture energy data collapses on one curve for a particular test and is shown in Figure 4.29(a,b). The fracture energy exhibits a power law dependence on the pore neck or body radius with an exponent of −(1.2–1.3) and −(1.5–1.6) for the four-point bending and telephone cord test results respectively. This implies that the governing property controlling fracture is actually the pore size distribution and not the porosity. G_c obtained for Ta-MSQ lies on the curve obtained for Ta-xerogels for the four-point bending test while it deviates from the curve for the telephone cord tests. This, along with the earlier discussion on fracture efficiency



(a)



(b)

Figure 4.29 Critical fracture energy data plotted using measured: (a) pore neck size; (b) pore body size, for different porosity films

suggests that the telephone cord measurements might be more sensitive to changes in interface chemistry. Varying the porosity of MSQ substrates or other porous dielectrics would be needed to test this hypothesis and see if this behavior is generic to all porous dielectrics and not just to xerogels.

The power law dependence of fracture energy on pore size for different porosity and pore size distribution films can be due to either a roughness effect of the porous dielectric which increases the shielding contribution from the interface between the film and dielectric

during crack propagation or an intrinsic failure property of the porous low-*k* dielectric. Each of these factors is analyzed separately.

Interface roughness

Energy dissipation due to interfacial roughness may manifest itself in a number of ways, each of which will have its own dependence on the amplitude and the wavelength of the roughness. One possibility for change in fracture energy due to nonplanarity may be understood by consideration of the Griffith criterion for fracture, which indicates the energy required to separate two surfaces depends on the total area of separation [152]. For a planar interface, this is simply the length of the debonding crack times its width. However, for a debond that deviates from a planar path, an increase in the total debonded area occurs, leading to an increase in interface fracture energy that scales with the true debonded area over the planar area. A second possibility for a change in the fracture energy is that as the debond travels along the interface the debond tip propagation direction relative to the direction of the far-field applied loading may change. This change in debond orientation results in a change of the near-tip stress state and therefore a change in the debond driving force or energy release rate [153]. The final possibility to be considered is asperity contact behind the debond tip, which acts to shield the debond from the applied loading [154]. Models that account for each of these factors are very difficult to construct and implement in a straightforward manner. A simple model was proposed by Evans and Hutchinson [154] in which an idealized interface morphology, composed of one roughness and wavelength, was examined. They proposed that the effectiveness of shielding manifests itself in terms of a shielding parameter given by:

$$\chi = \frac{Ew^2}{\xi \Gamma_0} \tag{2.13}$$

where w is the amplitude of the roughness, ξ is the wavelength, E is the elastic modulus and Γ_0 is the work of adhesion. A good review by Lane [155] investigates the effects of interfacial roughness on fracture.

To determine whether the decrease in fracture energy is due to a surface area effect, AFM measurements were made on the different dielectric surfaces used for the telephone cord experiments. These experiments yielded the values for w and ξ needed in Equation (2.13). The corresponding shielding parameters for the different films are plotted in Figure 4.30. The shielding parameter increases with increasing pore sizes and hence, interfacial roughness cannot account for the decrease in fracture energy with increasing pore sizes.

Fracture at interface: crack path model

If shielding is not an issue, then one needs to look at the physical properties of the porous substrate, namely the morphology and chemistry, to uncover why the fracture energy depends on pore size. Fundamentally, the fracture energy is the work done to separate bonds per unit area of the interface. This implies that fracture energy is proportional to the bond strength of breaking bonds (weak sites) and the total number of bonds that are breaking.

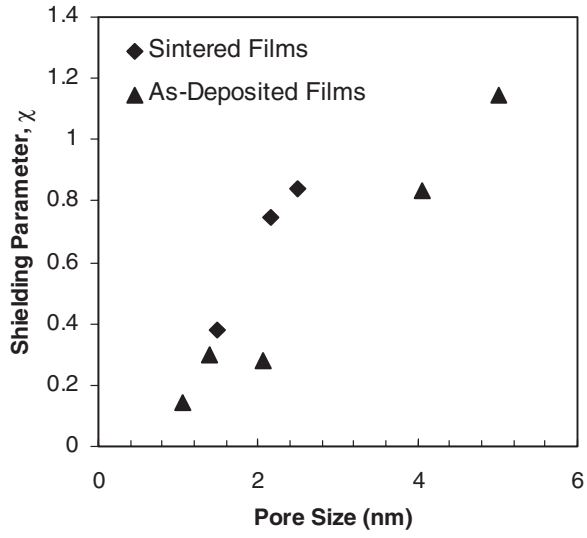


Figure 4.30 Shielding parameter calculated using the AFM parameters for different films and Equation (2.13) with $E = 350\,\text{GPa}$ and $\Gamma_0 = 10\,\text{J/m}^2$ for a Ta/SiO_2 interface

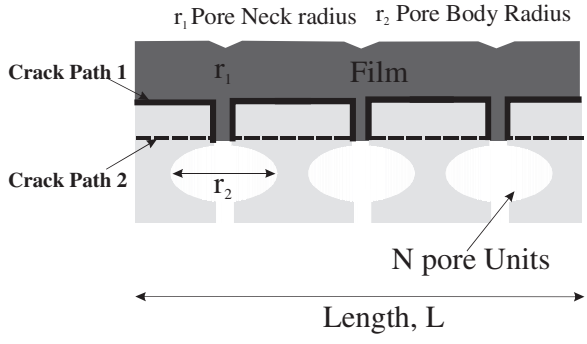


Figure 4.31 A simplified schematic of the fracture interface between Ta and porous xerogel, showing the two possible paths that a crack can take

Thus, the weak sites in the interface need to be identified and quantified to explain the fracture energy trend with varying substrate porosity. A simplified model of the Ta–porous substrate fracture interface is presented in Figure 4.31.

The pores are visualized as consisting of necks (r1) and bodies (r2) with the respective radii dependence on porosity that is known from ellipsometric porosimetry measurements. The Ta layer fills up the necks of the underlying substrate and there exists a graded substrate (Si/O/C) and film (Ta) layer whose thickness increases with. This graded layer is seen in X-ray photoelectron spectroscopy scans of the fractured surface. Delamination needs a flaw in the interface for nucleation and this flaw is provided by the pores in the underlying substrate. There are two possible delamination (crack) paths that the Ta layer can take during

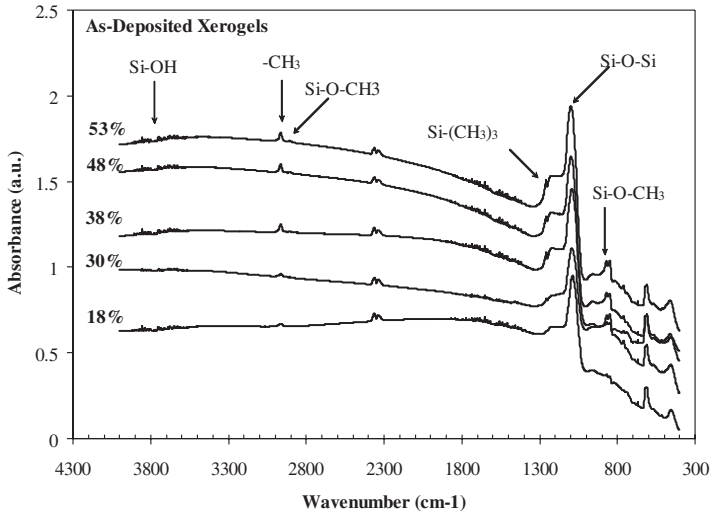


Figure 4.32 FTIR Spectra of as-deposited Xerogel at varying porosities. Area under the different peaks labeled gives an indication of the number density of the bonds

fracture testing. Crack path 1 implies the Ta layer delaminates along the interface, while path 2 implies cracking of the substrate.

The chemical structure of the dielectrics was studied using a NICOLET Model Magna 560 FTIR spectrometer in the transmission mode. The FTIR traces for the as-deposited xerogel of different porosities are shown in Figure 4.32. For all porosities, there is no obvious peak centered at 3200–3600 cm^{-1}, which is related to moisture absorption [156]. Furthermore, molecular water absorbed on the surface exhibits a spectral peak centered at 1650 cm^{-1}, which is absent for these substrates confirming their hydrophobic nature. Peaks at 2980 and 1260 cm^{-1} represent the $–CH_3$ and $Si–CH_3$ groups, respectively, from the surface modification step during fabrication. The extent of these groups increases with porosity indicating that the organic content in the substrates increases with porosity [157]. A similar spectrum is obtained for sintered xerogel (Figure 4.33).

A cage-like Si–O–Si structure can be seen for the sintered samples that differs from the network-like arrangement in the as-deposited xerogel substrates. Also the samples display $–CH_3$ and $Si–CH_3$ peaks at 2980 and 1260 cm^{-1}, respectively. The $Si–CH_3$ peak is overshadowed by the Si–O–Si peak, making quantification of the bonds using this peak difficult. Thus, the $–CH_3$ peak is used to quantify bonds in these substrates. The number of $–CH_3$ will be proportional to both the amount of Si–C bonds and the Ta–C bonds in the substrate and the interface, respectively. Using the FTIR and XPS analysis, the different bond types in the substrate and at the interface can be determined and are shown in Figure 4.34 while the bond energies for these bonds are listed in Table 4.4 [158].

Based on Table 4.4 one can conclude that the weakest ‘chain’ linkages in the substrate and interface are Si–C and Ta–C respectively. The C–H is not part of the backbone or chain and breaking of those bonds will not result in delamination. Using this information, one can compare the different crack paths available for fracture in Figure 4.31. Ta–C is the

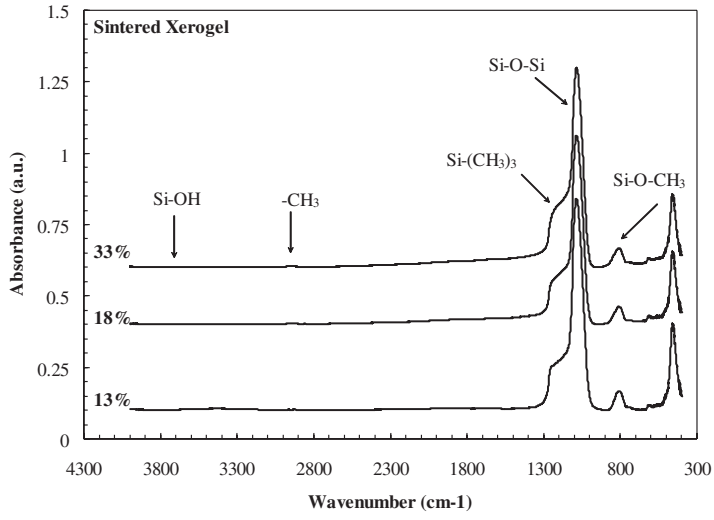


Figure 4.33 FTIR spectra for sintered films (sintered at 1000°C) showing a cage-like Si–O–Si structure that is different from the as-deposited network like structure

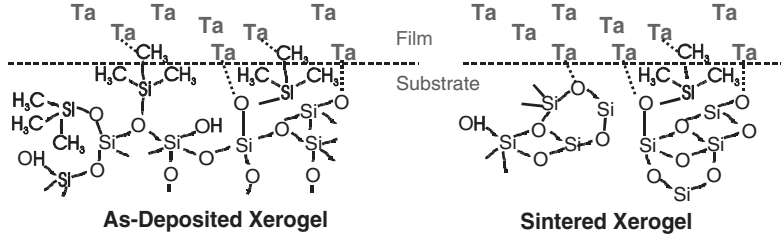


Figure 4.34 Chemical bonds in the film, substrate and interface inferred using FTIR and XPS analysis

Table 4.4 Strengths of the different bonds in the film and substrate [158]

Bond type	Strength (KJ/mol)
C–H	338
Si–C	451
Ta–C	500
C–C	610
Si–O	799
Ta–O	799

weak linkage in crack path 1, while Si–C is the weak linkage in crack path 2. The work done (fracture energy) for separating the interface is given by:

$$W \equiv G_c \propto \frac{A_i B_{Si}}{N_i} \tag{2.14}$$

where, i = 1,2, A_i represents the area, B_{Si} represents the bond strength of the weakest site and N_i represents the average bond density of the weakest site. The number density, N_i of Si–C and Ta–C will be approximately the same at the interface as each C will form an interfacial Ta carbide. The area of path 2 will always be less than that of path 1 as it is the projected area between the pores. Also $B_{S1} > B_{S2}$ (Ta–C vs Si–C). Thus, the work done will always be less for crack path 2 and delamination will occur in the substrate. This is supported by the XPS analysis where the fracture surface (graded layer of Si/O/C/Ta) was shown to move deeper into the substrate with increasing porosity.

The bond density in Equation (2.15) N_i is obtained from FTIR, while the area is obtained from the calculated pore size distribution. Data from the different films is plotted as a function of pore neck radius in Figure 4.35. The effective interfacial area decreases as with an exponent of around −(0.34–0.38) for as-deposited and sintered substrates. This is due to the pores becoming larger as the porosity increases. The organic content increases with increasing porosity and this varies with pore radius with an exponent of 0.79–0.81 for sintered and as-deposited respectively. The lower number of bonds and smaller pores in the sintered substrates imply that the fracture energy will be higher when compared with as-deposited films, which matches the trend shown in Figure 4.28 for both tests.

The calculated distributions in Figure 4.35 are substituted in Equation (2.10), yielding a fracture energy power dependence of $n \sim -(1.1–1.2)$ which matches well with the experimentally determined exponent of $n \sim -(1.3–1.5)$. The model implies that a variation in chemistry with changing substrate porosity is the governing factor over interfacial area for fracture of bonds. This chemistry variation is a consequence of the surface modification of the present samples and may or may not apply for all porous dielectrics. However, the

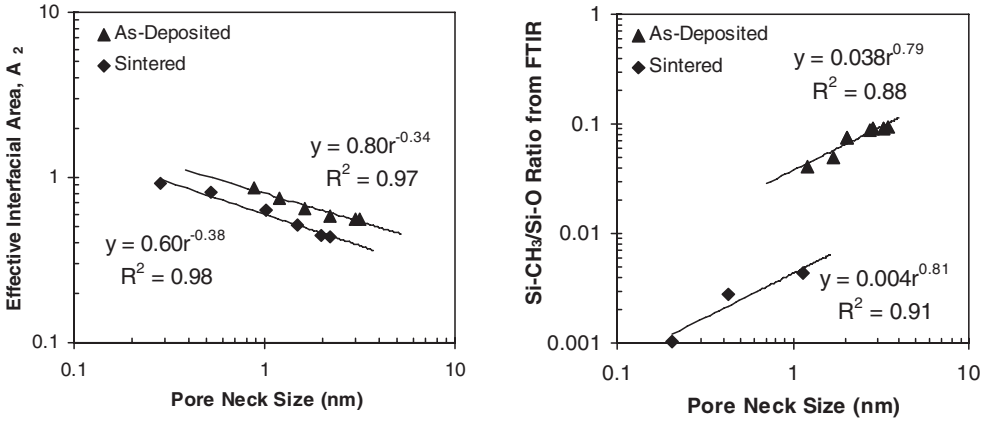


Figure 4.35 The effective interfacial area calculated using ellipsometric porosimetry pore size distribution and bond ratios calculated using FTIR spectra as a function of pore neck size

interfacial area will always decrease with increasing substrate porosity, implying that a pore size dependence on fracture energy should be applicable to all Ta–porous substrates.

4.3 THERMAL PROPERTIES OF LOW-*k* MATERIALS

4.3.1 Thermal stability

The concept of thermal stability encompses a number of issues, including changes in composition and changes in structure. While most authors refer to stability as the onset of weight loss, other significant changes can occur prior to weight loss such as phase transformation. Hybrid materials in general lose their organic content at a certain characteristic temperature while the inorganic component remains. At higher temperatures, the inorganic component begins to sinter and for porous materials, their structure changes. Table 4.5 summarizes the stability of several of the well-known low-*k* materials. Stability temperatures represent a maximum value for each class of material.

As an example of how a hybrid material behaves, Figure 4.36 shows the results of the mthermogravimetric analysis of an as-prepared, mesoporous silica film with 56% porosity. At temperatures up to 300°C, the weight change is negligible and represents predominantly adorbed water. Above 300°C, the weight decreases with a constant slope up to ~450°C [167], representing the loss of some bound water and bound alkoxy and solvent groups left over from the sol–gel reaction. Between 450 and 600°C there is a steep weight loss, representing the loss of surface methyl groups used to render the material hydrophobic. Beyond 600°C, sintering occurs and water is lost as a result of Si–OH condensation reactions.

To verify the previous TGA results, FTIR scans were done over a wide range of temperatures using the same 56% porosity film used in the TGA study. As described in Figure 4.37, our interests are in the water molecule (3400, 1627 cm^{-1}), single OH (3750 cm^{-1}), paired OH (3540 cm^{-1}), internal hydrogen-bonded OH (3650 cm^{-1}), and CH_3 group (2977 cm^{-1}) stretches. The data indicate that there is no free water, no internal hydrogen-bonded OH, or paired OH in the film due to lack of peaks in those regions. Distinct peaks exist showing

Table 4.5 Low-*k* dielectric material stability

Material	Temperature (°C)	Comments
Polyimides	<500	Maximum glass transition temperature [159]
Polybenzoxazole	<500	[160]
Polyarylether (Flare)	~450	[161] Values for first generation
SiLK	500	[162]
Benzocyclobutene	375	[163]
MSQ, HSQ and derivatives	500	[164] Organic components removed
PTFE-type	450	[165]
Nanoporous silica	400–500	Organic surface modification components removed. Sintering begins
Parylenes	400	[166] Phase transformation at 230°C Isothermal thermogravimetry

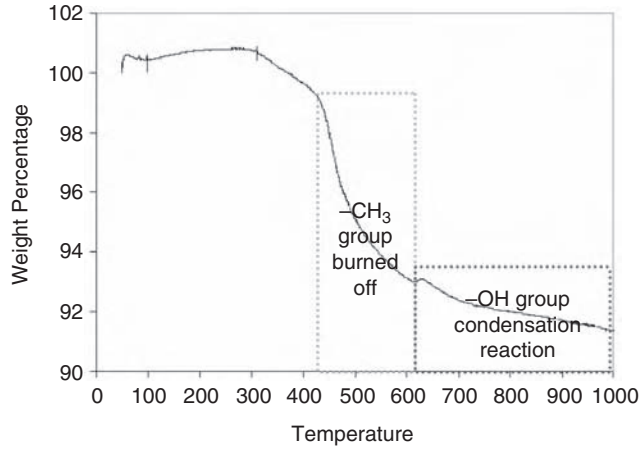


Figure 4.36 The thermal gravimetric analysis (TGA) result of nanoporous silica film, a porosity of 56%, with 10°C/min scan rate (Reproduced with permission from Elsevier) [168]

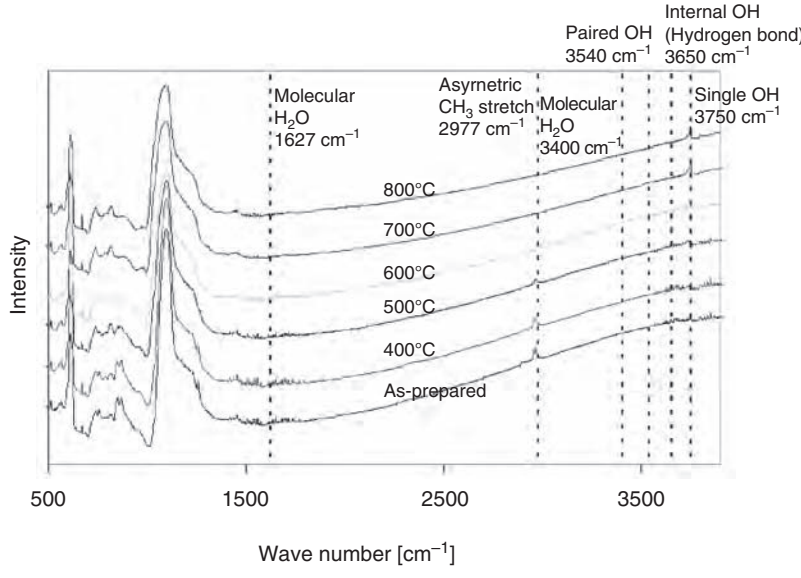


Figure 4.37 FTIR results of the nanoporous film as a function of temperature (Reproduced with permission from Elsevier) [168]

CH_3 (2977 cm^{-1}) and single OH (3540 cm^{-1}) groups. These groups do not coexist in that there are no OH peaks in as-prepared films treated at 400 and 500°C. The OH peaks begin to appear only at higher temperatures in the absence of CH_3 groups. The intensity of the CH_3 peak is reduced in the 500°C sample when compared with the 400°C sample, indicating that the CH_3 groups begin to be removed and finally disappear after 600°C. The surface modification procedure cannot replace all the residual –OH groups in the material due to diffusion and thermodynamic limitations of small pores. Thus, the weight decrease beyond

600°C implies the removal of –OH groups due to a condensation reaction leading to Si–O–Si groups. The Fourier transform infrared spectroscopy results in Figure 4.37 verify this conclusion.

4.3.2 Thermal conductivity of low-*k* dielectric films

One of the major impediments to introducing low-*k* materials into integrated circuits is concern over heat dissipation. With microprocessors dissipating in excess of 500 000 W/m^2 any decrease in the thermal conductivity of the dielectric poses severe challenges to microprocessor design. Joule heating [169] is driven by the active devices in microprocessors and these devices are relatively inefficient switches. The metal interconnects, especially copper, are efficient conductors of heat, but the metal lines and vias are not currently designed, for heat removal from chips [170]. Thus, maximizing the thermal conductivity of the dielectric is imperative.

Heat dissipation is also a problem during back-end-of-the-line processing. Chemical mechanical planarization (CMP) is basically a frictional process that generates a lot of heat and may produce hot spots, leading to film delamination [171]. Small decreases in the thermal conductivity of dielectrics, in conjuction with variations in interconnect geometry can cause large changes in heat flux and sudden increases in the interconnect temperature [172]. Thus, understanding the fundamental mechanisms underlying thermal transport in dielectric films is essential to the efficient thermal design of integrated circuits.

A number of excellent reviews of thermal processes in dielectrics have appeared recently by Goodson and Ju [173], Cahill [174], Goodson *et al*. [175], and Cahill *et al*. [176]. In this section, we present information on the thermal conductivity of low-*k* materials and the relationship between thermal conductivity and elastic modulus. The differences in conductivity between the films can be explained qualitatively by disorder in the films that affects phonon transport and scattering.

Thermal transport: theoretical considerations

Of the three modes of thermal transport, conduction, convection, and radiation, the dominant issue for interconnect systems is conduction. The other modes of transport are important primarily in packaging and trying to maximize heat rejection. Low-*k* materials may be either porous or dense and so the total thermal conductivity λ_t of a porous material is comprised of a number of contributions (see Equation 3.1) such as conduction through the solid matrix λ_s, conduction through the gas in the pores λ_g, and to some extent, radiation through the solid matrix and voids λ_r [177, 178]. Unless temperatures are very high, radiation is not a concern and conduction through the gas in a porous dielectric is a factor only if the processor is designed to operate at cryogenic temperatures. Thus, the remainder of this section will focus on conduction through the solid matrix.

$$\lambda_t = \lambda_s + \lambda_g + \lambda_r \tag{3.1}$$

All the important, low-*k* materials can be considered to be disordered, or amorphous, dielectric solids. Heat transfer in these materials may be treated in terms of the propagation

of anharmonic, elastic waves through a continuum. The energy is propagated in discrete by phonons that arise due to vibrations of molecules making up the solid matrix. We can view the phonons as lattice waves that have a discrete wavelength-dependent velocity. The frequency ω of these lattice waves with velocity v covers a wide range and the thermal conductivity k, in general form, can be written in terms of a superposition of these waves [176].

$$k = \frac{1}{3}\int \rho C_{\mathrm{p}}(\omega)\, v\ell(\omega)\mathrm{d}\omega \tag{3.2}$$

where $C_{\mathrm{p}}(\omega)$ is the specific heat contribution over a frequency interval, $\mathrm{d}\omega$, for lattice waves of frequency between ω and $\omega + \mathrm{d}\omega$, and $\ell(\omega)$ is the attenuation length or the mean free path for those lattice waves. At temperatures above 50 K, phonon motion loses all coherence and since the mean free paths of the phonons carrying most of the energy are short, heat transfer through disordered dielectric films can be considered to be a diffusion process. Borrowing the form from kinetic theory, we can write the thermal diffusivity (α) as:

$$\alpha(T) = k(T)/(\rho C_{\mathrm{p}}) = (1/3)v_{\ell}(T) \tag{3.3}$$

where the macroscopic density ρ, specific heat C_{p} of the material, the transport velocity, v_{ℓ} of the lattice waves (or phonons) and the phonon mean free path ℓ, are the factors that determine the thermal conductivity. The temperature dependence of the thermal conductivity for a crystalline material is shown in Figure 4.38. The four general features of this curve are common for all materials. At very low temperatures, the thermal conductivity is determined by the physical size of the material and it increases roughly as T^3 until it reaches a peak in region II. In region III, the thermal conductivity decreases as $1/T$, largely due to phonon scattering and the Umklapp phonon–phonon process. The actual value of thermal conductivity in region III depends quite sensitively on the presence of defects, fluctuations

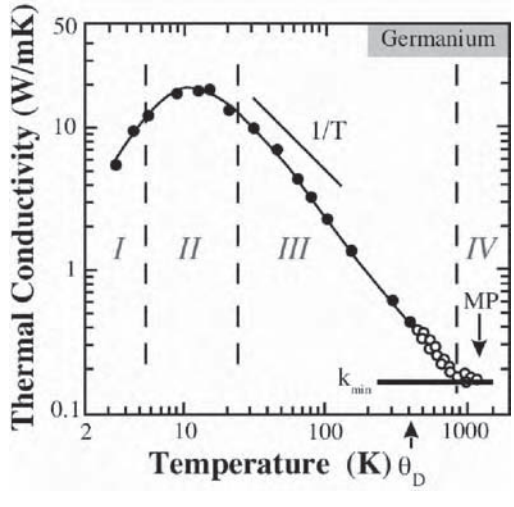


Figure 4.38 Thermal conductivity behavior as a function of temperature

in density, and any process that could lead to phonon scattering. At very high temperatures, in excess of the Debye temperature, the thermal conductivity plateaus.

For dielectric films, the temperature dependence is very weak for ρ, C_p and v, and so it is the mean free path is the main factor that affects the conductivity. In region IV, there is a relatively simple relationship that can be derived to express the *minimum thermal conductivity* [174]. To calculate the minimum thermal conductivity, one assumes the mean free path for phonons λ, is related to a characteristic length defined using the average volume occupied per atom of the dielectric.

$$\lambda = \left[\frac{M_w}{m\rho N_{av}} \left(\frac{3}{4\pi} \right) \right]^{1/3} \tag{3.4}$$

where M_w is the molecular weight of the substance, m is the number of atoms per molecule, ρ is the density, and N_{av} is Avogadro's number.

The phonon velocity v is taken to be proportional to the square root of the elastic modulus E divided by the density.

$$v = C\sqrt{\frac{E}{\rho}} \qquad \text{where} \quad C \sim 0.87 \tag{3.5}$$

Using these approximations, the minimum conductivity can be written as:

$$k_{min} = 0.87 k_B \left[\frac{M_w}{m\rho N_{av}} \right]^{2/3} \sqrt{\frac{E}{\rho}} \tag{3.6}$$

For amorphous disordered solids such as glasses, the mean free path is almost constant at room temperature [179] and is limited to several interatomic spacings. For instance, the mean free path of fused silica at room temperature is 5.6 Å [180], which is about the size of an elementary silicate ring in the disordered structure of glass [181]. For comparison, the characteristic length for calculation of the minimum thermal conductivity is about 1.5 Å. Conductivities in excess of the minimum arise due to the increase in mean free path at lower temperatures, or alternative mechanisms for heat conduction such as electrons or ions carrying heat away in the form of a current.

The thermal conductivity of a material is process dependent since changes in process history influence the number of defects in the material and hence alter the scattering of phonons. Process history effects are especially important for glassy materials and polymers whose defects are frozen in at the glass transition temperature. The process becomes more complicated for materials possessing pores since phonon scattering can be due to defects in the matrix, but also from very small pores and from the abrupt density change that occurs at the pore surface. Generally, an integrated circuit operates at temperatures much less than the Debye temperature of the dielectric. Thus, most of the heat transfer is due to long-wavelength phonons, of wavelength much larger than the minimum calculated in Equation (3.4) whose wavelengths are larger than the pore size. In such a case, effective medium theories should yield good estimates of the thermal conductivity. The effective medium theory of Landauer [182] successfully predicts the thermal conductivity of Vycor glass (porosity ~30%) [183]. Vycor has pores that are roughly 10 nm in diameter and the success of the effective medium approach suggests that the maximum wavelength of phonons is limited to the pore size ~10 nm.

Thermal conductivity measurements

The measurement of thermal conductivity has a long history, but until recently, measurements on very thin films have been difficult and unreliable [175, 177, 184–187]. Two techniques that have found wide usage due to their reliability and versatility are the 3ω technique and photothermal deflection. The details of 3ω technique can be found in the literature [188–194] and a schematic of a 3ω system is shown in Figure 4.39. The photothermal deflection technique is based on the periodic heating of a sample by a modulated laser pump beam. There are various configurations of this method [187, 195–198] and one of those configurations is shown in Figure 4.40. The absorption of the pump laser beam caused a local temperature rise, which in turn lead to a local surface deformation, the magnitude of which could be less than 0.1 nm. The surface deflection signal was detected by the probe beam and was related to the thermal conductivity of the sample. This detection method of thermal waves is called the photothermal deformation technique.

The measurements of both the 3ω and the photothermal method are frequency dependent. It is important that the frequency of measurement is such that the measured thermal conductivity is independent of the film thickness. This is ensured by choosing the thickness of the films and the frequency in such a way that the thermal diffusion length $\sqrt{2\alpha/\omega}$ for the energy pulse is much greater than the film thickness, where α is the thermal diffusivity. This ensures that the dielectric does not store any thermal energy and that a one-dimensional quasi-steady-state thermal heat conduction situation occurs.

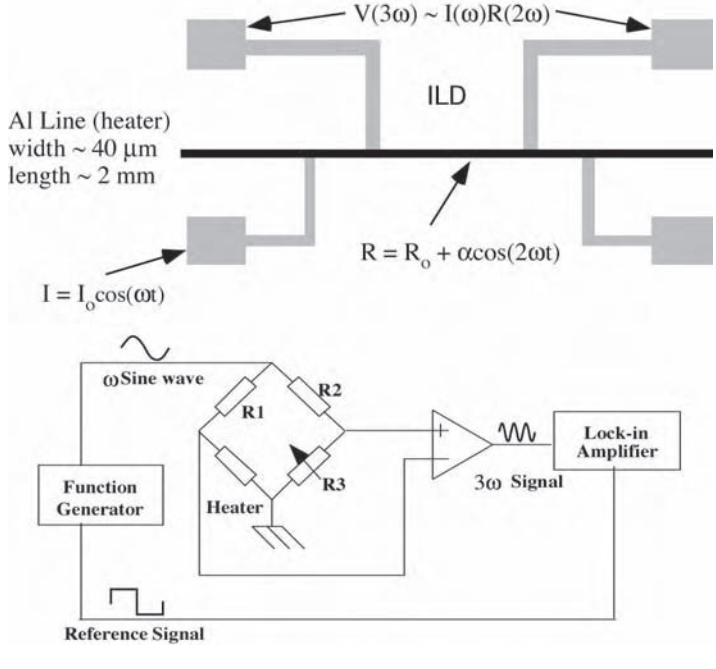


Figure 4.39 Schematic diagram of the 3ω technique. Current is applied at a frequency ω, and the voltage signal is read at a frequency 3ω

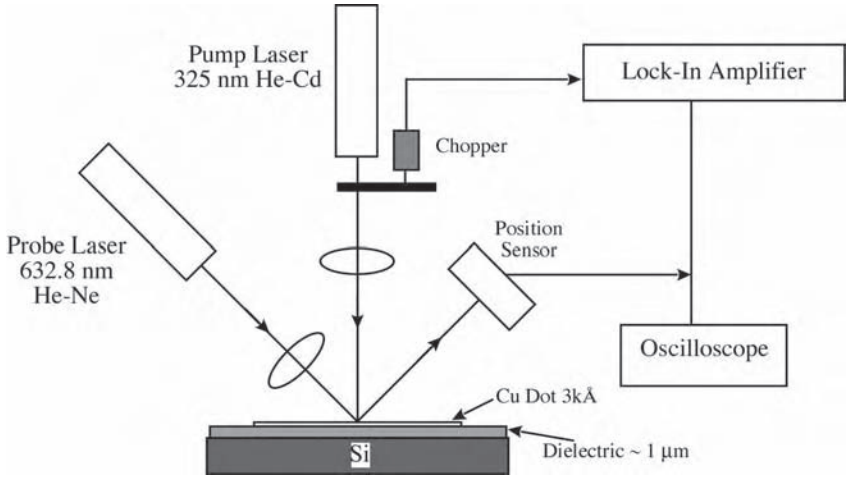


Figure 4.40 Schematic diagram of the photothermal deflection technique. Heat energy is applied to the sample causing it to expand. As the energy dissipates, the thermal diffusivity of the material is determined by recording its relaxation to its room temperature state

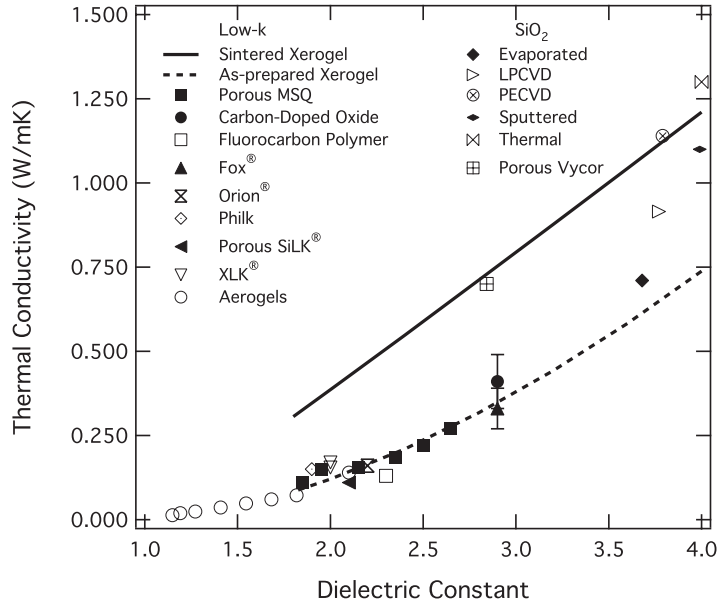


Figure 4.41 A comparison of the thermal conductivity for several low-*k* materials [173, 201–206]

Figure 4.41 displays a comparison of the thermal conductivity for a number of low-*k* materials and for a variety of fabrication methods for producing dense SiO_2. The highest values of thermal conductivity for the low-*k* materials are for the sintered porous xerogel film [206]. The sintering process reduces matrix and pore-induced phonon scattering by healing the microstructure, removing microcracks, reducing microporosity [199], reducing

residual organic content, and causing the pore size distribution and pore shape distribution to become narrower [200]. Thus, the thermal conductivity of sintered porous silica films is essentially a linear function of the film density.

Figure 4.41 also shows that for a given dielectric constant, the inorganic materials exhibit better thermal conductivity than the polymers. Polymeric materials have inherently lower thermal conductivity due to the flexibility of their chains and the corresponding low speed of sound in the material. Crystalline polymeric materials have higher conductivities than amorphous materials. Making either of these classes of materials porous reduces their thermal conductivity accordingly. The hybrid organosilicates (or silsesquioxanes) have conductivities that fall in the general range of as-deposited xerogel and polymeric materials. Additional phonon scattering occurs in the hybrid materials due to the abrupt density changes that occur at organic–inorganic interfaces. In addition, they suffer from the same defects that plague xerogel materials. As the organic of hybrid materials increases, their thermal conductivity approaches that for purely organic, polymeric materials. The decrease in conductivity that arises from increasing organic content is offset by the decrease in defect density in the solid matrix. This keeps the hybrid materials in line with the organics, as shown in the figure.

The measured thermal conductivity for a variety of dense SiO_2 materials is also process dependent, as shown in Figure 4.42. Differences are attributed to changes in bond lengths and removal of impurities such as Si–OH. The degree of disorder and number of defect sites is reduced after high-temperature annealing and the thermal conductivity approaches those of thermally grown silicon dioxide films. Any material with a glass transition temperature would benefit from annealing step to increase its thermal conductivity.

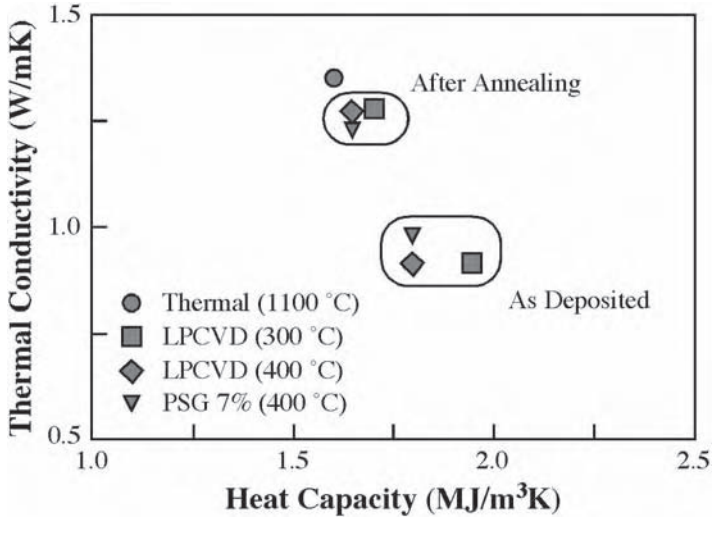


Figure 4.42 Effects of high-temperature annealing of SiO_2 on its heat capacity and thermal conductivity. Temperatures in the graph are deposition temperatures (Reproduced with permission from Annual Reviews) [173]

4.4 INTERACTION OF POROUS MATERIALS WITH METALS AND BARRIER MATERIALS

Cu diffusion into dielectric materials has been documented for SiO_2 [207–210], Si [211] and the low-*k* dielectrics Parylene, poly-aryl-ether, SiLK™, MSQ, and BCB [212]. Cu acts as a deep-level contaminant in Si and adversely affects the performance of devices. A diffusion barrier is employed to insure that Cu penetration is reduced or eliminated altogether. Many types of diffusion barriers have been studied, including Ta, TaN, Ta–Si–N, W, Ru and self-assembled monolayers [213]. Ta and TaN are widely used now due to their high melting temperature, their thermodynamic stability with respect to Cu (no realction or alloying) and their excellent ability to block Cu ions. To maintain the advantage of Cu's low resistivity and the performance of a low-*k* dielectric, diffusion barriers must be as thin as possible.

The tradeoff between diffusion barrier integrity, adhesion to substrate and metal, and thickness places strict requirements on the integrity and stability of these barriers, especially in systems that include porous low-*k* materials, where the ability to form a continuous layer may be compromised by open pores at the surface. Furthermore, as Cu interconnect lines become thinner, the barriers must become virtually molecularly thick. Based on the problems that barriers are facing with low-*k* dielectrics, one needs to go back to first principles and understand the charge injection/diffusion that the barrier is supposed to prevent; and this mechanism needs to be understood in the context of the properties of low-*k* dielectrics.

4.4.1 The effect of the chemistry of the dielectric

The mechanism of Cu charge injection and diffusion in dielectrics and especially low-*k* dielectrics has been an object of intense research in the past few years. Table 4.6 shows a list of activation energies associated with Cu diffusion in a number of dielectrics. Metal drift in oxygen-containing hybrid organic–inorganic material has been linked to the oxidation tendency and the heat of formation of the metal oxide [214]. Rodriguez *et al.* [215] showed that the surface chemistry of a nanoporous silica low-*k* dielectric has a stronger effect on Cu diffusion that does the porosity. In that class of dielectric, as the porosity increases, the internal surface is more accessible to surface modification agents. This leads to a lower amount of moisture in the dielectric and hence less exposure of the metal to potential oxidizing species.

In an integrated device, there are two main driving forces for Cu diffusion into a dielectric; the concentration gradient and the action of an electric field. For the diffusion of metallic Cu to be enhanced by the action of an electric field, the metal must be ionized first. The ionization occurs by oxidation [214, 215]. The Cu oxide, which results from the ionization, acts as the source of the Cu ions that are available for diffusion. This is similar to the diffusion of silver in glass, which was discussed by Kapila and Plawsky [216]. The experimental evidence suggests that hydroxyl species generated from water in the dielectric or oxygen exposed to the metal act as the oxidizing species [210]. Chemically bound or adsorbed water species in glasses can exist in two configurations: in a hydrogen-bonded form (connected to a hydrophilic silanol, SiOH, group) and in a free form. If an electron

Table 4.6 Activation energies for diffusion of Cu in dielectric materials

Dielectric	Activation energy (eV)	Comments
LPCVD SiO_2	0.99	[220] Based on initial Cu drift rate
PECVD Oxide		[207] Reanalyzed data
	1.22 ± 0.03	[208] Small sample
	0.91 ± 0.36	[221] Small sample, approximate technique
	0.63 ± 0.25	[210] Electric field dependent; PECVD and thermal oxide; model suggests 1.1–1.3 eV (thermal only)
	1.8	
PECVD Oxynitride	1.39	[220] Based on initial Cu drift rate
BCB™	1.15	[220] Based on initial Cu drift rate; low-*k* atop a layer of thermal oxide
AF4™	1.41	[220] Based on initial Cu drift rate; low-*k* atop a layer of thermal oxide
SiLK™	0.92	[220] Based on initial Cu drift rate; low-*k* atop a layer of thermal oxide
ALCAP-E™™	1.21	[220] Based on initial Cu drift rate; low-*k* atop a layer of thermal oxide
PAE-2™	1.01	[220] Based on initial Cu drift rate; low-*k* atop a layer of thermal oxide
Nanoporous silica	1.16	[221] Porosity-dependent value

is trapped by a SiOH center, a chemical reaction takes place [217] that produces a negatively charged SiO^- center and a hydrogen ion H^+. This chemical reaction consumes the water-related traps until no further trapping occurs. Hydrogen ions are known to possess substantially higher mobility than Na, Cu or other metals and can move freely throughout the device, causing shifts in characteristics of the MOS capacitor [218, 219]. Rodriguez *et al.* [215] proposed that the combination of moderate temperatures (<300°C) and an external electric field may induce a condensation reaction of the kind that takes place during sintering at high temperatures:

$$2SiOH = Si–O–Si + OH^- + H^+$$

liberating OH^-, that can serve to oxidize the Cu metal.

The source of Cu^+ available for diffusion is a nonstochiometric metal oxide formed at the Cu/SiO_2 interface. The growth of this oxide is accelerated by an applied electric field and by higher temperatures [222].

$$2Cu + \tfrac{1}{2}O_2 \rightarrow Cu_2O$$
$$Cu_2O + \tfrac{1}{2}O_2 \rightarrow 2CuO$$

The oxidation of Cu_2O to CuO is slow compared with the oxidation of Cu to Cu_2O [223]. Depending on the temperature, the oxidation reaction may not produce stoichiometric Cu_2O, but Cu_3O_2 [224]. Additionally, the product of diffusivity and solid solubility of Cu^{2+} in oxide

is insignificant compared with that of Cu^+ in oxide [212], and we can assume that primarily singly ionized Cu ions are injected into the dielectric. Hydroxyl ions that reach the Cu/dielectric surface may react with Cu to form Cu(OH), which is not stable and decomposes to form CuO.

$$Cu + 2OH^- \rightarrow Cu(OH)_2 + e^-$$
$$Cu(OH)_2 \rightarrow CuO + H_2O$$

The metal or the oxidizing species must diffuse through the metal oxide layer for the reaction to continue. Since Cu forms *p*-type oxides (e.g., Cu_2O) the diffusion of metal ions through this metal oxide layer toward dielectric occurs in preference to diffusion of larger OH^- toward metal [225]. Cu corrosion is not self-limited and will continue until all Cu is used. The injection of metal ions leads to a charge build-up in the dielectric and an increase in dielectric leakage [212]. When the density of Cu ions in the dielectric reaches a critical value, a conduction path that links the cathode and anode may form triggering a dielectric breakdown.

Wang *et al.* [226] found a smooth amorphous-like layer including Cu–O–Si between Cu and a porous hydrogen silsesquioxane film after annealing at 500°C for 30 min.

The Si–O–Si angle and rotation around the Si–O–Si link are variable, but the Si–O bond lengths are the same as in quartz or other crystalline modifications. The density of SiO_2 grown in Si is ~2.1 g/cm^3, which is smaller than the density of quartz. Thus the structure of SiO_2 is open, with large interstices in which the Cu^+ can fit. A Cu^+ ion diffusing through the bulk may stay trapped by an SiO^- group, it may continue diffusing towards the Si where it may react to form a silicide, or it may diffuse into be Si [211]. Among the identified or postulated intrinsic defects in SiO_2 there are only two negatively charged defects: SiO^- (in our case, from the silanol groups) and a strained Si–O–Si bond [227].

Rodriguez *et al.* [215] used capacitance–voltage measurements in metal–insulator–semiconductor capacitors to estimate the concentration of Cu^+ that diffuses in a porous dielectric as a function of the temperature, the external electric field and the chemistry of the dielectric.

Figure 4.43 shows the Cu^+ charges detected as a function of time in nanoporous silica xerogel of different porosities. In all cases, the injection of Cu follows a saturation scheme. The concentration of Cu^+ is the highest in the 18% porous film, decreases for the case of 30% porosity and decreases furthermore for higher porosities; this trend is observed for all conditions of external electric field and temperature. Although this result may appear counterintuitive, as one would expect the higher amount of open space in the higher porous material to translate in an increase in the amount of Cu^+ diffusion, the experimental results suggest that Cu^+ injection depends not only on the physical properties of the dielectric (pore morphology, pore size, porosity), but also on the chemical properties (organic and hydroxyl content).

Figure 4.44 shows the effect of the stressing temperature in Cu^+ diffusion and Figure 4.45 shows the effect of the external electric field. For a film of a particular porosity, Cu^+ diffusion increases with both temperature and electric field, but the increase is exponential with temperature and linear with respect to the electric field. Note that the large amount of Cu^+ diffusion at 200°C induces rapid breakdown of dielectric and failure of the capacitor under test.

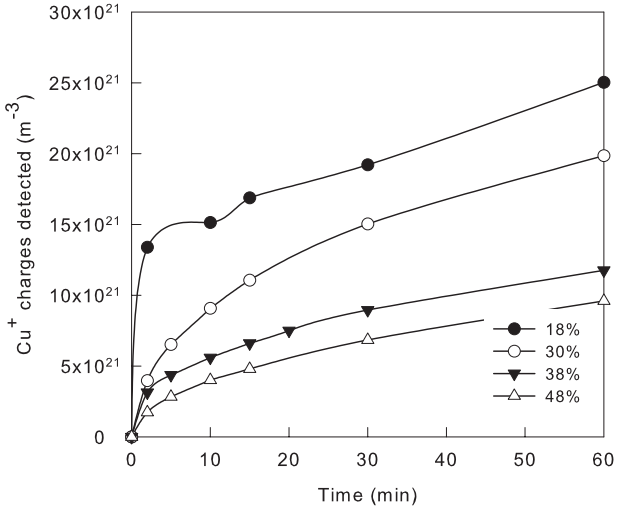


Figure 4.43 Cu^+ concentration in nanoporous silica as a function of porosity

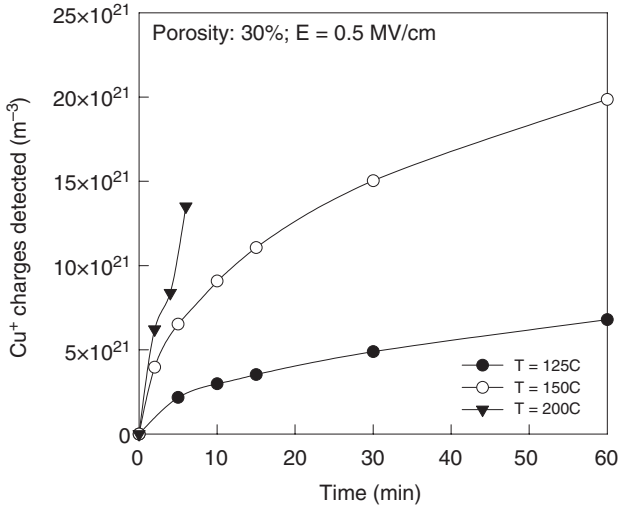


Figure 4.44 Cu^+ concentration in nanoporous silica as a function of temperature

The tortuosity of the porous structure may reduce the apparent diffusivity of Cu^+ in the dielectric, but at the same time an increasing surface path for diffusion with porosity may enhance the diffusion of Cu^+ [228]. The organic and hydroxyl content are related through the surface modification step during fabrication. The results in Figure 4.43 suggest that in nanoporous silica the surface is more accessible to the surface modifier in higher porosity films and this enables the introduction of organic groups on the surface to be greater.

Rodriguez *et al.* [215] showed that the trend of increasing Cu resistance with increasing porosity holds, even when taking into account the changes in interfacial area between the

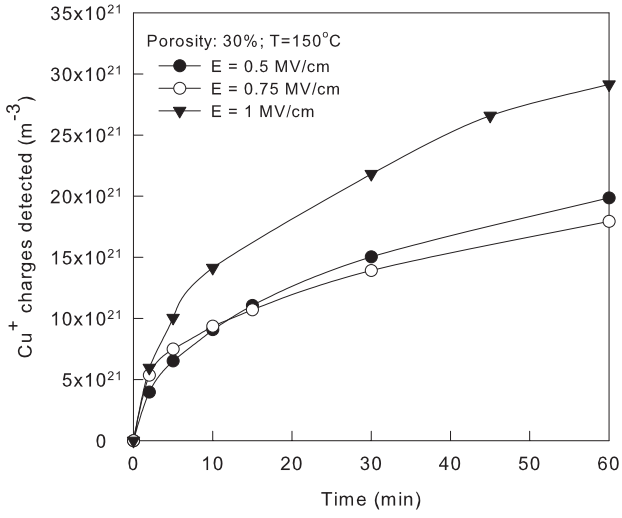


Figure 4.45 Cu^+ concentration in xerogel, as a function of the electric field

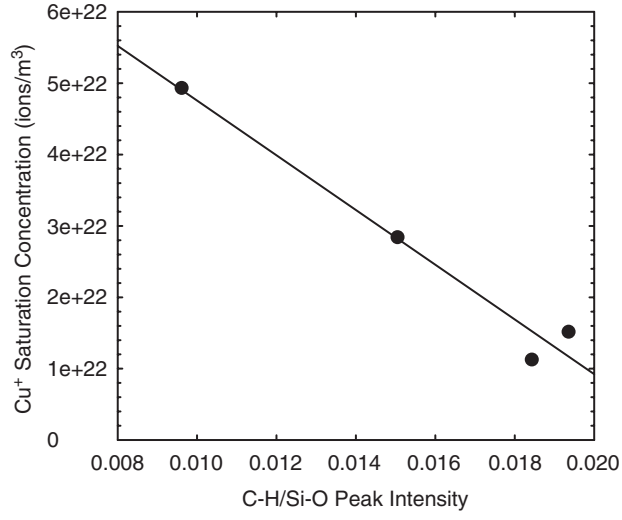


Figure 4.46 Cu^+ concentration after 60 min at 0.5 MV/cm and 150°C as a function of the organic content of the film (Reproduced with permission from the American Institute of Physics) [215]

metal and the dielectric as the porosity increases. The maximum Cu^+ concentration obtained in the experiment decreases as the organic content increases, as shown in Figures 4.46 and 4.47. The organic content in the film was characterized by Fourier transform infrared spectroscopy and by the contact angle. Figures 4.46 and 4.47 suggest that the surface chemistry of the dielectric has a stronger effect than porosity on Cu diffusion: as porosity increases the amount of organic content in the dielectric increases, which implies a lower amount of moisture and less oxygen exposed to the metal, which in turn translates into the increased

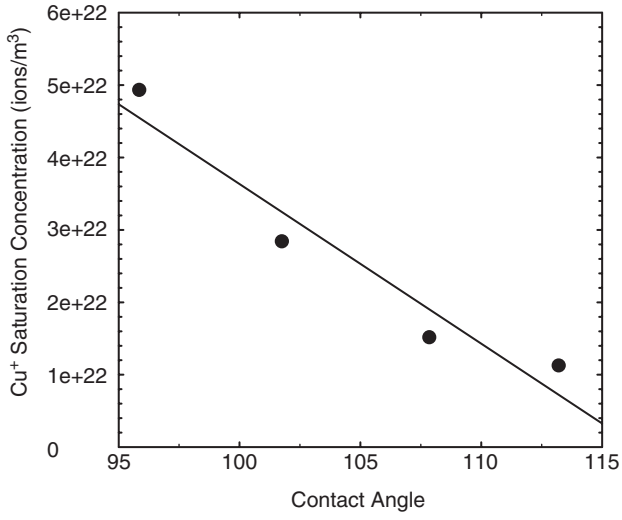


Figure 4.47 Cu^+ concentration after 60 min at 0.5 MV/cm and 150°C as a function of the contact angle of the film (Reproduced with permission from the American Institute of Physics) [215]

film resistance to Cu diffusion shown in Figure 4.43. The re-inclusion of organic content via surface modification after the film is damaged by sintering proves to be a method that increases the film resistance to Cu^+ diffusion.

The surface modification step during the fabrication of hybrid porous dielectric such as xerogel or mesoporous silica removes the –OH content in the film and renders the material hydrophobic. However, not all the silanol groups are replaced and the extent of surface modification is constrained by steric hindrance effects and the reactivity of silanols that form hydrogen bonds. Steric hindrance effects may appear at the entrance of the pore necks or two trimethylsilyl groups blocking a third. Saxena *et al.* [229] studied the pore shape and size of xerogel using ellipsometric porosimetry. The average pore size of xerogel increases with increasing porosity. Most of the mesopores are of two types, tubular capillaries closed at one end and narrow-necked ink-bottle pores. As porosity increases and pore size increases, the pore shape becomes further skewed and more tubular, widening the gap between the pore opening size and the pore body. The size of the pore body r_{body}, and the pore neck r_{neck}, of mesoporous silica varies with porosity Π, according to $r_{body} = 0.46e^{0.04\Pi}$ and $r_{neck} = 0.65e^{0.03\Pi}$, and so the probability that the molecules of the surface modifier reach the porous silica surface increases with porosity. The reactivity of the silylating agent with the porous material depends on the type of hydrogen bonding [230]. Hydrogen-bonded hydroxyls that participate in the silylation reaction do so at a rate that is one order of magnitude slower than isolated silanols. The percentage and distribution of hydrogen-bonded hydroxyl groups on gel surfaces depend on surface curvature effects. A small positive radius of curvature increases the O–H—O distance of neighboring hydroxyl sites, reducing the extent of hydrogen bonding on a particle compared to a flat surface with the same surface coverage of OH groups. A small negative radius of curvature, as in cylindrical pores or necks between particles reduces the O–H—O separation between neighboring hydroxyl groups, increasing the extent of hydrogen bonding over that of a flat surface [231]. Although

it is accepted in the literature that molecular water does not appear in thermal SiO_2, there are silanol groups (SiOH) present in SiO_2 and other inorganic dielectrics as a result of the fabrication process. The silanol groups may be isolated or forming hydrogen bonds. In silica, the hydroxyl coverage at equilibrium is about 4.6 OH/nm^2, of that amount, 1.4 OH/nm^2 (~30%), are isolated and 3.2 OH/nm^2 are hydrogen bonded [231].

Rodriguez *et al.* [232] showed that at short times (<60 min) the average concentration of Cu^+ in the dielectric is a linear function of the square root of time. The diffusion of Cu^+ create space charges in the dielectric that balance the effect of external applied electric field, and the transport occurs mainly by molecular diffusion. As time increases and the Cu ions move farther away from the Cu/dielectric interface the effect of the electric field becomes more predominant.

Using a mathematical model to reproduce the experimental data, Rodriguez *et al.* [232] showed that the diffusivity of Cu^+ ions in xerogel follows an Arrhenius-type dependence with temperature, with an energy of activation of 1.16 eV and a pre-exponential coefficient that is a function of the porosity Π,

$$D = 1.4 \times 10^{-3} \exp(-0.061\Pi) \exp\left(-\frac{1.16\,\text{eV}}{k_B T}\right) \frac{m^2}{s} \tag{4.1}$$

The level of the activation energy suggests that the effect of surface diffusion is not predominant in the conditions of temperature and electric field used in the experiments (<200°C, <10^6 V/cm); and the diffusion of Cu^+ is tied to the presence of defects such as vacancies and interstitials. Impurity atoms can diffuse by jumping directly from one interstitial site to a neighboring one or from defect sites to another defect site.

Copper diffusion in parylene-n (Pa-n) and other low polymers has been the subject of much investigation [233–236]. Initial studies [233] dealt with the diffusion of copper under thermal annealing in the absence of an electric field. Copper was detected by RBS in Pa-n when it was thermally annealed at temperatures >350°C [233]. The extent of copper diffusion under thermal annealing depended on the initial crystalline state of Pa-n [233]; β-phase Pa-n was more resistant to thermal diffusion than α-phase (the initial phase when deposited).

Mallikarjunan *et al.* studied copper diffusion in a variety of low-*k* polymers both organic and inorganic [234, 237, 238]. The organic polymers studied were Pa-n and polyarylether (PAE) while HOSP™ was the hybrid dielectric. Silicon dioxide and Pa-n were chosen to be the baseline dielectrics in their work. Pa-n showed copper diffusion under an electric field of 1 MV/cm. Pre-annealing in N_2 at 300°C prior to metal deposition resulted in a slight reduction in copper diffusion, as evidenced by the magnitude of the shift in the flat-band voltage. The reduction in Cu diffusion can be explained in terms of the microstructural changes that Pa-n experienced. On pre-annealing Pa-n in N_2 at 300°C, the residual monomer present in the as-deposited film is expelled and the crystalline content of the polymer increases from 57 to 80%. In addition, Pa-n undergoes a phase transformation from a monoclinic β phase to a hexagonal β phase at 230°C, making it harder for Cu to diffuse.

In another study by the same group [234], Pa-n was pre-annealed in Ar (3% H_2) at 250°C for 1 h. BTS testing of this Ar-annealed (3% H_2) sample showed no copper penetration under testing conditions of 0.5 MV/cm and 150°C. Annealing in a hydrogen atmosphere was argued to remove surface oxygen species and hence limit the oxidation and penetration of copper. Pa-n is deposited using a free radical mechanism. Termination of residual free

radicals occurs when the polymer is exposed to the atomosphere and reacts either with moisture or atmospheric oxygen.

Mallikarjunan *et al.* also studied copper drift in FLARE™ and HOSP™ [239]. Copper diffusion was faster and more extensive in HOSP™ than in thermal oxide. Al is also found to diffuse in HOSP™, even though it does not diffuse in thermal SiO_2.

Bartha *et al.* [240] employed similar oxide-capped dielectrics with SiLK™ and found that Cu drift rates followed the trend SiLK™ > BCB™ > PECVD oxynitride at 200°C and 0.8 MV/cm. Different formulations of SiLK™ viz. SiLK™ I, J, H showed different drift rates, but no explanation is offered for this variance due to the proprietary formulation of the polymer.

Several key questions remain unanswered from previous work on polymers most importantly the mechanism of copper penetration into the dielectrics. Evidence was presented showing that surface oxygen species were involved in Pa-n and that surface oxygen was able to oxidize the Cu and drive it into the polymer. This suggests that the mechanisms for copper penetration into oxide-based glasses and copper penetration into polymer are similar and that both involve an oxidant from the dielectric. To test this conjecture, several experiments were run using SiLK™. In these experiments SiLK™ was tested as-deposited and after exposure to an oxygen plasma. Exposure to the plasma greatly increased the concentration of surface oxygen species. The polymers were tested using BTS and the results of those tests are shown in Figure 4.48.

Copper penetration into the SiLK™ specimens was compared with penetration into a nanoporous silica xerogel and also into porous MSQ. As expected, the xerogel admitted the highest level of Cu while MSQ admitted the lowest. Interestingly, Pa-n allowed more penetration of Cu than SiLK™, even though is ostensibly contains no oxygen in its molecular structure. The oxygen in SiLK™ is strongly covalently bonded and so does not participate

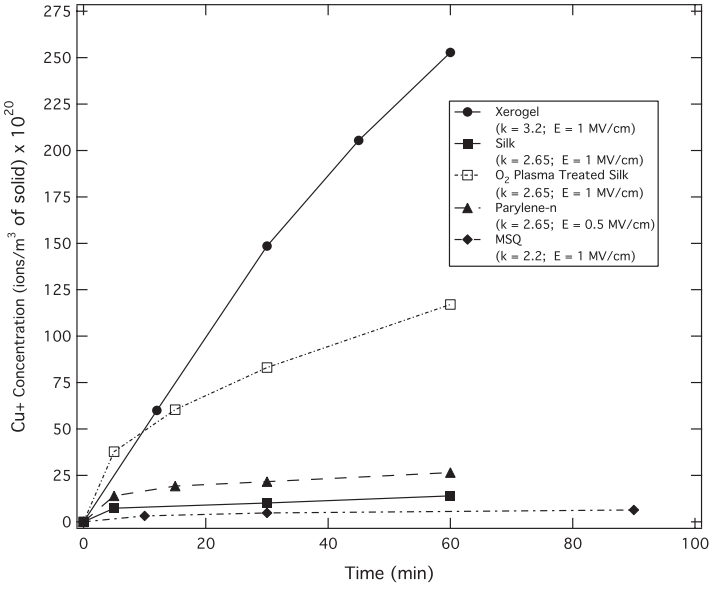


Figure 4.48 Copper diffusion into several low-*k* dielectrics

in Cu oxidation. However, upon exposing the SiLK™ to the oxygen plasma, sufficient weakly bound oxygen species are present at the surface to facilitate Cu ionization and large-scale Cu penetration. This clearly indicates that the oxidizer comes from the dielectric and that the mechanism of copper penetration into dielectrics is similar, regardless of the chemistry of the dielectric. Removal or scavenging of oxidizing species is critical to providing a barrier to copper penetration.

4.4.2 The effect of dielectric morphology

Rodriguez *et al.* [241] used SIMS measurements to obtain Cu concentration profiles in xerogel after bias thermal stressing at 150°C and 1 MV/cm. Figure 4.49 shows the Cu profiles as a function of porosity. The penetration depth decreases with an increase in porosity and the concentration of Cu^+ is the highest in the 18% porous film, decreases for the case of 30% porosity and decreases furthermore for higher porosities.

In general, two types of profiles of Cu diffusion are observed in the literature. In one case, such as the experiments reported by Nishino *et al.* [242] and Willis and Lang [210], a large concentration of Cu is observed near the Cu/dielectric interface, but very little remains in the dielectric, which may imply that the Si acts as a sink for Cu atoms. In another case, such as the experimental data reported by Shacham-Diamand *et al.* [208] and by Rodriguez *et al.* [241], the profiles are broader and more evenly distributed across the dielectric.

The shape of the Cu^+ concentration profiles depends on the morphology of the dielectric, the external electric field and the interaction between Cu and the dielectric at the interface. The total concentration of Cu^+ decreases with the porosity of the dielectric. This

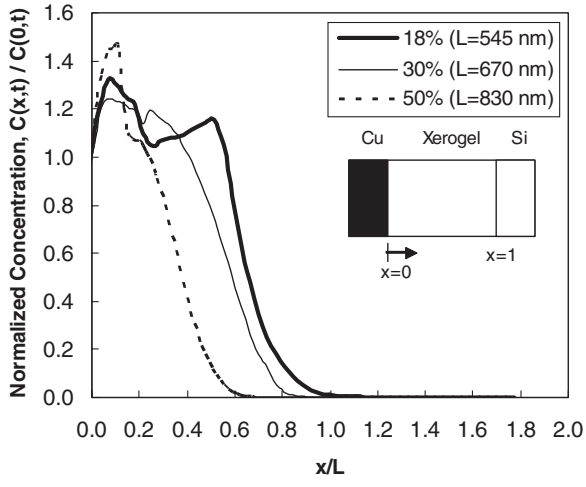


Figure 4.49 Secondary ion mass spectroscopy (SIMS) data plotted for Cu/mesoporous silica/Si capacitors. The porous silica films are of three different porosities and the diffusion of Cu occurs after bias temperature stressing conditions of 106 V/cm, 150°C for 30 min (Reproduced with permission from the American Institute of Physics) [232]

behavior is the combined result of both the chemistry and the morphology of the dielectric. The injection of Cu is triggered by outgassing of hydroxyl and water-related species from the dielectric; furthermore, the reduced available cross-sectional area for diffusion, due to porosity, leads to reduced diffusion through the porous film, as shown in Figure 4.50. Similarly, the tortuosity of the porous structure makes the effective path for the diffusion across the film longer than the actual film thickness and reduces the apparent diffusivity.

The presence of positive (or negative) charges in the dielectric creates local space-charged regions that distort the external electric field. As a consequence, the effective electric field near the metal–dielectric interface is lower than the external electric field that results in a decrease in the rate of injection of Cu ions.

The concentration of Cu^+ at the Cu–dielectric interface follows an exponential relationship with the porosity of the dielectric, which may be the result of an oxidation reaction with different levels of the oxidizing species, in this case, oxygen exposed to the metal or –OH content in the dielectric.

Rodriguez *et al.* [241] showed that the apparent penetration depth of Cu^+ in the dielectric does not change significantly for times greater than 5 min, at 10^6 V/cm and 150°C. However, the level of Cu^+ concentration near the Cu/dielectric interface increases as time increases. Those results suggest that a chemical reaction occurs at the interface, which is induced by the external electric field and the temperature, and the product is the source of Cu^+ ions available for diffusion. The rate of generation of Cu^+ is larger than the rate of transport of these ions in the dielectric (a combination of molecular diffusion and drift), which results in an accumulation near the Cu/dielectric interface, as the experimental results in show. As the reaction continues, the depletion of reactants leads to a decrease in the concentration of Cu^+ at the interface.

4.5 CONCLUSIONS

Despite a decade or more of research and development, much more work needs to be done before low-*k* materials will be integrated into commercial integrated circuits. Any new low-*k* material will have to pass a series of stringent tests before it is deemed a suitable replacement for SiO_2. The properties of low-*k* materials depend upon their chemistry, their microstructure and often upon their processing history. Thus, each material may behave quite differently and as their structure and composition change, meeting industry standards in one formulation does not guarantee meeting them as different versions of the material become necessary to meet increasingly rigorous roadmap requirements. In this chapter we showed that:

- Bulk mechanical properties such as the elastic modules, while important, are not the only mechanical measure of importance in choosing or designing a low-*k* material. It is also important to assess the interfacial interactions between the different materials, and especially how surface properties such as interfacial energy, surface roughness, interfacial reactions, and intrinsic stress affect the stability of a deposited thin film.
- The thermal conductivity of a low-*k* material is highly dependent upon the material properties and also the microstructure, especially defects in the backbone or matrix

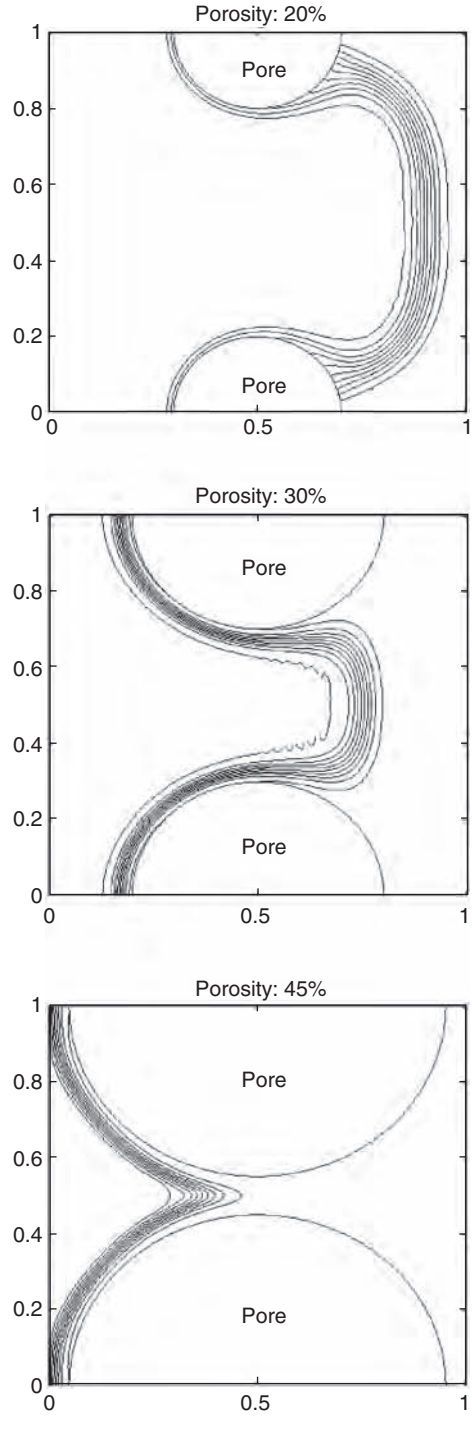


Figure 4.50 Contour plots of Cu^+ concentration in a model porous solid. The simulations used the following parameters for the diffusivity in the matrix material D, the surface concentration of dopant C_0, and the number of oxidizing species at the Cu–dielectric interface n: $D = 10^{-19}\,m^2/s$; $C_0 = 10^{23}\,atom/m^3$, $n(x,0) = 0$ (Reproduced with permission from the American Institute of Physics) [232]

material. Most materials were shown to follow a single curve, representing the thermal conductivity as a function of dielectric constant. In such materials, increasing porosity for a hybrid dielectric material such as MSQ as a means of lowering the dielectric constant resulted in a decrease in thermal conductivity equivalent to increasing the materials organic content.

- Oxygen-containing species are the prime culprits in enhancing the diffusion of Cu into low-*k* dielectrics. These species whether they are in inorganic or organic materials, in the bulk, or at the surface, tend to travel toward the Cu–dielectric interface, oxidize the Cu and allow the Cu ions to then penetrate into the dielectric under the application of an electric field.
- Of all current low-*k* materials tested, none meet all the requirements required for a dielectric, and none can compare to the standard set by dense SiO_2. It remains to be seen which material property will govern whether a given low-*k* dielectric is commercially viable in future generations of microprocessors.

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5 Integration of Low-*k* Dielectric Films in Damascene Processes

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5.1 INTRODUCTION

Due to the continuous scaling of advanced integrated circuits to deep sub-micrometer levels, signal delay caused by the interconnect (*RC* delay) has become increasingly significant compared with the delay caused by the gate [1–3]. In addition, the cross-talk noise and power dissipation became much more important in circuit performance [3, 4]. In order to compensate for the decreased circuit performance, the microelectronics industry has

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replaced the aluminum conductor by copper (i.e., lowering resistance) and silicon dioxide (SiO_2) by a low-k dielectric, i.e., a material with a lower dielectric constant (i.e., lowering capacitance) [5].

Silicon dioxide (SiO_2), the dielectric of choice from 2–0.25 micrometer technology, has a dielectric constant k of 4. In order to obtain a material with a lower dielectric constant, the molecular polarizability needs to be lowered [6–7]. The latter can be achieved either by inserting atomic groups with a small polarizability and/or by lowering the electronic density. The effect of density on the film permittivity is stronger than the effect of the polarizability since the density can be lowered to zero (air gaps) achieving a k value of unity.

In the first generation of low-k materials, some of the Si–O bonds were replaced with the less polarizable Si–F bond, producing fluorinated silicate glasses (FSG). For most companies, FSG has been the material of choice for both the 180 and the 130 nm technology nodes [8–11]. In the second generation of low-k dielectrics, lower dielectric constants were achieved for silsesquioxane-based materials and CVD organosilicate glasses (OSGs). The lower permittivity is partly due to the lower density of these materials compared with SiO_2. The density is lowered by breaking the three-dimensional Si–O–Si network by incorporating Si–H or Si–R groups (where R is an organic moiety such as CH_3). CVD OSGs are the materials of choice for the 90 nm node [12, 13]. The most common CVD OSG materials on the market are Black Diamond™ ($k = 2.9$: Applied Materials), Coral™ ($k = 2.85$: Novellus), and Aurora™ ($k = 2.9$: ASM). However, in the same generation another interesting class of materials with low k values exists; the organic (carbon-based) polymers. Unfortunately, chemical bonds with low polarizability, in the latter case C–C bonds, tend to be weaker, limiting thermal stability and stiffness, limiting the thermomechanical properties [14]. Therefore, aromaticity is included in order to obtain a certain extent of processability. The best-known example of the latter low-k class is Dow Chemicals' SiLK™ ($k = 2.65$) [15]. A representative summary of the different classes of low-k materials can be found in Table 5.1.

In order to achieve k values below 2.5 (ITRS requirement for the 45 nm node and beyond [16]), additional porosity has to be introduced into the 'dense' low-k materials. Additional porosity can be introduced in the material, either through a sol–gel process or by inclusion of sacrificial nanoparticles (i.e., porogens), which are decomposed and desorbed during a high-temperature bake step.

Table 5.1 A representative list of candidate low-k materials, their dielectric constant and the method of deposition

Low-k type	k value	Deposition method
Fluorinated silicate glass (FSG or SiOF)	3.2–3.6	CVD
Hydrogen silsesquioxane (HSQ)	2.8–3.0	Spin-on
Methyl silsesquioxane (MSQ)	~2.7	Spin-on
Organo silicate glass (OSG or SiOC(H))	2.8–3.0	CVD
Organic hydrocarbon polymers	2.6–2.9	Spin-on
Porosity-containing materials	<2.6	Spin-on / CVD

Introducing pores in a dielectric poses several challenges for successful integration into microelectronic circuits [17, 18]. The mechanical strength of the dielectric is reduced by porosity, potentially leading to failure during chemical mechanical planarization (CMP) [19, 20, 21, 22] or during wire bonding to the finished chip [23]. In addition, moisture, wet chemicals and gaseous species (such as precursors used during CVD) can penetrate into porous low-*k* materials, giving rise to an increase in both the dielectric constant and the leakage current [24]. Thus it is expected that porous low-*k* materials need to be hermetically sealed. One of the most extensively investigated methods is plasma sealing [25–27], which creates a densified surface layer. However, if we look to this approach from a different perspective, the sealing layer can also be classified as plasma damage. This kind of process-induced low-*k* damage leads to deterioration of the material properties, reflected by increasing *k* values and leakage current and decreasing dielectric breakdown strength. A strict control of the extent of such damage upon integration is essential for downscaling of the interconnect system.

In this chapter, the challenges related to the damascene integration of low-*k* materials in interconnects will be discussed. Several damascene integration approaches will be presented, followed a detailed discussion of the different integration challenges (such as resist poisoning, plasma damage, compatibility issues with wet cleans, barriers, CMP and pore sealing). Finally, a short insight in the reliability challenges related to the introduction of porous low-*k* materials will be given, together with some future expectations.

5.2 DAMASCENE INTEGRATION APPROACHES

5.2.1 From aluminum to copper in integrated circuits

As was discussed in the introduction, copper (Cu) metallization has replaced aluminum (Al) in the present CMOS technology nodes. Copper interconnect technology provides significant improvements in chip performance and BEOL manufacturing. Higher performance results from lower effective resistivities and higher electromigration lifetimes [28–30], compared with aluminum interconnects (Table 5.2). These allow design tradeoffs between lower-resistance wires or smaller wire cross-sections. Simpler, lower cost BEOL manufacturing is likely and there is evidence for greater process control, leading to lower systematic yield loss [28, 31].

Table 5.2 Resistivity and electromigration performances of several metallic compounds

	Resistivity (μΩ cm)	Electromigration performance
Al	2.66	Weak
AlCu (0.5%)	3.10	Medium
W	5.65	Very high
Ag	1.59	Weak
Au	2.35	Very high
Cu	1.67	High

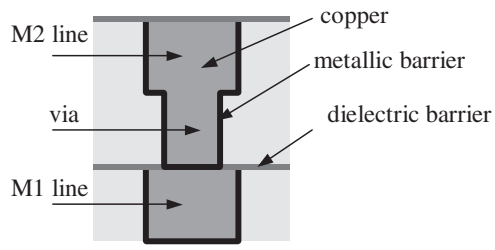

Figure 5.1 Copper encapsulation by metallic and dielectric barriers. (Reprinted from New Directions in Antimatter Chemistry and Physics, 2001, 154, C.M. Surko and F.A. Gianturco (eds.), figure 1, with kind permission from Springer Science and Business Media)

The introduction of copper has however implied multiple challenges and technological developments in order to cope with the high-volume manufacturing requirements. The first challenge exists in the fast diffusion of copper in silicon and silicon dioxide. For interconnect structures this can lead to an enhanced interline leakage due the diffusion of copper ions in the intermetal dielectric. Inside the silicon substrate, copper can easily act as a mid-gap trap, reducing the lifetimes of charge carriers and thus alter transistor properties [32]. For these reasons, copper has to be entirely encapsulated by diffusion barriers, as illustrated in Figure 5.1. The sidewall and bottom surface of the lines are covered with a metallic barrier deposited prior to copper deposition (see Section 5.3.3). Most widespread metallic barriers are binary refractory compounds such as TaN or TiN. The top surface of the lines is entirely capped by a dielectric barrier (such as Si_3N_4, SiC, SiCN), deposited on the whole surface of the wafer (see the discussion of dielectric copper barriers in Section 5.2.2).

In contrast to aluminum, it is very difficult to plasma etch copper. Elevated temperatures (>200°C) are required to create volatile products (Cu_3Cl_3). High etch rates can be obtained in pure chlorine, however no anisotropic etch profiles can be achieved [33]. For that reason, copper etching has not been considered seriously. Consequently, it is not possible to keep the same integration flow as previously used for aluminum (Figure 5.2a). The interconnect architecture had to be obtained by damascene patterning [31], in order to make copper integration possible. The difference between the copper damascene and the aluminum gap-fill approach is depicted schematically in Figure 5.2. In damascene integration, two approaches can be distinguished, namely single and dual damascene patterning. In the single damascene approach, only one pattern, either trenches or vias, are etched in a dielectric, while in dual damascene both trenches and vias are patterned in a dielectric.

After the damascene patterning, regardless of the architecture, the metallization process is identical, and as depicted in Figure 5.3. The metallic barrier is deposited onto the line and via topography, after which copper deposition is performed in several steps. The first step consists in the deposition of a seed layer by a physical vapor deposition. This highly conductive seed layer enables the remaining gaps to be filled with copper by electrochemical plating (ECP). The challenge of this step is to obtain void-free copper structures, which could be problematic for narrow lines and small via structures. To reduce the probability of void formation in narrow plated copper structures, the barrier and the seed layer have to be thin and as conformal as possible. After copper fill, the excess of metal on top of wafer is removed by chemical mechanical polishing (CMP), after which the copper structures are capped by the dielectric diffusion barrier. The flat surface so obtained is ready for next damascene level.

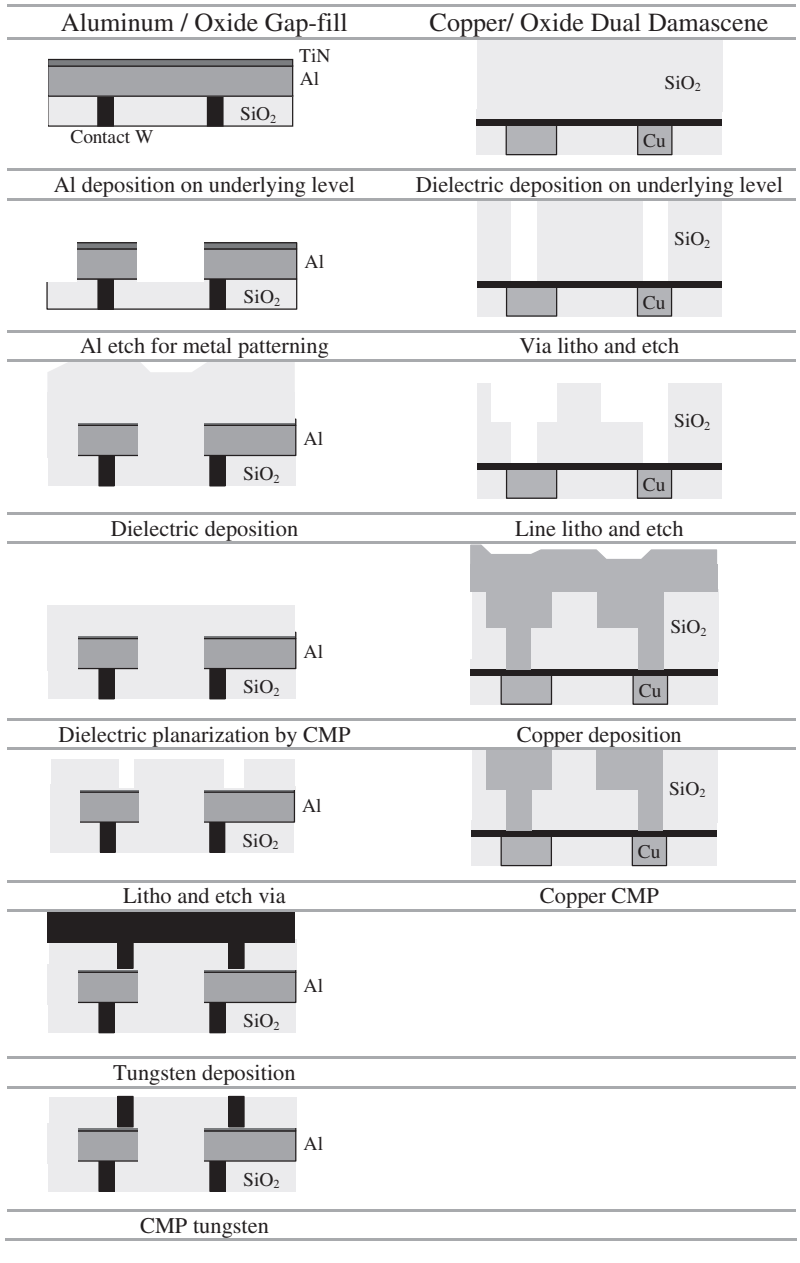

Figure 5.2 Schematic representation of the conventional aluminum/oxide gap-fill approach versus dual damascene copper/oxide integration

As was depicted in Figure 5.2, the transition from aluminum/tungsten interconnects to a copper interconnect leads to a reduction of the number of process steps required to build the interconnect. This is due to the fact that a single metal deposition step is able to fill both line and via at the same time. This architecture is a so-called dual damascene. The

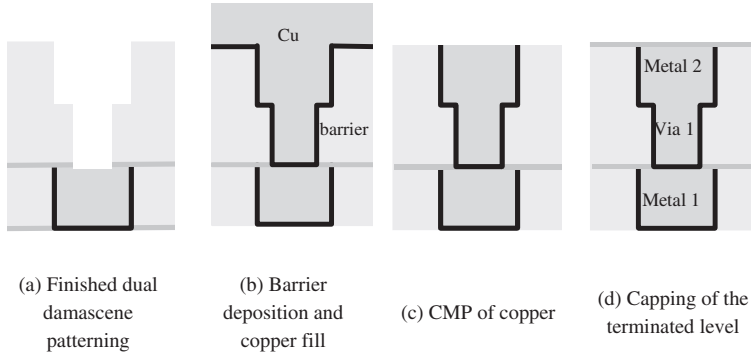

Figure 5.3 Schematic representation of the different process steps in the metallization module. (Reprinted from New Directions in Antimatter Chemistry and Physics, 2001, 154, C.M. Surko and F.A. Gianturco (eds.), figure 1, with kind permission from Springer Science and Business Media)

reduction of the number of steps in this architecture reduced directly the cost of ownership, which makes it preferable over the single damascene approach in which via level and line level are constructed separately. However, subsequent single damascene fabrications remains possible and are technically even simpler; that is why it is still an option in specific cases where the dual damascene appears challenging.

In the next section a more detailed description of the dual damascene architecture and its options will be offered. The dual damascene architecture was historically developed with silicon dioxide (SiO_2) as intermetal dielectric. More recently, introduction of low-*k* dielectrics have accentuated damascene integration challenges and necessitated new additional materials and processing schemes, which will also be addressed in the following paragraphs.

5.2.2 Dual damascene architectures

Standard dual damascene patterning schemes

This section deals with the different schemes to pattern dual damascene structures. The three most common schemes reported are the self-aligned (SA) [34, 35, 36, 37, 38], via first (VF) [34, 37, 38, 39, 40, 41, 42] and trench first (TF) [34, 37, 38, 43] schemes. These different approaches can be distinguished by variation in the chronology of lithography for line and via.

The SA architecture is explained in Figure 5.4. It consists in etching the whole dielectric stack (via and trench dielectric) selectively to the intermediate etch stop layer (ESL) that serves as a hard mask for the via. It should be noted that the ESL has been opened in a previous patterning step. The main advantage of this technique is that lithography is always performed on flat surfaces both at line and via levels. However, the key issues related to this SA scheme are the etching selectivity between dielectric and the intermediate etch stop layer and the sensitivity to lithography misalignment. Indeed as via and line are designed at the same critical dimension, any misalignment between line and via lithography brings a marginality during etch that decreases the via diameter. This misalignment issue was shown to be responsible for drastic yield loss due to etch stop in the vias [37] and that is why SA architecture is not widespread in manufacturing.

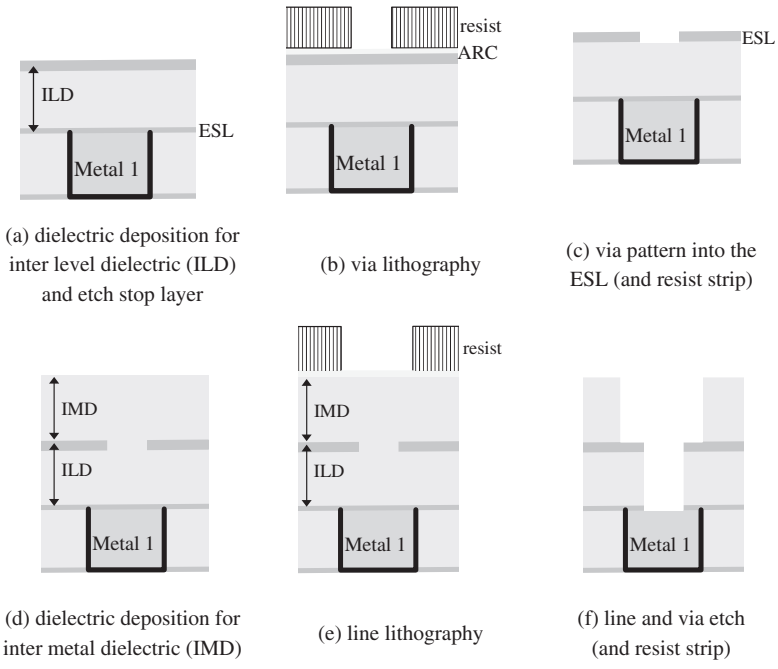

Figure 5.4 Schematic representation of the self-aligned dual damascene approach. (Left-hand panel reprinted from New Directions in Antimatter Chemistry and Physics, 2001, 154, C.M. Surko and F.A. Gianturco (eds.), figure 1, with kind permission from Springer Science and Business Media)

Another dual damascene approach is the VF architecture, which is depicted schematically in Figure 5.5; the vias are etched through the entire dielectric stack (trench-and via-dielectric) and the trench etch is done at the end. This scheme usually implies that the bottom of the via is protected during line etch, to avoid any copper resputtering. This can be achieved by a high etching selectivity between dielectric and the dielectric barrier on top of the underlying metal or by a coating (with recess) of a polymer plug. This plug can be removed by ashing at the end of etch process. An antireflective coating (ARC), which is typically used for planarizing and reducing substrate reflections during the lithography process, can be used for this purpose, as illustrated in Figure 5.5.

The via etch is one of the most challenging steps in the VF architecture, not only due to the high aspect ratio, but also to ensure good electrical contact for both isolated and dense vias afterwards. A good selectivity is needed with respect to the resist as well as to the underlying etch stop layer. However, the VF architecture offers very good robustness to lithography misalignment. Moreover, even if the line lithography has to be performed with via topography, the density and the total surface of via is quite low. If necessary, this topography can be planarized by a polymer coating [44]. Compared with the SA architecture, no intermediate etch stop layer is needed in the VF approach, which decreases the number of dielectric deposition steps and avoids additional dielectric layers in the stack.

Finally, the TF architecture is exactly the opposite of the VF architecture; the line is patterned before the via. Here, most difficulties are concentrated at the via lithography which becomes very critical when made on top of the trench topography. That is why the via first architecture is the most widely used architecture presently for technologies down to the 65 nm node [37, 39–42].

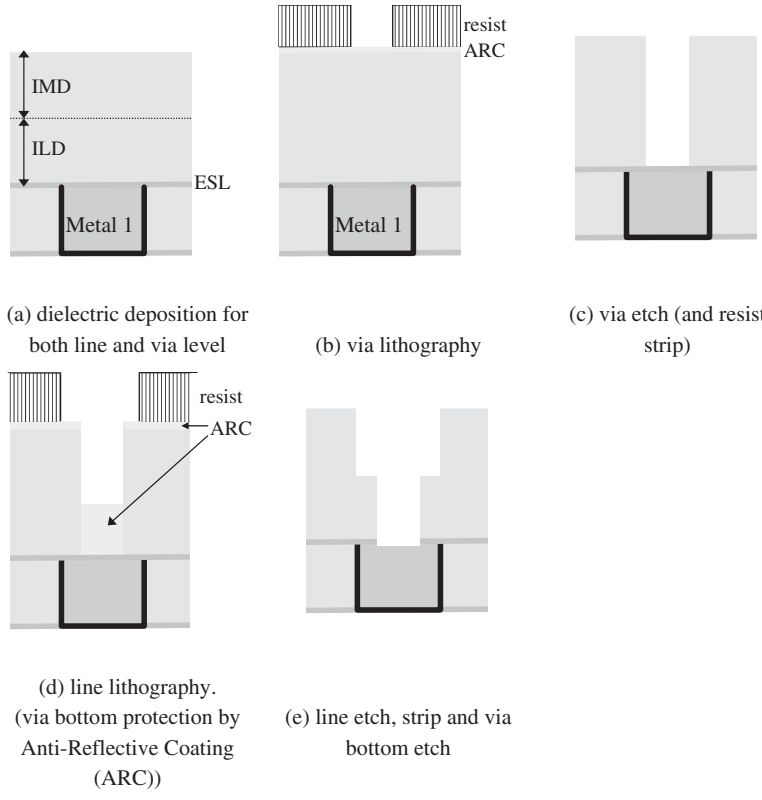

Figure 5.5 Schematic representation of the via first dual damascene approach

Novel dual damascene patterning schemes associated with low-*k* dielectrics

Moving from SiO_2 as dielectric to a low-*k* dielectric has added complexity in the dual damascene process integration. This is mainly due to the extreme sensitivity of low-*k* or porous low-*k* materials to etch, strip and wet chemical processes, as well as their compatibility with photoresist and shear forces during CMP. Regarding architecture, the first-mentioned challenge has resulted in resist poisoning by the underlying low-*k* material (see Section 3.1) which leads to missing patterns. For that reason, capping layers between low-*k* and resist have been proposed to avoid any direct contact. Moreover, hard masks have been implemented to minimize the exposure of ultra low-*k* to plasma sources (especially strip plasmas), see Figure 5.6. A dual top hard mask caps the low-*k* dielectric, avoiding any resist poisoning during lithography. Dual hard mask processes have more attractive merits in dual damascene integration [40, 45, 46]. The resist pattern is transferred in the upper hard mask, after which resist stripping is performed on top of the second hard mask without exposure to the low-*k*. In this way the dual hard mask suppresses process damage of the low-*k* [46]. In a final step the pattern is transferred in the low-*k*. Hard mask layers are chosen taking into account an optimal etch selectivity and a good ability to print sub-100-nm structures.

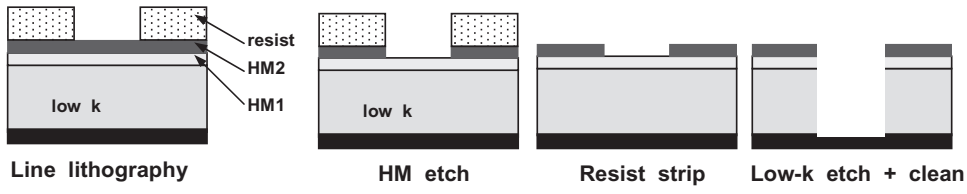

Figure 5.6 Damascene patterning with dual hard masks to avoid resist poisoning and strip damage on top of the low-*k* material

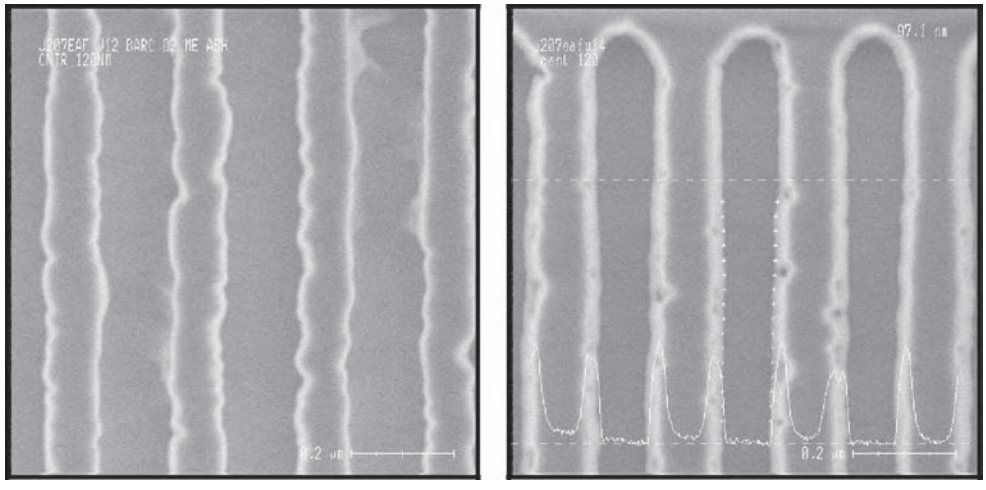

Figure 5.7 Top view SEM figures illustrating phenomena caused by a poor resistivity of the photoresist against the etch-plasma, resulting in; (left) deformation of the etched lines, (right) pitting in the dielectric.

As dimensions are getting smaller, the photoresist thickness needs to be scaled down accordingly. This thin resist layer in combination with poor selectivity and resistance of the new photoresist generations (248 and 193 nm) to fluorocarbon plasmas, leads to sidewall erosion and/or deformation of the resist mask [47] and hence to the etching/deformation of the patterning in the inter-metal dielectric (IMD, see Figure 5.7). In order to overcome these problems, bilayer resist systems or dielectric hard mask layers (see the discussion of etch stop and hard mask layers later in this section) are used on top of the IMD to be patterned.

Additional dielectric layers associated with damascene integration

As discussed in the previous paragraphs, multiple dielectric layers are necessary to construct a reliable interconnect using damascene patterning in low-*k* dielectrics. The following dielectric layers can be distinguished:

(i) *Etch stop layers* (ESL) between via- and trench-dielectric to permit a precise control of the trench etch, also referred to as embedded hard mask.

(ii) Single or multiple *hard mask layers* on top of the trench dielectric to facilitate lithography and etch processes.

(iii) *Copper diffusion barriers*, which cap the copper lines in order to prevent copper outdiffusion. Simultaneously, this layer must also protect the copper from corrosion during subsequent patterning steps and act as an etch stop for partially landed vias (and is therefore also referred to as a via etch stop layer).

A summary of the most common dielectric liners is given in Table 5.3. Typically, these dielectric layers have a thickness ranging from 30 to 150 nm. Traditionally in the first technology nodes, in which SiO_2 or FSG served as dielectric material, SiN was used as via ESL, line ESL, Cu diffusion barrier, and as single dielectric hard mask (HM). SiN ($k = 7$) was well adapted for first interconnect generations, since it exhibits a high etch selectivity with SiO_2-based dielectric materials. At the same time, reliable interconnects were achieved owing to the excellent adhesion properties between Cu and SiN.

However, due to the continuous drive towards lower effective k values of the entire stack, different materials with lower k values have replaced SiN (see Table 5.3). The introduction of SiOC materials in combination with SiN would have led to an increase of the SiN layer thickness, due to the low etching selectivity between SiOC and SiN [48]. To conclude, SiN layers were not any more suitable for high-performance interconnects and other layers were desperately needed.

Since the material, performance and reliability requirements for the dielectric copper barriers are quite different from the hard mask or etch-stop layers, they will be discussed separately.

Dielectric copper barriers. As discussed above, the continuous scaling of interconnects demands to lower the dielectric constant of all materials present in the dielectric stack. The insulating copper diffusion barrier represents one of these materials. The traditionally used dielectric barrier has been silicon nitride; however it has a relatively high k value ($k = 7$), compared with low-k dielectrics ($k < 3$). It can be understood that SiN has quite a dramatic contribution to the effective k value of the dielectric stack. Indeed, it has been shown that

Table 5.3 Effective dielectric constant for different low-k dielectric liners

Composition of low-k dielectric liner	Effective dielectric constant (k)
SiN	7
SiC_xN_y	4.5–5.5
SiC_x	3.5–5
SiC_xO_y	3.5–4
Bilayers:	3–4
SiC_xN_y/SiC_x	
SiC_xN_y/SiC_xO_y	

the effective k value can be lowered by almost 10% by replacing 50 nm SiN barrier with a barrier of k ~5 (SiC_xN_y) [48].

Most studies of films with $k < 7$ to replace silicon nitride have focused on PE CVD-grown silicon-based diffusion barriers that incorporate carbon with or without nitrogen or oxygen, e.g., SiC_xN_y [10, 48–53], SiC_x [50, 52, 54–56], SiC_xO_y [49–51, 57, 58] or bilayers (containing two of these materials) [59, 60] (see Table 5.3). These films necessitated the development of new precursors, such as tetramethylsilane (4MS) and trimethylsilane (3MS), which have replaced the standard silane (SiH_4). In addition, boron-based films are suggested as potential alternatives to the silicon-based diffusion barriers [61, 62].

Among the important diversity of proposed low-k barriers, SiC_xN_y is one of the most widely integrated dielectric liners for the 90 nm technology node. However, in the case of SiC_xN_y unwanted amines (NH_2 groups) may form and diffuse to the top surface of the dielectric stack. The latter might result in resist poisoning issues [63], such as 'footing'. Resist poisoning issues resulting from embedded layers can be solved by the use of new integration strategies, including dual hard masks.

The introduction of SiC_x, which has a lower dielectric constant than SiC_xN_y, shows improvement not only with respect to k value, but also etch selectivity to SiOC low-k dielectrics, resist poisoning, antireflective coating (ARC) behavior, adhesion strength to copper and low-k, and electrical and reliability performance [50, 64]. However, the relatively high film stress of SiC_x results in poor stack stability and a degraded interface quality of SiC_x/SiOC low-k [60].

To simultaneously achieve a low-stress and stable dielectric film, bilayers were proposed. For instance, Chiang *et al*. [59] recommended to combine dense SiC_x ($k = 4$) and SiC_xN_y ($k = 5$) layers; SiC_xN_y is first deposited on top of the Cu lines and prevents plasma-induced modification of SiC_x during the via opening and photoresist stripping processes. As an alternative, SiC_xN_y/SiC_xO_y bilayers could also be used. The dense SiC_xN_y (5 nm)/Cu interface provides efficient barrier properties against Cu diffusion; the second SiC_xO_y layer offers excellent adhesion properties with the upper SiOC low-k dielectric layer. Typically, bilayer approaches can provide an effective dielectric constant of the whole stack as low as 3.0 and could be considered for the 45 nm technology node and below in association with porous SiOC dielectrics ($k < 2.5$).

Most studies indicate that the incorporation of methyl group (H content) leads to a lower density and therefore a lower k value. However, as the density drops in these films, both their bulk properties (such as hermeticity) and the interface with copper (adhesion) can degrade. The critical diffusion path for EM has been attributed to the Cu/cap interface and therefore it is necessary to improve this interface to achieve reliable interconnects [65].

The *hermeticity* of dielectric copper barriers can be enhanced by using high power He plasma [66], which densifies the top surface, consequently preventing moisture uptake. Post-deposition plasmas (e.g., H_2, He, N_2 and O_2) may also be necessary to enhance the adhesion between the low-k barrier and the SiOC low-k dielectrics (Figure 5.8c). Obviously, oxidizing plasmas degrade the intrinsic physical properties of a dense low-k barrier, such as SiC_xN_y, however the impact of O-based plasmas is limited to the upper barrier surface, in contrast to porous layers, where damage can penetrate much deeper. This is a major issue for the integration of lower-k dielectric barriers (which are typically microporous).

The *adhesion* characteristics of the barrier/Cu and barrier/dielectrics interfaces can be enhanced by plasma treatments prior and after the low-k barrier deposition. A plasma treatment (e.g., NH_3) can reduce potentially existing copper oxide (CuO) at the metal line

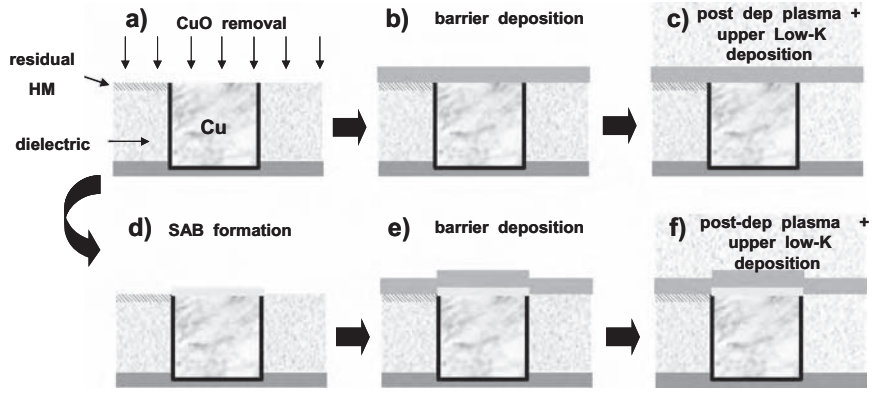

Figure 5.8 Schematic representation of the introduction of a low-*k* dielectric barrier for two integration schemes: 1) directly above the metal lines (a–c) or 2) within an hybrid stack on top of a self-aligned barrier on the Cu (d, e). After Cu CMP, the dielectric hard mask can be partially (left-hand side of metal lines) or completely removed (right-hand side) between the metal lines. The process describes CuO removal (a), self-aligned barrier deposition above the metal lines (d), PECVD barrier deposition step (b, e), and post-deposition plasma followed by the upper dielectric deposition (c, f)

surface after CMP [67, 68] and consequently enhance adhesion and electromigration lifetimes. However, as described in Figure 5.8(a), after a metal level is completed (i.e., after the Cu CMP process), the low-*k* dielectric between the metal lines is exposed (in the case where not dielectric HM has been used). SiOC low-*k* dielectrics, and more specifically porous ones, are very sensitive to plasma treatments (see the discussion of damage from low-*k* copping in Section 5.3.5). Therefore, when they are directly exposed to plasma treatments, they may be degraded and their effective dielectric constant may increase.

More recently, self-aligned Barriers (SAB), i.e., a selective formation or deposition of a metal barrier directly on the top of Cu metal lines, have been proposed as a replacement of the dielectric copper diffusion barriers (Figure 5.8d). It can be easily understood that a Cu/metal interface will demonstrate stronger adhesion properties than at the Cu/dielectric barrier interface. SAB techniques based on selective CVD [69, 70], electroless deposition [71–76], or copper surface modification [77, 78] have been studied. However, when SABs are integrated as a stand-alone process above the Cu lines prior the SiOC dielectric deposition, i.e., without any low-*k* dielectric liner, via over-etching cannot be prevented for misaligned vias. Furthermore, using the same configuration, the SAB must show barrier efficiency against Cu diffusion, a property that still needs to be demonstrated for most of the proposed processes. Finally, such processes are also very sensitive to plasma treatments (e.g., O_2), and bulk intrinsic properties could be modified, delaying the introduction of such process within Cu interconnects.

Therefore, a proposed architecture for SABs integration consists in introducing an hybrid stack to coat the Cu metal lines, i.e., a SAB surrounded with a thin low-*k* dielectric barrier (as depicted in Figure 8e,f). Using this technique, the SAB would provide reliability enhancement of interconnects as a result of higher adhesion properties with Cu lines, whereas the low-*k* dielectric liner prevents Cu out-diffusion, achieves over-etching control, and protect the SAB from plasma-induced modification. For instance, EM enhancement by

more than two orders of magnitude was demonstrated using a CoWP/SiN hybrid architecture [79]. As a consequence, low-*k* barriers liners will require adapted pre-deposition plasma treatments to strengthen adhesion properties with the SAB, and not Cu, for such approaches.

Etch stop and hard mask layers. As discussed previously, the dual damascene integration of porous low-*k* materials requires novel integration schemes, including embedded etch stop layers and dual hard masks. Since these layers contribute also to the effective *k* value of the dielectric stack, the traditionally used silicon nitride and silicon oxynitride films have been replaced by materials such as SiO_2, SiC_x and SiC_xN_y [48, 80]. To push the *k* value down even further, organic hard mask and etch stop layers, such as plasma-polymerized BCB (k = 2.7) [80], or the spin-on films FF-02™ [81, 82] from JSR Corporation and Ensemble™ [83, 84] from Dow Chemical has been proposed as replacement of the PECVD Si-based dielectrics. The last two materials have been proposed to provide a full spin-on integration scheme and were shown to present higher etch selectivity than PECVD barriers with SiOC low-*k* dielectrics [81–83].

The main disadvantage of dielectric hard mask layers is the selectivity with respect to the low-*k* dielectric (e.g., SiOC) to be etched, which implies the need for relatively thick hard mask layers. In order to address this problem metallic hard masks or metallic oxides have been introduced; TaN, TiN or Al_2O_3 [85–87]. The metallic hard mask show the best patterning result with respect to selectivity towards the underlying layers (Figure 5.9). Due

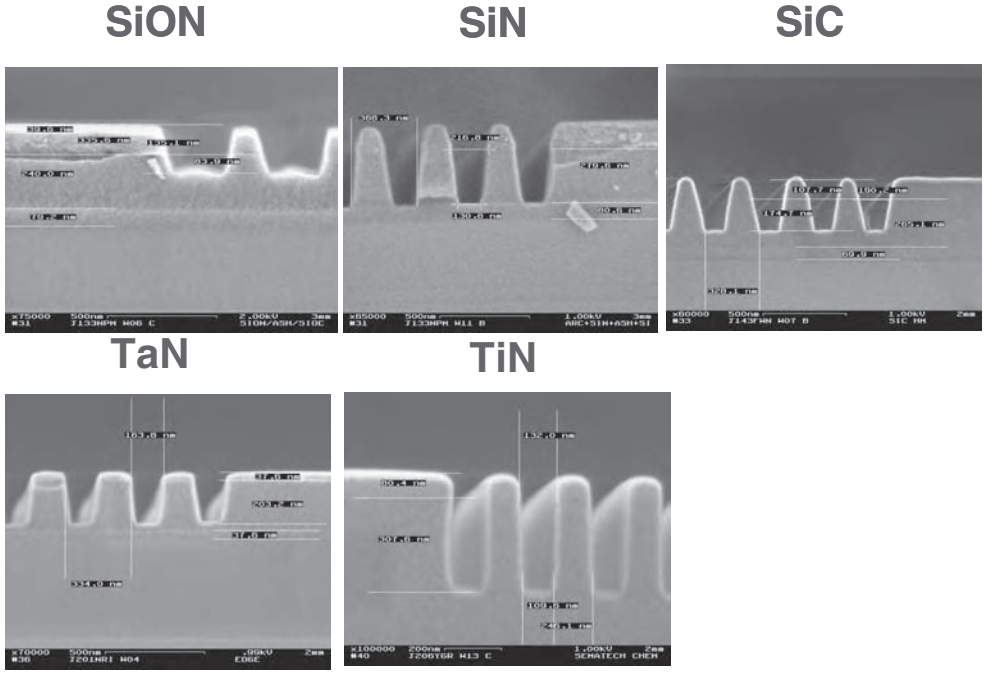

Figure 5.9 Different types of hard masks used to pattern the dielectric. In the top images cross-section SEM pictures show the dielectric profiles after etch using the dielectric hard masks (SiON, SiN and SiC), while in the bottom images the profiles are shown for the metallic hard masks (TaN and TiN). (Courtesy of the Crolles2 Alliance)

to this high etch selectivity, the hard mask thickness can be reduced, which gives rise to a smaller topography enlarging the lithography process window for the second pattern in the dual damascene process. Nevertheless, care has to be taken that the metallic hard mask is completely removed during the CMP process in order to have a minimal interline leakage.

5.3 LOW-*k* INTEGRATION CHALLENGES

5.3.1 Resist poisoning

With the introduction of low-*k* dielectrics, new integration issues have appeared. One of them, called 'resist poisoning', has been mainly reported during the integration of SiOC low-*k* and porous low-*k* materials [19, 88–91]. During the line lithography of dual damascene patterns, it has been observed, when the commonly used 'via first' architecture is employed (see Section 5.2.2). This resist poisoning effect is an alteration of the development process of chemically amplified photoresists by an alkaline contamination. After lithography, incomplete resist development (Figure 5.10a) leads after etch to unwanted fences in trenches around vias (Figure 5.10b), and eventually, after metal filling, to bad electrical contact (open) between via and top metal line. This resist poisoning effect is amplified by an interaction of several factors: resist, materials, integration architecture and integration processes [63, 92]: their respective implications in the via poisoning phenomenon are described:

- The deep ultraviolet (DUV) resists used (248 or 193 nm wavelength) are based on a chemical amplification. During light exposure and the post-exposure bake of positive resists, acids are generated which catalyze the resist deprotection reactions [63, 93]. These

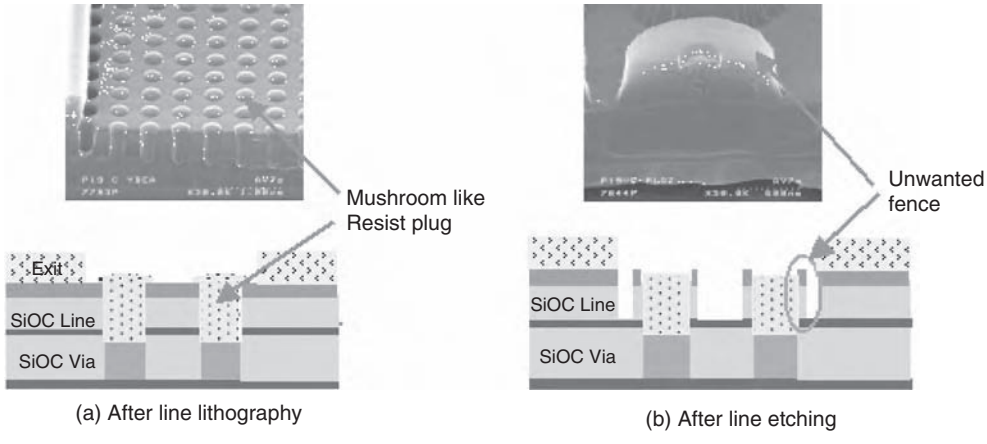

Figure 5.10 'Resist poisoning' issues observed in the via first dual damascene architecture; (a) after line lithography (incomplete resist development of the poisoned resist in vias leads to unwanted mushroom like resist plug); (b) after line etch (unwanted fences around vias). (Courtesy of CEA-LETI)

resists are then very sensitive to any alkaline contamination, since the latter can neutralize these reactions. Very small concentrations (a few ppb) of airborne amine are known to easily contaminate DUV resists [93].

- Since the introduction of *low k materials*, dielectrics are microporous (e.g., 'dense' SiOC) or porous (e.g., porous SiOC) which implies that they can retain volatile species in their volume: i.e., they act as reservoirs. They easily retain contamination from ambient or previous process steps. Therefore, usually a dense capping layer (such as SiO_2) is used on top of these dielectrics, preventing any direct interaction between the resist and the material.
- However, in the commonly used '*via first architecture*', line lithography is performed on opened vias. So locally, in vias areas, the line resist can be in direct contact with low-*k* dielectrics (Figure 5.10a).
- Standard technological *processes* such as stripping or cleaning usually contain alkaline species as amines. Particularly in the via-first approach, where the via stripping and cleaning are performed just before line lithography, nitrogen contamination from the via stripping can lead to missing via links (i.e., trenches).

Indeed, the main cause of resist poisoning is due to amines generated during via stripping and cleaning which are trapped in the volume of the 'porous' dielectric [94]. During the subsequent line lithography step, amines can be released through the opened vias and poison the resist locally. This leads to incomplete resist development and localized residues, inducing unwanted masking during the following etch step. In addition, all materials or processes containing nitrogen (as SiC_xN_y barrier layers and etching or stripping chemistries) can also generate amines (mostly by reaction with moisture) and then induce resist poisoning [63, 92].

Quantifying 'the poisoning potential' of a process can be very difficult, as minimal quantities of amines are sufficient to create the phenomenon. Thermal desorption gas chromatograph mass spectroscopy (TD-GCMS) [19, 95, 96], Multiple internal reflectance Fourier transform infrared (MIR-FTIR) spectroscopy [97] and time-of-flight secondary ion mass spectroscopy (TOF-SIMS) [96, 97] proved to be sensitive enough to reveal amine presence, but are rather costly. Meanwhile, indirect methods, like 'dose-to-clear compensation methods' [98, 99] can easily be used to compare photoresist poisoning effects of different processes, resists or materials.

The poisoning issue is usually more severe on isolated vias or on vias located at the patterns corners (as shown in Figure 5.11a), due to the larger reservoir volume (of the 'porous' dielectric) per via in this configuration. Porous low-*k* materials are also more prone to resist poisoning, due to their larger free volume compared with dense dielectrics [89, 97, 99].

Finally, several solutions were proposed to overcome this issue. Suppression of all amine sources (material and processes without nitrogen [63, 92]), or resist robustness improvement [91] minimize the problem (Figure 5.11b), but cannot really eliminate it. Nevertheless, an architecture modification, e.g., using a dual hard mask (see Figure 5.6) to prevent any contact between the resist and the low-*k* material, can offer a definite solution [89, 100].

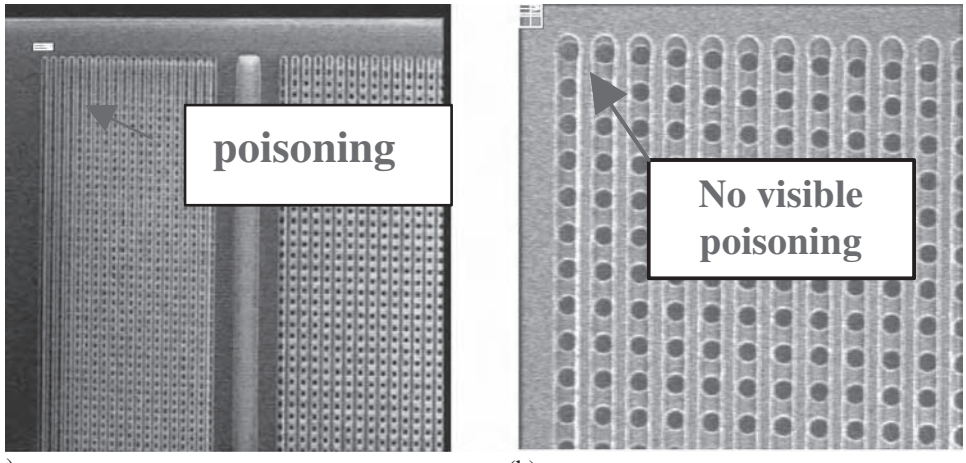

Figure 5.11 SEM top view images after line lithography in via-first architecture, showing: (a) poisoning at the pattern corners when amine based processes are used; (b) no visible poisoning after suppression of all amines sources in the integration process. (Courtesy of CEA-LETI)

5.3.2 Compatibility of low-*k* materials with wet cleaning

Cleaning of wafers is necessary after certain critical processing steps such as etch, photoresist stripping and post-CMP residues removal. In addition, for dual damascene, wet clean processes need to be implemented after via etch. Since at that moment the copper of underlying metal layers is exposed during etch, it tends to be contaminated with CF_x, CuF_x, CuO and Cu_xO by-products [101, 102]. The removal of Cu by-products or contaminants from the damascene structure is very important before the metallization can start. This cleaning must be able to effectively remove any etching by-products [88, 103], such as polymeric residues (as illustrated in Figure 5.12) and the re-sputtered copper onto the sidewall as well [104]. This copper has been redistributed from the via bottom onto the sidewall during the 'final' etch or during the pre-(barrier) clean. The trapped copper between the dielectric and the metallic barrier can lead to increased leakage and poor reliability. The presence of polymeric residues at via bottom or sidewall could cause an electrically failing via [39] or reliability issues after processing [105]. All of the above implies that wet cleans are inevitable during the integration of multiple level copper interconnects.

However, due to the porous nature of many low-*k* dielectrics, they are extremely susceptible to absorption of wet cleaning liquids. These films can be significantly affected when interacting with liquids during various processing steps. Typical wet strip compatibility checks are done by *k* value, FTIR and ellipsometry measurements [106]. One of the issues, which can be demonstrated by the latter, is film swelling, which causes a change of the film volume due to solvent absorption. The degree of swelling depends on the overall rigidity of the film skeleton. Swelling can be quite substantial, especially for the organic polymers [25, 107].

Traditionally, dilute HF has been used for wet removal of copper oxides and surface conditioning [108], due to its effectiveness and low cost. The problem with porous low-*k*

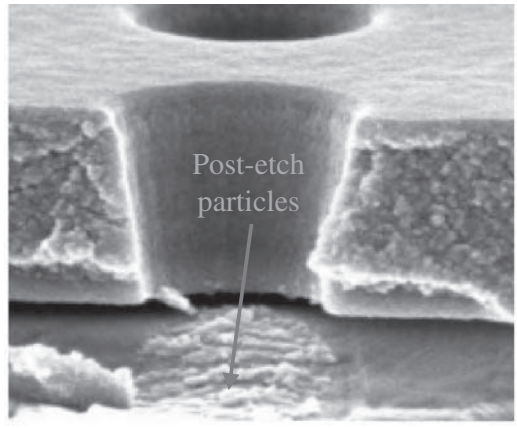

Figure 5.12 Cross-section SEM picture showing post-etch residues at the bottom of a via hole after via etching. (Reproduced with permission from SEMATECH)

materials is however the compatibility with the damaged sidewall, which is often also removed during this clean (more details can be found in Section 5.3.5). New, more compatible, and efficient chemistries are emerging. Very dilute organic acids mixed with adapted surfactants have shown good results, although water and surfactant absorption into the pores remains an issue [109]. Nitrogen-containing post-etch cleaning chemistries can result in amine contamination on the low-*k* surface [96]. Amine contamination is detrimental for the lithography process, since it can lead to poisoning of chemically amplified DUV resist (as was discussed in Section 5.3.1).

Most of the back-end-of-line post-etch/ash cleans are performed in a spray tool or wet bench with a commercially available solvent. Removal of the etch residues and ash residues has been accomplished primarily by dissolution. It is challenging to implement physical cleaning methods, such as megasonics, for low-*k* cleaning, because of possible damage to sensitive structures. High-cleaning-efficiency ultrasonic or megasonic chemical agitation can physically crack or rupture the fragile, free-standing, high-aspect-ratio dielectric 'walls' temporarily created during damascene fabrication schemes. Reducing the aggressiveness of the bath agitation generally requires extending the immersion time to compensate for the reduced cleaning efficiency [110].

New emerging technologies such as cryogenic cleans [111], and supercritical fluids [112, 113] are under investigation. Supercritical carbon dioxide ($SCCO_2$) efficiently removes contaminants trapped in the pores and facilitates the low-*k* damage repair using organic molecules, such as hexamethyldisilazane (HMDS) or equivalents (see Section 5.3.5). Cleaning effectiveness remains to be a delicate balancing act with respect to the low-*k* compatibility. However, new cryogenic surface-conditioning approaches might offer a solution.

5.3.3 Compatibility of metallic diffusion barriers with low-*k* materials

As discussed in Section 5.2.1, copper diffuses rapidly through silicon, silicon oxide and other dielectrics and it adheres poorly to most dielectrics. Because of these issues, a metallic

barrier layer is generally needed between copper and the dielectric, providing interfacial mechanical strength and preventing copper diffusion. In addition, the barrier layer should be as thin as possible, in order to maintain a low wire resistivity. The most promising candidates for the barrier material are refractory metals and their nitrides; Ti, Ta, TiN, and TaN, partly due to the fact that these materials had also been used in aluminum metallization [114]. These metallic barriers can be deposited in damascene structures using either physical vapor deposition (PVD) or chemical vapor deposition (CVD).

Physical vapor deposition (PVD) is a process, in which a thin film of material is deposited on a substrate according to the following sequence of steps:

1. Material to be deposited is converted into vapor by physical means;
2. Vapor is transported at low pressure from its source to the substrate;
3. Vapor undergoes condensation on the substrate to form the thin film.

In very-large-scale integration (VLSI) fabrication, the most widely used method of accomplishing PVD of thin films is by sputtering, wherein atoms or molecules are ejected from a target material by high-energy particle bombardment and subsequently the ejected atoms or molecules can condense on a substrate as a thin film. Due to the directionality of the metal ions, the condensed metal film is nonconformal on topography.

Chemical vapor deposition (CVD) refers to the formation of a nonvolatile solid film on a substrate from the reaction of vapor phase chemical reactants containing the right constituents. A reaction chamber is used for this process, in which the reactant gasses are introduced to decompose and react with the substrate to form the film. CVD processes are ideal to use for thin films with good step coverage.

These two different deposition techniques result in different challenges when applied on porous low-*k* materials. The main risk of 'thin' PVD barriers is the appearance of pinholes in the barrier, resulting in copper diffusion in the dielectric (right-hand illustration in Figure 5.13), while for atomic layer (AL)CVD barriers precursor penetration can occur inside the dielectric (left-hand illustration in Figure 5.13). In the next two sub-sections the challenges related to both deposition techniques of metallic barriers on low-*k* dielectrics will be discussed in more detail.

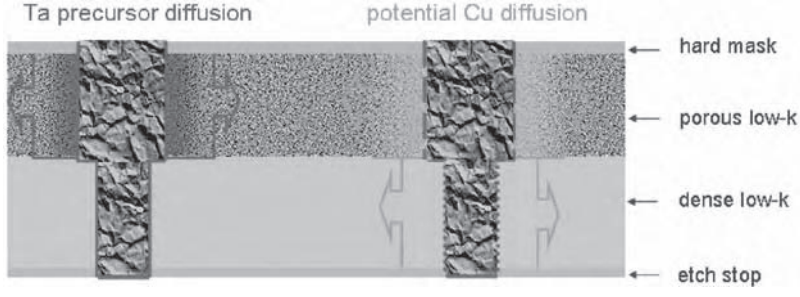

Figure 5.13 Two problems that are encountered during metallization: (1) Ta precursor diffusion inside the porous low-*k* material can occur using ALD or CVD barrier deposition; (2) copper diffusion can occurs in the dielectric, if very thin PVD films are deposited, which tend to be discontinuous

Physical vapor deposition

For future process generations, uniform and conformal deposition of thin barrier/seed combinations is required for barrier efficiency and robust gap-fill. However, this becomes difficult to achieve with PVD [115] due to the shrinking line and via dimensions. The intrinsic problem with PVD is the directionality of the sputtered metallic atoms during deposition, which results in nonconformal barrier coverage. The barrier coverage is larger at the field than at the sidewall, as can be seen in Figure 5.14. The main problems that could arise due to a nonconformal PVD barrier coverage are the higher via resistance due to thick barrier on the via bottom [116] and the limited thickness of the barrier on the sidewall,

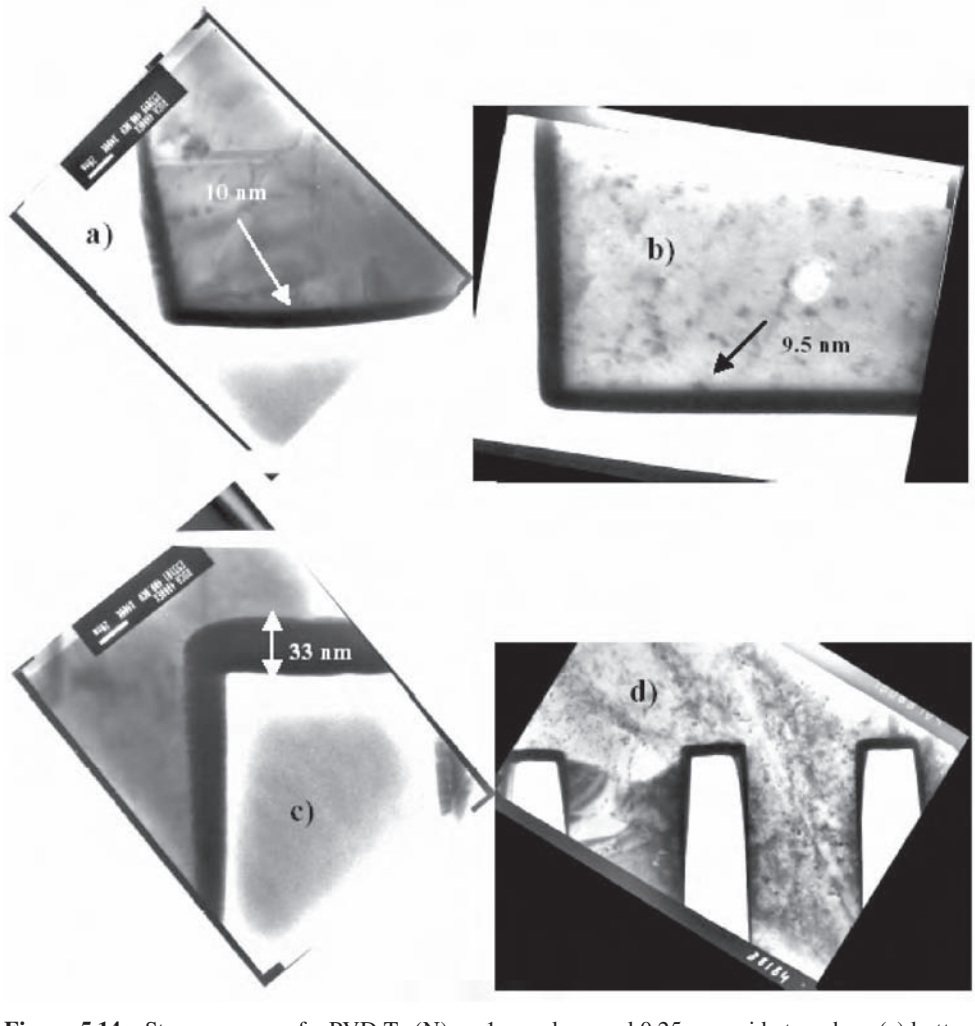

Figure 5.14 Step coverage of a PVD Ta (N) on 1-μm-deep and 0.25-μm-wide trenches: (a) bottom of the trench without etch stop; (b) bottom of the trench with etch stop; (c) field coverage; (d) sidewall coverage. (Courtesy of IMEC)

enabling rapid diffusion of Cu into the dielectric (as illustrated in Figure 5.13) and the generation of voids during Cu electroplating [94]. Further scaling could eventually result in a discontinuous film on the sidewall, creating easy copper penetration pathways inside the dielectric and Cu diffusion into the active areas, leading to a significant reliability and performance loss. In addition, it will be very difficult to close pores on sidewall surfaces of porous low-*k* materials (especially at the sidewall region and near the via-trench bottom), unless very thick films are deposited. Thick metallic barriers are not acceptable, since the copper volume in the lines should be kept as large as possible, in order to keep the line resistivity low. If thin PVD films are applied on mesoporous materials, a neck will be formed over the pores resulting in discontinuous barrier films (schematically depicted in Figure 5.15). The neck or overhang causes a 'shadow', preventing further deposition on the underlying part of the pores. This phenomenon is even worse at the trench and via sidewalls, where the coverage is limited by the poorer step coverage.

For dielectric films with higher porogen loads, there is an enhancement of the probability that the mesopores will end up so close to each other that their necking connection will be affected. Iacopi *et al*. [117] postulated that if the size of this interconnection becomes comparable to the size of the mesopores, the pore structure becomes open (as shown in Figure 5.15b), and so a conformal coverage is no longer possible. These pores will need to be bridged by the PVD deposition, so that a substantially thicker barrier layer is needs to be deposited to achieve an efficient sealing. Sun *et al*. [118] claim that, due to the increasing pore sizes, the roughness of the low-*k* surfaces increases, which has a dramatic influence on the barrier continuity.

The sealing efficiency of thin barrier layers depends however not only on the porosity [117] and pore size [118, 122], but also on the surface composition of the dielectric [119]. A strong correlation was found between the carbon content of the dielectric and the sealing efficiency of PVD Ta(N) films on porous low-*k* films. Higher carbon concentrations lead

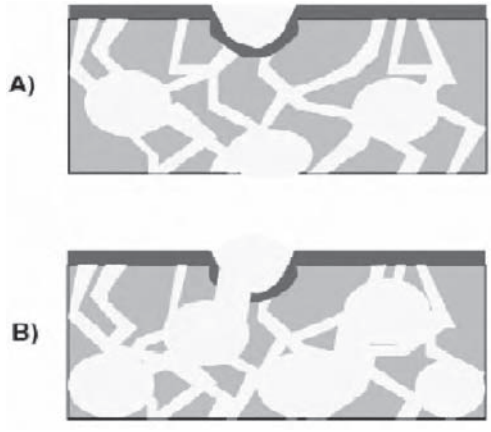

Figure 5.15 Pore structure in a mesoporous dielectric film: sacrificial nanoparticles (porogens) generate mesopores connected by the original microporosity of the matrix MSQ material. The mesopores appearing at the surface can be conformally covered by thin PVD deposition (A). When the porogen load percentage of the films is increased (B), part of this closed pore structure can be converted into an open one (with necking comparable to the pore size): these pores can only be sealed by bridging them with a thicker cap layer

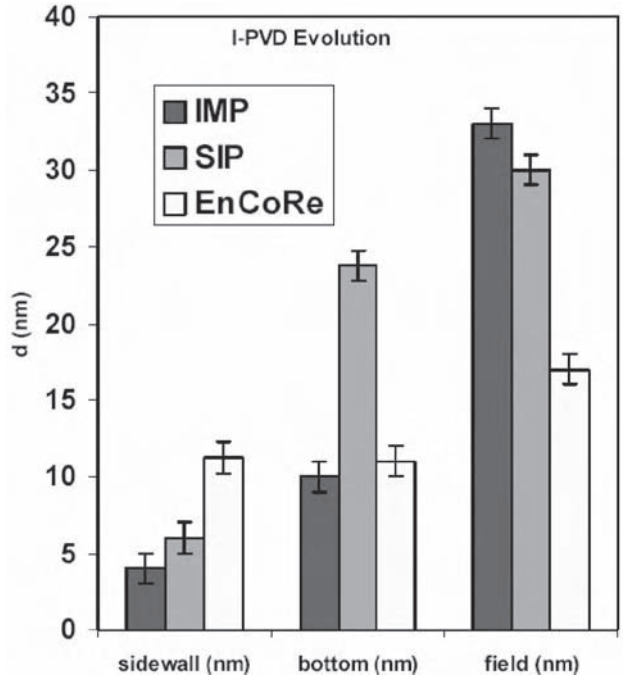

Figure 5.16 Step coverage evolution for different PVD techniques obtaining in 250-nm-wide oxide trenches (AR = 4). IMP (ionized metal plasma) was the first generation of PVD sputtering tools, following by SIP (self-ionized plasma) and more recently Applied Materials introduced an improved SIP technique, namely EnCoRe™. (Courtesy of IMEC)

to pore sealing with thinner barrier films in conditions of similar pore size and porosity. The tendency of Ta to react with carbon at the dielectric surface can lead to the formation of Ta-C [120, 121]. Iacopi *et al*. [119] proposed a model based on the formation of a transition layer at the Ta (N)/dielectric interface where Ta acts as a catalyst that locally promotes cross-linking (i.e., densification) of the matrix.

To overcome these drawbacks and to be able to tailor the barrier profile, the most advanced ionized PVD techniques enhance conformality through source design, process optimization and re-sputtering (like substrate-biased deposition or deposition/etch processes) [122–124]. This technology trend in order to achieve better barrier conformality for PVD is schematically shown in Figure 5.16, where the field, sidewall and bottom barrier coverage for three PVD barriers are compared. Therefore, it can be expected that PVD will remain the preferred and viable technique for several technology nodes. However, the inherent anisotropic character of this technique requires a continuous innovation of both technology and material science (interactions between sputtered metal and low-*k*).

Chemical vapor deposition

There are multiple films being developed as replacement for the PVD metallic liners. The leading candidates are metal nitride alloys, such as WCN [125, 126], TaN [115, 127–130]

and TiN [125], deposited by deposition methods such as chemical vapor deposition and atomic layer deposition (ALD). All three candidates can form ultra-thin (1–2 nm) barriers films with excellent conformality. The growth of these ultra-thin, conformal copper diffusion barriers by ALD is based on chemically saturated surface reactions that are *sequentially repeated* to create a *layer-by-layer growth* mode, which is in contrast to conventional CVD where all precursors are led into the reactor at the same time. The self-limiting nature of this chemisorption process in the ALD reactor gives rise to a very uniform and conformal growth behavior and full control over the total stack thickness just by fixing the amount of sequential cycles. Hence, ALD shows excellent step coverage in very-high-aspect-ratio trenches and vias (as illustrated by the three images in Figure 5.17). Additionally, high-quality conductive films can be deposited at low temperature with low defect density, good thickness uniformity and accurate thickness control. Therefore, ALD is expected to be a potentially ideal method to prepare thin and conformal diffusion barriers and/or nucleation layers for future IC generations when conventional PVD is running out of steam.

Low-k *compatibility with ALD processes.* However, there are still some problems to be solved before ALD can be successfully applied and integrated into future ultra low-*k* process flows. The starting surface condition plays an important role for the growth behavior during the initial stages of growth [125, 131, 132]. This is attributed to either a different density of functional, reactive groups on the substrate surface (e.g., –OH versus $–NH_2$ ligands) or to a different reactivity of these groups with the precursor molecules. If the density of functional groups and/or the reactivity is too low, the nucleation of the ALD film is severely hampered which could result in an island-type growth behavior rather than layer-by-layer growth during the initial cycles of growth [132].

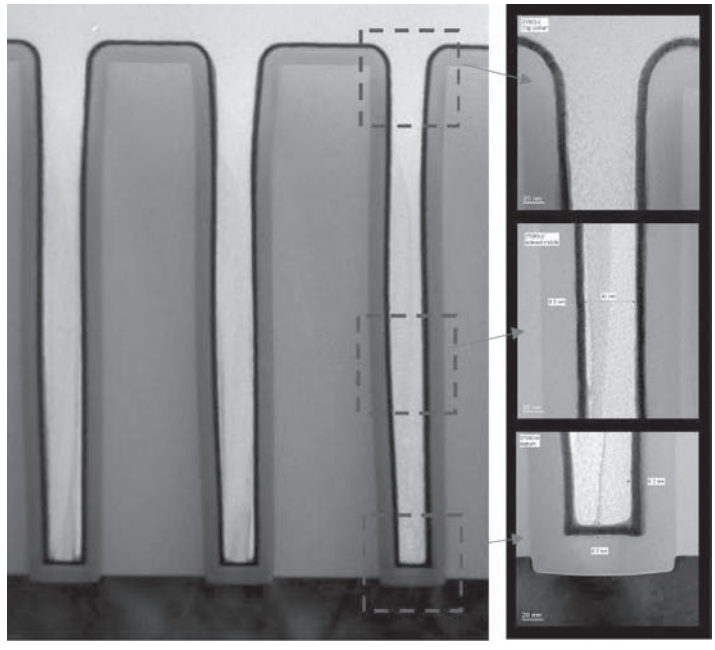

Figure 5.17 TEM micrographs of ALD WCN grown in deep trenches. (Reproduced by permission of ASM)

The growth behavior of ALD layers can be studied using Rutherford backscattering spectroscopy (RBS) or X-ray fluorescence (XRF) [131] by measuring the total number of deposited Ta atoms. The total amount of material deposited as a function of the number of applied cycles (i.e., the growth curve) can be better interpreted if the derivative of this curve is plotted as function of cycle number, i.e., the growth per cycle (GPC). Four different growth modes (Figure 5.18) are described in literature, depending on number of initial chemisorption sites and the growth chemistry [133]. Substrate-inhibited growth of type I and II originates from a limited substrate reactivity. The increase in GPC (i.e., the amount of material deposited per cycle) indicates an island-like growth behavior.

An example of substrate inhibited growth behavior is shown in Figure 5.19. If the initial density of active surface groups is small, the deposition will take place predominantly on already-deposited TaN material and an island-like type of growth behavior will occur. Accordingly, it will take a large number of cycles before the islands touch each other (Figure 5.19). In Figure 5.20(a), RBS spectra of Ta are shown for different deposition cycles of ALD TaN on SiOC. The area density of Ta is extracted from the RBS spectra and plotted as function of cycle number to obtain the growth curve. In Figure 5.20(b), the ALD TaN growth curves on a CVD SiOC surface are shown for different surface treatments. As can be seen, the amount of deposited material is significantly increased by the use of argon (RF) or hydrogen reactive pre-clean (RPC) plasmas prior to the precursor exposure, whereas on pristine or HF-treated SiOC surfaces hardly any material is deposited.

The selectivity for precursor adsorption on pristine SiOC surfaces originates from the low amount of reactive surface groups on the surface (presence of predominantly unreactive methyl groups), while argon or hydrogen plasmas enhance the number of reactive sites significantly by creation of dangling bonds and/or OH groups. After 20–50 deposition cycles, the growth curve of the plasma-treated samples starts to manifest the expected linear trend. In the linear regime the number of reactive sites no longer varies and the amount of material deposited per cycle (GPC) becomes constant. However, it is difficult to determine the point where the film becomes closed and pinhole-free.

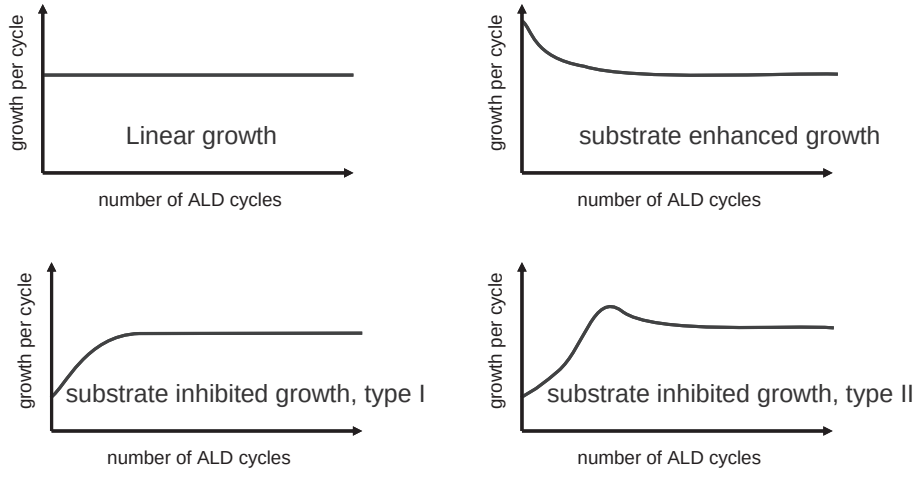

Figure 5.18 Different growth modes encountered during ALD depending on the surface condition such as chemistry, availability, and accessibility of reactive sites

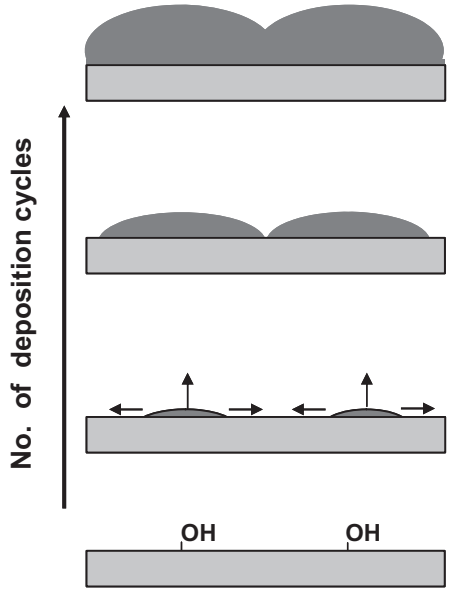

Figure 5.19 Schematic representation of island-like growth mechanism

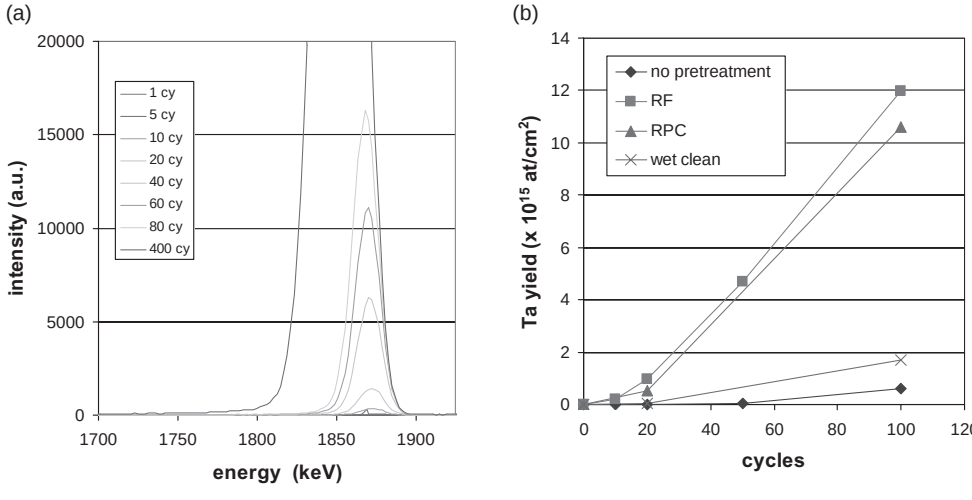

Figure 5.20 (a) RBS Ta spectra; (b) ALD TaN growth curves on CVD SiOC substrate for different surface treatments (RF: argon pre-clean, RPC: reactive pre-clean or hydrogen preclean, wet clean: HF surface treatment)

For copper barrier applications, pinholes are highly undesirable since they form a leakage path for copper ions. HF-dip decoration studies have been used to show a good barrier conformality and continuity performance in high-aspect-ratio SiO_2 structures [123, 134]. Although the HF-dip test illustrates that the ALD barrier does not show evidence of pinholes on SiO_2, it does not guarantee pinhole-free growth behavior on a CVD SiOC die-

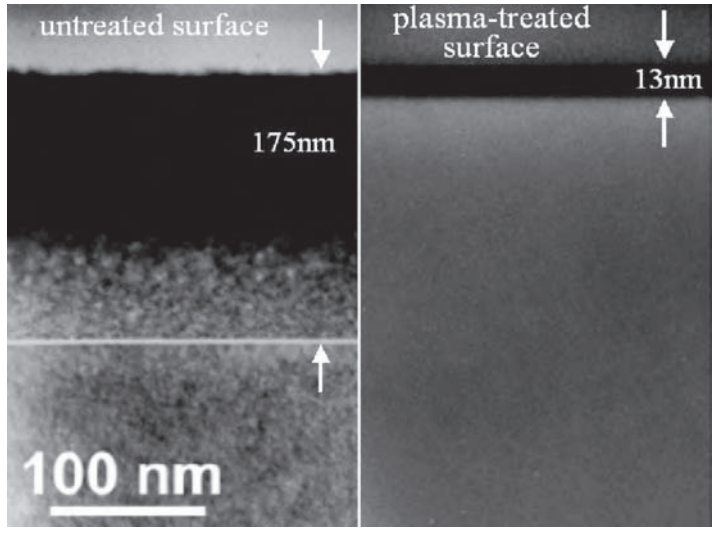

Figure 5.21 TEM images of ALD WCN deposited on a porous SiOC film with (left) an untreated surface and (right) an N2-plasma exposed surface. (Courtesy of IMEC)

lectric, since SiOC does not get etched by HF. Therefore, Satta *et al*. used low-energy ion scattering (LEIS) to test the continuity of ALD TiN films on SiO_2 [132]. A less expensive method is time-of-flight secondary ion mass spectroscopy (TOF-SIMS) [135].

An additional problem arises when the ALD technique is combined with porous low-*k* materials. Diffusion of reactants into the dielectric during ALD deposition is a major concern [27]. The precursor penetration initiated metal deposition in the form of islands through almost the entire dielectric layer (as can be seen in the left-hand TEM image of Figure 5.21). Increasing the size of the precursor molecules can prevent the penetration. Bulky metal organic ligands will help to avoid massive diffusion into the low-*k* material if the pore diameter of the dielectric is not too large. Another method to prevent precursor diffusion is to seal the pores by use of additional treatments, such as plasma exposure. In the right-hand TEM image of Figure 5.21, a clear sharp interface can be observed between the ALD layer and the low-*k* surface, as well as the absence of precursor in-diffusion. The latter has been established by plasma sealing of the low-*k* surface.

In summary, ALD seems to be a promising technique to achieve conformal barrier deposition in narrow vias and trenches. However, before it can be successfully implemented on porous low-*k* surfaces, two compatibility problems need to be solved, namely substrate-inhibited growth and precursor in-diffusion. Choosing a proper sealing layer can solve both issues. Pore sealing of low-*k* surfaces will be discussed in detail in Section 5.3.4.

5.3.4 Pore sealing

Most porous ultra-low-*k* dielectrics have a highly interconnected pore structure. Due to this porous structure, liquid and/or gaseous species can easily fill the pores of the low-*k* matrix during various processing steps, such as dry etching, wet cleaning and atomic layer

deposition (ALD). Fortunately, the highly interconnected pore structure also enables techniques, such as positron annihilation lifetime spectroscopy (PALS) [136, 137] or ellipsometric porosimetry (EP) [138], to characterize the effectiveness of different sealing methods. Since, in both cases, a probe (positronium in the case of PALS and a solvent vapor in the case of EP) can diffuse through the porous material and an effective sealing layer will reduce this diffusion. The two common sealing approaches, which have been proposed in the literature to prevent diffusion, are either deposition of very thin PECVD liners stuffing the pores or pore sealing by a proper plasma treatment (sidewall restructuring). In the following sub-sections the two techniques will be discussed in further detail and in addition some alternative sealing methods will be presented.

Pore sealing by liner deposition

The use of a dielectric liner to improve the robustness of copper interconnects fabricated in porous low-k dielectrics was first reported in 1997 [139, 140]. The principle of this sealing approach is based on the deposition of an additional layer (also called 'liner'), either a CVD inorganic or a spin-on or plasma-polymerized (in)organic material. This liner stuffs the pores at the top surface and at the trench sidewall. Examples of the CVD liners are SiO_2 [139–144], SiC_xN_y [142, 143, 145–147] and Si_3N_4 [142, 146, 148] and on the other hand the most known plasma-polymerized liner is BCB [149, 150]. The k value of BCB ($k = 2.8$) is lower than that of SiO_2 ($k \sim 4$), which in turn is lower than that of SiC_xN_y and Si_3N_4 ($k \sim 5$–8). Therefore, based on the lowest effective k value, the preferential choice for pore sealing would be BCB, followed by SiO_2 and SiC(N). However, generally the pore sealing efficiency decreases with the k value (due to decreasing density of the pore sealant), which could mean that thicker BCB layers are needed compared with SiC_xN_y layers. In addition, the step coverage in narrow via/trench combinations of these materials is something which should receive sufficient attention.

The success of pore sealing by dielectric liners has been demonstrated by an improvement in both interline leakage [142, 147, 148, 151] and dielectric breakdown strength [142, 146, 147]. It has even been tried to replace the conventional PVD metal barrier with a dielectric liner as sidewall diffusion barrier [152], however this change may cause other integration problems, such as delamination, since the Ta(N) layers also serve as adhesion promoter between the copper and the low-k dielectric.

Dielectric liners are typically deposited after full damascene patterning of the porous film, but before the breakthrough of the bottom SiC_xN_y. Afterwards, both liner and bottom cap need to be opened, to ensure electrical contact to the lower metal level. Such dielectric removal steps for the via bottom have been successfully realized and integrated in dual damascene processes without compromising the via contact resistance [152]. However, one of the drawbacks of this approach can immediately be observed in Figure 5.22, which shows a schematic representation of this pore sealing method. During the etch-back of the liner, and breakthrough of the bottom SiC(N), the pores at the top surfaces run the risk of being opened again. To overcome this problem, one could implement embedded and top hard masks capping the pores at the top surfaces; however, this approach yields higher effective k values of the integrated stack and in addition more process complexity.

Another drawback of the liner approach is the fact that in the case of low-k materials with large pore sizes (>2 nm) relatively thick layers (>10 nm) are needed to achieve efficient

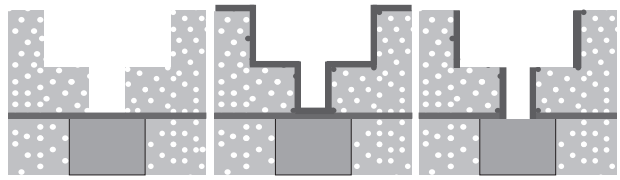

Figure 5.22 Schematic representation of an integration route using a dielectric liner in order to achieve pore sealing

pore sealing [119]. Thick liners are not compatible with future technology nodes, since this will increase the overall *k* value of the stack and increase the line resistivity due to the reduced line width. In addition, all additional steps, needed to seal the porous sidewall by a dielectric liner will increase the manufacturing cost substantially.

Finally, a slightly different liner technique has been reported in the literature, which seals the porous low-*k* layers with a smooth coating of silica just a few nanometers thick, based on a catalytic growth [153]. The maximum depth, to which the pores are filled by the silica, is controlled by the depth to which the aluminum catalyst was deposited. It is however questionable whether this techniques will be suited for porous materials with a large pore size, since these materials are easily filled with ALD precursors (depending on their molecular size).

Plasma sealing

Microporous low-*k* SiOC materials (i.e., a pore diameter smaller than 2 nm) have been shown to seal upon exposure to plasmas through reconstruction or densification of the low-*k* surface, creating a dense SiO_2-line layer [154–156]. The densification can also be denoted as plasma damage, leading to an increase of the *k* value and to a degradation of the electrical properties (see Section 5.3.5). A good knowledge and control of these plasma processes is therefore essential in providing a scalable solution. Nevertheless, for microporous dielectric films, the densification can be confined into a few nanometers of the surface, provided the appropriate choice of plasma power [155]. Higher plasma power/bias were found to be necessary to seal as the porosity of the low-*k* material increased [154]. For materials with a high porosity and a large pore diameter, the amount of material, which needs to be restructured/redeposited, is not enough to close the surface [157]. In general, the effect of plasma treatments can easily attain several hundreds of nanometers depth in such dielectrics [158].

Gas cluster ion beam (GCIB) processing has been identified as a potential candidate for low-damage pore sealing, since the extent of the plasma damage is claimed to be minimal [159, 160]. GCIB processing is a novel method of treating surfaces using a high-energy beam (1–30 keV) of atomic or molecular clusters ($n > 5000$). The overall cluster energy is high, but the individual atomic kinetic energy is low, so the clusters interact with only the top surface of the sample, which could be beneficial for minimizing bulk low-*k* damage.

Microporous SiOC films can also be sealed using a UV–O_3 photochemical process, however it should be noted that it is accompanied with a thickness loss of ~10% [161]. Such a large extent of low-*k* damage is unacceptable.

For organic polymers, the case is slightly different than for SiOC-type materials. ALD precursor penetration is even observed for the dense organic materials [27, 162]. The relatively small precursors (WF_6 and NH_3 for ALD WCN) can easily diffuse through the free volume of the polymer matrix. It has been found that reactive plasmas (especially O_2) can densify the polymer surface [27, 162]. The composition of the plasma is crucial. Exposure to plasmas results in a decrease in H_2O-contact angle, which suggests incorporation of polar groups into the polymer surface. Samples treated with an etching plasma containing oxygen are partially sealing, since such etching gases create and eliminate the sealing layer at the same time. On the other hand, inert gases, such as nitrogen, densify the surface completely. The formation of a top layer rich in carbon and nitrogen has been reported for polymer surface treated with nitrogen [163]. Unfortunately, these sealed polymer films seem to loose their sealing property when exposed to elevated temperature (>300°C) [27].

Another plasma sealing method reported in the literature makes use of an etch by-product [143, 164]. A fluorocarbon polymer layer is generally deposited at the low-*k* sidewall during the patterning using C_xF_y plasma species, which has been shown to protect the low-*k* bulk against plasma damage [165, 166]. Unfortunately, this fluorocarbon layer will be removed relatively easily during resist stripping [166] and/or wet cleaning [164]. Therefore, Ohtake *et al.* [164] proposed using a plasma containing C_4F_8 and N_2, which modifies the plasma-etched surface to a FCN layer. These layers were found to block the copper diffusion into the low-*k* films.

In summary, the proper choice of plasma energy and composition can establish pore sealing. It will however always be a balancing act between pore sealing and plasma damage. A general trend to keep in mind is the more porous a low-*k* material is, the more difficult it will be to seal without extensive damage.

Alternative pore sealing techniques

Due to the tradeoffs for both pore sealing techniques mentioned above, different pore sealing techniques have been explored. Alternative integration schemes for porous low-*k* have been proposed, in which the porosity in the material will be created at a later stage [167–169]. The porosity could either be created after etch (post-etch burn-out: PEBO) or after CMP (post-CMP burn-out: PCBO). The schematics of both integration schemes are compared with the conventional flow in Figure 5.23. It should however be noted that the PCBO approach is only compatible with a permeable top hard mask, which allows the volatile compounds to pass through it. Moreover, in the PEBO integration scheme it is assumed that the etch plasma modifies the porogens at the sidewall of the damascene structure such that pores cannot be created during cure. Finally, it should be mentioned that porosity creation later on in the process flow requires process temperatures below the decomposition temperature of the porogen.

In both approaches, the sidewall roughness can be considerably reduced and the barrier integrity improved compared with the conventional process. The improved barrier–dielectric interface of the PEBO structures translates into considerable gains in terms of reliability and enables further downscaling of the metallic barrier [170]. A possible drawback of this approach might be the considerable material shrinkage during burn-out (~10%), which could cause dielectric failure due to high stress build-up.

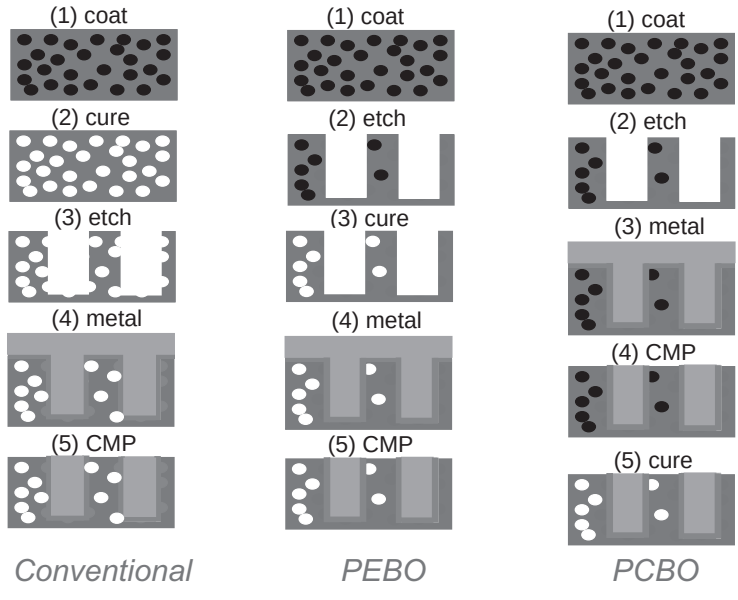

Figure 5.23 Schematic representation of three different integration schemes, in which the porosity is created either after coating (conventional scheme), after etch (post-etch burn-out (PEBO) scheme) or after CMP (post-CMP burn-out (PCBO) scheme)

5.3.5 Processing damage to low-*k* films

The preservation of the electrical properties of low-*k* dielectrics throughout integration in damascene processes is a challenging task, since low-*k* dielectric films are extremely susceptible to physical and chemical damage during interconnects processing. Their low density (as low as 1 g/cm^3 for *k* approaching 2.0) translates into low stopping power to physical bombardment of ion species in plasma environments. Consequently, a rather large depth of damage can be expected for such films (hundreds of nanometers). Also, the increasing amount of porous volume in the dielectric films typically leads to mesoporosity and an interconnected pore structure [117]. Typical molecular sizes used for chemical processes are smaller than pore sizes of mesoporous dielectrics. The hindrance for penetration of such molecules into the pore network is thus generally low, and chemically active species can move with high rate (thousands of micrometers per second) in the bulk of dielectric films.

Both physical and chemical damage will typically lead to an increase of the *k* value and/or electrical performance (leakage current and breakdown) of the dielectric material through film densification, introduction of dangling bonds/electrical defects and incorporation of polar species (mainly –OH bonds). Processing damage is thus a major concern for advanced technology nodes, where feature sizes are scaling dramatically and dielectrics with *k* value approaching 2.0 (porosity close to 50%) are required [16]. Plasma-based processes, combining both physical and chemical actions, are omnipresent in semiconductor processing and represent a key challenge in terms of damage induced to low-*k* dielectrics.

Damaging processes to low-*k* dielectrics

Virtually all damascene processing steps are possible sources of damage/modification of low-*k* dielectrics, from subsequent film depositions on the low-*k* materials to dielectric patterning (dry etch and dry photoresist strip or ash) and cleaning processes. An extremely careful choice of the process conditions is required to minimize the damage extent.

Damage from low-k *capping.* Film deposition onto low-*k* dielectrics poses the challenges of ion bombardment (for physical deposition processes), reactant species diffusion in the low-*k* film (for chemical deposition processes) and both of them for plasma-enhanced chemical vapour depositions (PECVD). Due to extensive precursor diffusion in the porous films, the material properties of a mesoporous films can be considerably altered after capping by PECVD layers. The chosen precursor gases and deposition conditions play a critical role.

The effect of precursor gases and deposition conditions was studied by Iacopi *et al.* extensively by depositing thin SiO_2 cap layers onto a porous HSQ material with SiH_4 and N_2O precursors[171]. Depositions with low (~15) and high (~30) N_2O/SiH_4 gas flow ratios were compared, to vary the concentration of oxidizing agents. The FTIR spectra of low-*k* films after capping with 20-nm-thick SiO_2 depositions with lower and higher N_2O partial flow are shown in Figure 5.24, curves b) and c), respectively. Compared with the spectrum of an uncapped film (Figure 5.24, curve a)), spectrum b) does not show significant loss of Si–H bonds (peak at 2250 cm^{-1}). There are clear indications for oxidation of the HSQ film during SiO_2 deposition with higher N_2O/SiH_4 ratio. Figure 5.24, spectrum c) shows about 60% reduction in intensity for the Si–H peak, and the presence of moisture absorption is also detected (region around 3500 cm^{-1}). The film becomes highly hydrophilic. Note that in the case of cap deposition with lower partial N_2O flow, still some slow moisture uptake was observed with FTIR in the low-*k* films during storage.

In contrast to the deposition of SiO_2 cap layers, the deposition of a SiC capping has a beneficial effect on the film properties [171]. FTIR measurements after SiC capping show the presence of more Si–H bonds than in the initial conditions plus also a significant amount of carbon containing bonds ($C–H_x$) which were initially not present in the mesoporous low-*k* film. Both these kinds of bond can help to enhance the hydrophobic behavior of the stack, like observed through long-term FTIR and electrical capacitance monitoring.

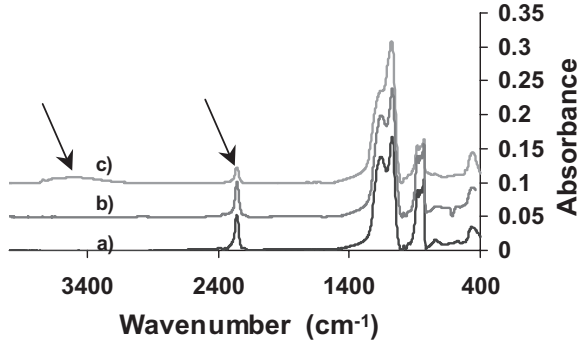

Figure 5.24 FTIR spectra of porous HSQ films: (a) initial (uncapped); and underneath a SiO_2 capping layer deposited with (b) low and (c) high partial N_2O flow. (Courtesy of IMEC)

Damage from patterning processes. Advanced patterning in damascene technology strongly relies on the use of plasma-based processes for dielectric etch and photo-resist removal (i.e., ash). Typically, fluorine or chlorine compounds are used for etching inorganic films, while highly oxidizing or reducing chemistries are used for the removal of organic-based dielectrics and photoresists. The chemical action is efficient and selective, but lacks directionality, a fundamental requirement for deep sub-micrometer patterning. Directionality is improved by using 'ion-assisted' etching, where the ion bombardment energy is used to trigger the etch reaction and desorption of the etch products from the surface.

With the appropriate choice of plasma power, the densification can be confined into a few nanometers of the top layers of microporous dielectric films [172]. In this way, film properties, such as *k* value, are not dramatically affected. The newly formed densified 'skin' layer can be even beneficial (as discussed under 'plasma sealing' in Section 5.3.4), since it can act as a protection or barrier to further damage to the film bulk [158, 172]. This is however not the case for mesoporous dielectric films.

To illustrate the difference between microporous and mesoporous films, a blanket microporous SiOC film (7% porosity) and a mesoporous SiOC film (~40% porosity) were exposed to plasma processes based on inert (He) and oxidizing (N_2O) gases, at a temperature of 350°C and comparable conditions of plasma power and chamber pressure. The compositional depth profiles of these treated films as measured by TOF-SIMS are shown in Figure 5.25 for

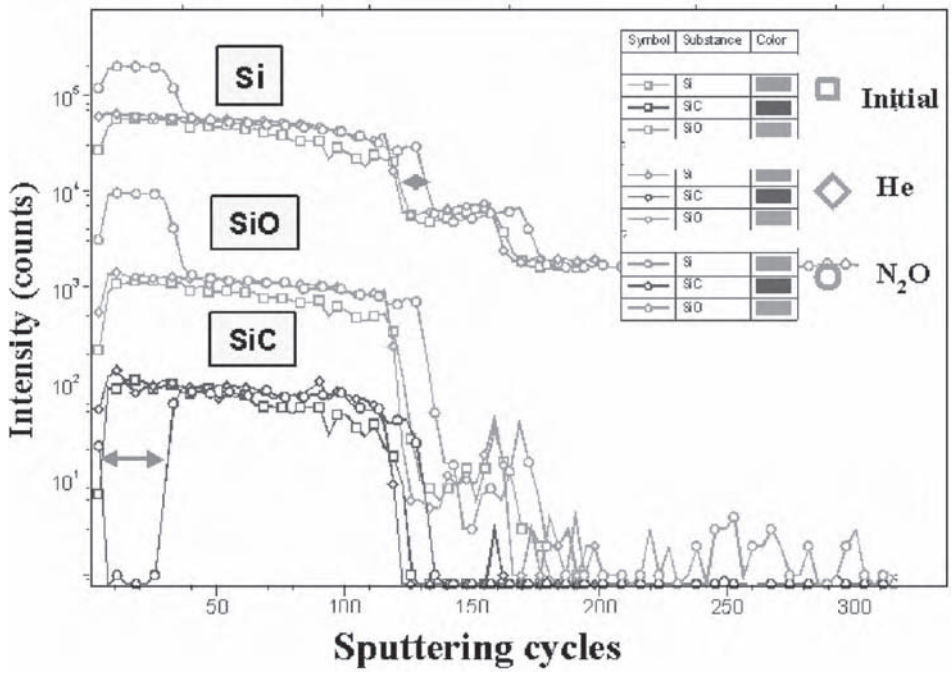

Figure 5.25 Molecule fragments detected by ToF-SIMS during compositional depth profiling on plasma treated microporous SiOC-based films. No significant change is found after exposure to He plasma, and a C-depleted region on top of the film is found after exposure to the oxidizing plasma. (Courtesy of IMEC)

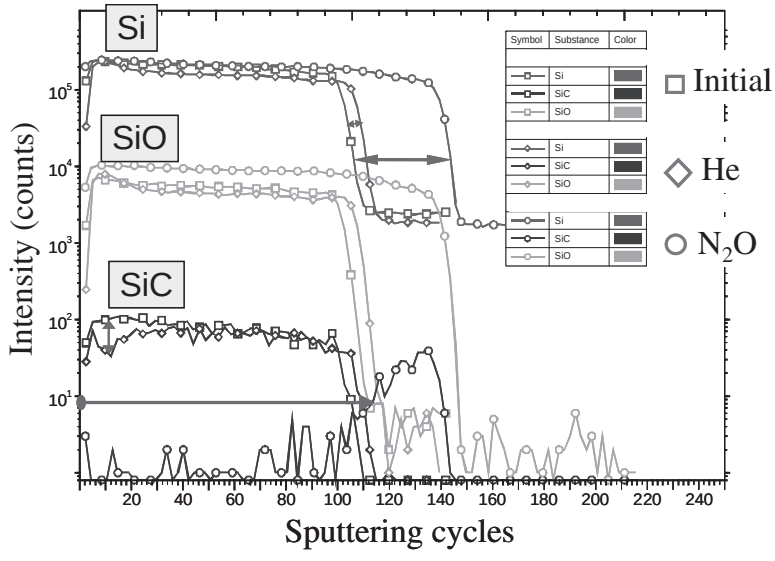

Figure 5.26 Molecule fragments detected by TOF-SIMS during compositional depth profiling on plasma-treated mesoporous SiOC-based films. Minor C depletion and densification is found after exposure to He plasma, while almost complete C depletion and major densification of the film is found after exposure to the oxidizing plasma. (Courtesy of IMEC)

the microporous and in Figure 5.26 for the mesoporous dielectrics. Counts for the detected fragments are reported versus the number of sputtering cycles, which can be taken as an indication of the sputter depth. In the case of the microporous film treated with He plasma the SIMS profiles perfectly overlap with the reference samples, which indicates that the bulk of the material is not affected at all by this treatment. On the other hand, the film treated with N_2O plasma appears composed of two distinct layers, showing a rather sharp transition. The top layer appears oxide-like (completely depleted in C), while the bottom one appears similar to the pristine film composition (see Figure 5.25). The modified layer is probably denser than the pristine film and its thickness can be roughly estimated as about 50 nm (taking into account the densification effect).

The mesoporous film treated with N_2O plasma is drastically affected in the entire bulk of the sample (see Figure 5.26). The sputtering time needed to get to the bottom of the layer is about 30% longer compared with the reference film. Ellipsometry measurements indicated that the film is strongly densified after plasma treatment. It can also be seen that the N_2O treated film is completely depleted in C (profile drops to noise levels) by the plasma process. The Si–C profile is rather graded, indicating that the damage reaches throughout the entire thickness of the film. On the contrary, the mesoporous film with He plasma treatment shows minor densification and compositional change (see Figure 5.25). The Si–C profile indicates minor C depletion confined to the top layers of the film (roughly the first 50 nm).

The results above indicate that exposure to inert plasmas (only *physical* action from ion bombardment) of microporous, low porosity dielectric films does not lead to bulk film modification (it can still lead to surface damage, though). Exposure of inert plasmas to

mesoporous, high-porosity films can lead to few tens of nanometers extent of modification near the top surface, due to low film density; plasma power and mass of the inert element are the parameters determining the extent of damage. On the contrary, exposure to oxidizing plasmas (physical plus *chemical* action) of microporous films can damage several tens of nanometers of material and in mesoporous films in the order of several hundreds of nanometers.

Overall, mesoporous, high-porosity materials appear to be significantly more sensitive to plasma exposure than low-porosity, microporous dielectrics. The physical damage can reach deeper because of the low density of high-porosity films, and the chemical damage can reach up to hundreds nanometers in the films due to the diffusion of reactant species through the mesoporous network. The extent of chemical action would be expected to show a difference between mesoporous materials with meso- and micro-connections, but so far no clear data showing such a comparison are available.

Sidewall damage. In damascene processes, and in particular during patterning, the top surface of low-*k* films can be protected from plasma damage by a protecting hard mask layer. However, the dielectric film is still exposed to the plasmas through the trenches/recesses sidewalls, resulting in sidewall damage [109, 165, 166, 173, 174]. The effects of the physical plasma damage on the film are considerably reduced in a highly directional (anisotropic) plasma condition. Therefore, in this case the biggest concern is the chemical action, and in particular the extent of lateral diffusion of the reactive species from the sidewalls to the bulk film.

The plasma process for resist removal is expected to be more critical than etch, since the sidewalls are not yet completely opened during the dielectric etch, and also because the sidewalls are usually protected by a thin film which is the result of polymerization during the etch process [165, 166]. This thin polymer film is subsequently removed during resist ash, so conditions of plasma pressure and temperature during this process become critical for the extent of diffusion of the active species.

The control on the extent of sidewall damage is critical for narrow spaced metal lines, since for sub-100-nm spacings, even a few nanometers damage on both sidewalls would lead to a significant percentage of damaged interline dielectric. The latter can be demonstrated by capacitance measurements on interdigitated lines embedded in different dielectrics [175]. The experimental interline capacitance obtained for different dielectric spacings is compared with the values computed through an electrostatic field solver assuming the dielectric preserved its pristine *k* value. For the meander forks embedded in SiO_2, a very good agreement was found between experimental and computed values in the whole spacing range investigated (Figure 5.27). However, for the SiOC : 1 and SiOC : 2 films the experimental values tend to be higher than the computed ones for the smallest spaced structures. In particular, while for the SiOC : 1 material considerable deviation is observed only for structures with spacing below 100 nm, for the SiOC : 2 dielectric there is substantial deviation already below 150 nm spacing. From this analysis it can be concluded that the effective *k* value of both low-*k* dielectrics once integrated is higher than their pristine value, and that this effect is more pronounced for the SiOC : 2. The capacitance data can also be analyzed more in detail using the 'electrical equivalent damage' model [176], which shows the presence of only sidewall damage for the SiOC : 1 and the combination of sidewall and top damage in the case of the SiOC : 2. EFTEM compositional profiling only indicates the presence of an approximately 20-nm-wide carbon-depleted region at the sidewall for both integrated low-*k* films (see SiOC : 1 in Figure 5.28).

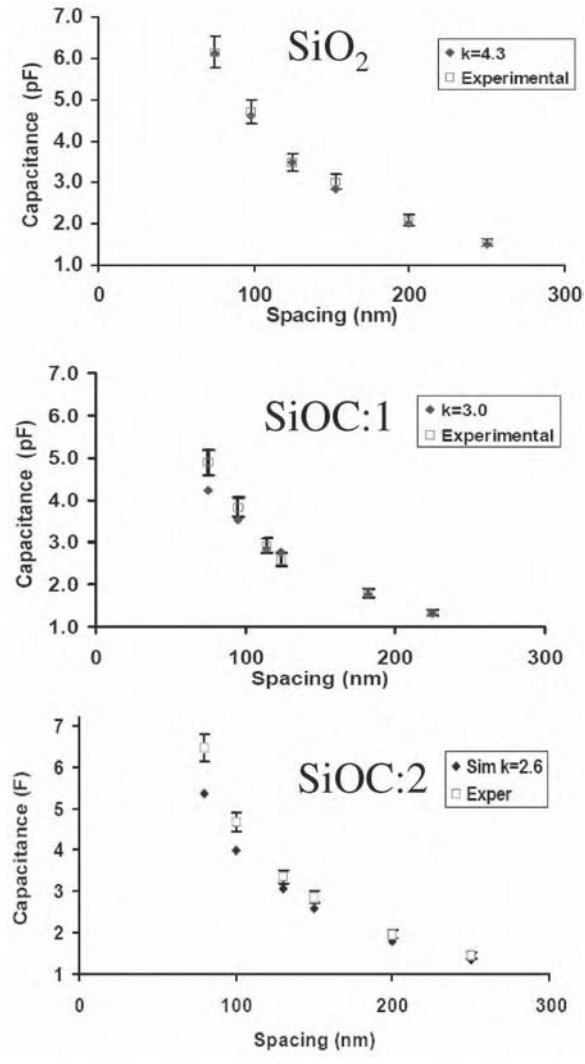

Figure 5.27 Experimental interline capacitance data are plotted against values computed by assuming a pristine k value for the particular dielectric under study. The capacitance measurements were obtained on interdigitated lines embedded in SiO_2 and two SiOC dielectrics with as-deposited k value of 3.0 and 2.6 (SiOC : 1 and SiOC : 2, with 7% and 16% microporosity, respectively). (Courtesy of IMEC)

One type of physical analysis alone is typically not sufficient to characterize the actual modification of the dielectrics and does not necessarily show a correct correlation to the consequences in terms of electrical behavior. In this context, the development of a high-sensitivity physical/chemical metrology for dielectric damage detection and its correlation to electrical performance is currently a main focus [177, 178]. The 'electrical equivalent damage' model [176] is a valid methodology for assessing process-induced dielectric

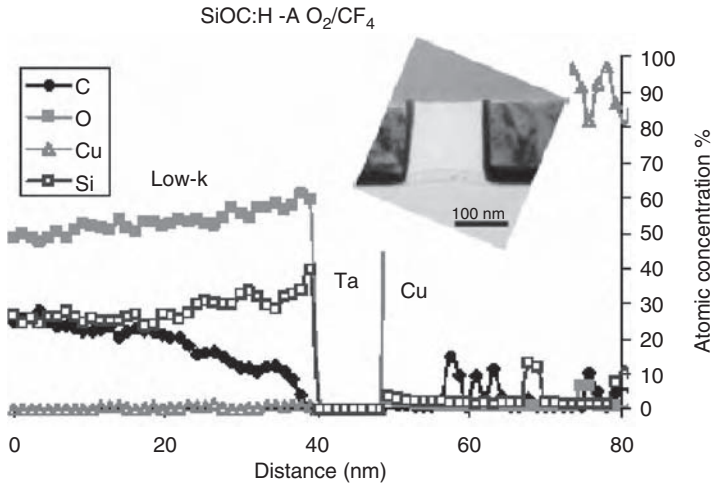

Figure 5.28 EFTEM analysis of the sidewalls of a 'dense' SiOC material (7% microporosity with $k = 3.0$) showing the carbon, oxygen, copper and silicon profiles. (Courtesy of IMEC)

damage. It allows the distinction between top and sidewall modification and the electrical quantification of the extent of damage.

Dealing with processing damage during low-*k* integration

Processing damage (both on top and sidewall) of low-*k* dielectrics is a major concern for advanced technology nodes. Since resist ashing is expected to be the most critical process step for low-*k* materials, most attempts to minimize the plasma damage are focused on new ashing processes and/or new integration schemes. H_2/He ashing seems to be one of the most promising resist removal processes for post-etch wafer cleaning compatible with SiOC films [166, 179–181]. The physical damage caused by these light ions is reduced, however the chemical damage can still be extensive. It should also be mentioned that this process is quite inefficient in resist removal and it should therefore be operated at elevated temperatures (to reduce the ash-time and consequently the plasma damage) [179].

Other researchers focus on shifting the resist-removal process to an earlier point in the integration flow, consequently the low-*k* will not be exposed to the ash-plasma. Most of these approaches involve the use of multiple CVD hard masks [40, 46] or metal hard masks [86, 87, 182, 183]. The resist patterns are transferred into the hard mask layers. After removing the resist, the low-*k* is patterned using the hard mask. The remainder of the hard masks on the dielectric layer after etch will be removed during the CMP process.

All these hard mask approaches assume that the ash plasma causes the major part of the sidewall damage. However, as illustrated in Figure 5.29, the damage by the etch-plasma should not be neglected. In this figure, a cross-section picture is shown of high-aspect-ratio vias patterned in a porous SiOC material. The carbon-depleted sidewall region has been decorated by a diluted HF treatment, which selectively etches SiO_2. The plasma damage caused by the oxygen-free via etch cannot be neglected, since a large part of the sidewall

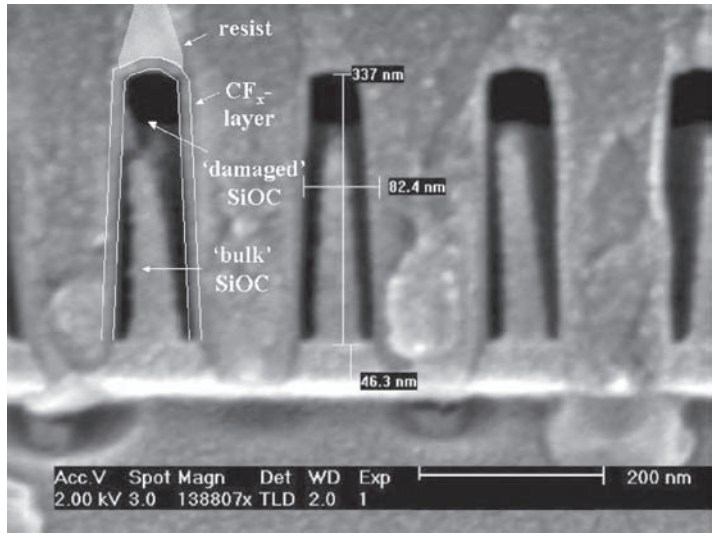

Figure 5.29 Cross-section SEM image of high-aspect-ratio vias patterned in a porous SiOC material before resist-ashing. The patterned structures were filled with a planarizing polymer, after which the plasma-damaged sidewall layer could be stained by a diluted HF etch. (Courtesy of Philips Research, Leuven)

has been etched. In addition, a thin fluorine-containing polymer layer was found to be present at the sidewalls. In contrast to what was expected, this passivation layer was not able to stop the plasma damage.

Since it seems to be extremely difficult to prevent plasma damage, the possibility of repairing the plasma damage in organosilicate or silsesquioxane films is being investigated as well. Two different repair processes can be distinguished, namely hydrogen plasma post-treatments or post-processing chemical substitution (silylation) of Si–OH groups with Si–CH_3 or other low polarizability groups.

The first technique makes use of the fact that hydrogen plasma treatments convert the dangling bonds, leading to the repair of bonds damaged by the patterning process [184, 185]. The combination of a pre- and post-patterning plasma treatment was shown to be even more effective against sequential damage caused by etching plasmas [184]. It should however be noted that the success of this technique is questionable, since hydrogen plasmas are known to remove CH_3 fractions from the films, decreases the amounts of cage-type Si–O bonds, and densifies the films, thus increasing the dielectric constants [186].

The second restoration technique involves the use of silylating agents, such as trimethylchlorosilane (TMCS) [187] or hexamethyldisilazane (HMDS) [187–190, 191]. The hydrophilic Si–OH groups are replaced with hydrophobic Si–O–$Si(CH_3)_3$. The change of hydrophobicity reduces the moisture uptake and consequently restores the k value to a large extent. However, the main issue concerning this approach is the efficiency of the proposed rather large molecules in obtaining a complete conversion of the silanol groups at the damage surface in the first place, and the possibility for those molecules to reach deeper into the damaged low-k volume (due to the presence of a densified surface layer). In order to improve the delivery efficiency, the use of carrier gases in supercritical phase is currently

being investigated, even though the hindrance of the active molecules will remain a limiting factor.

In another attempt to circumvent plasma damage, some authors [192, 193] proposed hybrid integration schemes. In these approaches, the SiOC material at trench level is replaced with a porous aromatic polymer (i.e., porous SiLK) in order to prevent plasma damage at these levels. Preliminary capacitance measurements [194] suggest however that the porous organic polymers are also prone to plasma damage (accompanied by a significant *k* value increase), which would eliminate the advantage of the hybrid integration approaches.

More recently, researchers demonstrated successful integration of ultra-low-*k* materials using a gap-fill-based integration scheme [195]. In this approach, a reliable metal level is fabricated in a dense organic or inorganic material. Following the metal CMP, the bulk dielectric is selectively etched out between the metal lines. After the etch-back, any desired low-*k* material can be used for (over) filling the gaps. However, in this scheme it is necessary that the deposited low-*k* fills the narrow gaps and withstands direct CMP. This expensive approach also shows the desperate need for a breakthrough in the 'red brick wall' in the back-end-of-line part of the ITRS roadmap [16].

5.3.6 CMP compatibility

Chemical mechanical planarization (CMP) of copper and barrier metal is key to fabricate Cu damascene interconnects. The introduction of low-*k* materials has placed additional requirements to the CMP process: it must have low friction between the wafer and the polishing pad [196], and must be chemically compatible with the low-*k* materials. The low friction requirement comes from the fact that low-*k* materials are generally weak both in cohesive strength as well as adhesive strength to conventional dielectric materials, which are needed in the integration stack for various purposes [197]. In Figure 5.30 a few examples

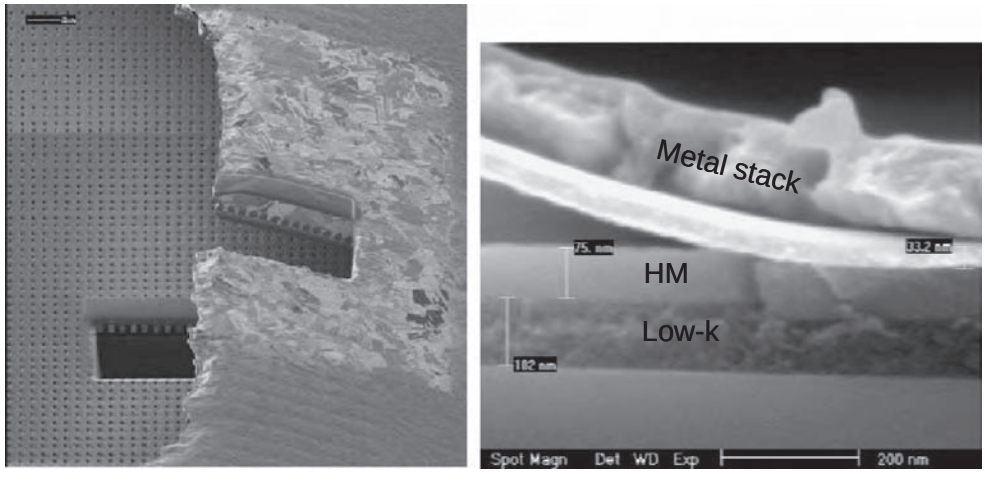

Figure 5.30 Cross-sectional SEM images illustrating examples of delamination after CMP; (left) adhesion loss between an embedded etch-stop layer and the via-electric (right) adhesion loss between the metallic barrier and the top hard mask. (Courtesy of Philips Research, Leuven)

of delamination issues obtained during CMP are shown. In most cases, the delamination is due to a lack of adhesion between the different films, rather than a loss of cohesion in the low-*k* dielectric itself. It has been reported that delamination usually starts at the wafer edge and on low pattern density areas [198, 199]. Dummy metal structures incorporated in the large open areas can therefore minimize the delamination probability [200].

A low-friction CMP process would minimize the risk of creating cracks in the low-*k* stack and of delamination, subsequently preserving the electrical yield of Cu/low-*k* structures [201]. The friction force in a CMP process by definition is the force that resists the relative motion of the wafer and the polishing pad in the slurry environment. This force, if it exceeds cohesive or adhesive strength of the low-*k* materials will result in cracks and eventually delamination. The friction force is a function of a variety of CMP process parameters. According to the Amontons–Coulomb law of friction, the friction force is directly proportional to the applied load, i.e., polishing pressure in the CMP process [202, 203]. In addition, the friction force also strongly depends on the morphology and properties of the polishing pad, and on the composition of the slurry.

The friction force in a CMP process can be measured by the PadProbe® real-time [204] or by a load cell attached to the wafer carrier [205]. It can also be calculated based on the changes in the current of the motor that drives the table on which the polishing pad is attached [199], or based on the increase in polishing pad temperature during the CMP process [206]. It has been observed that under the same polishing pressure and slurry environment, a conventional polishing pad yielded more friction compared with a fixed abrasive pad. SEM images of the surface of a conventional polishing pad and that of a fixed abrasive pad are shown in Figure 5.31. Differences in the pad surface topographies and in the mechanical properties of the pad top layers are the root cause of the difference in the friction force.

The slurry composition plays an important role in determining the friction force in a CMP process. The chemicals in the slurry modify the properties of the wafer and the pad surfaces and have an effect on the friction. In addition, the type and the concentration of abrasive particles in the slurry also have an impact on the friction force. Figure 5.32 represents the normalized friction force caused by different commercial and experimental slurries under identical polishing condition. The friction force caused by polishing with deionized (DI) water is the reference point. From this graph, it can be seen that DI water

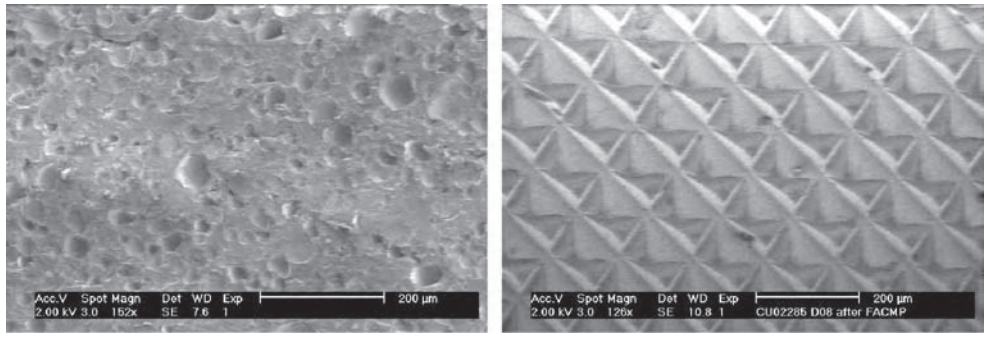
Acc.V Spot Magn Det WD Exp 200 µm
2.00 kV 3.0 152x SE 7.6 1
Acc.V Spot Magn Det WD Exp 200 µm
2.00 kV 3.0 126x SE 10.8 1 CU02285 D08 after FACMP

Figure 5.31 SEM images of a conventional (left) and a fixed abrasive (right) polishing pad. (Courtesy of Philips Research, Leuven)

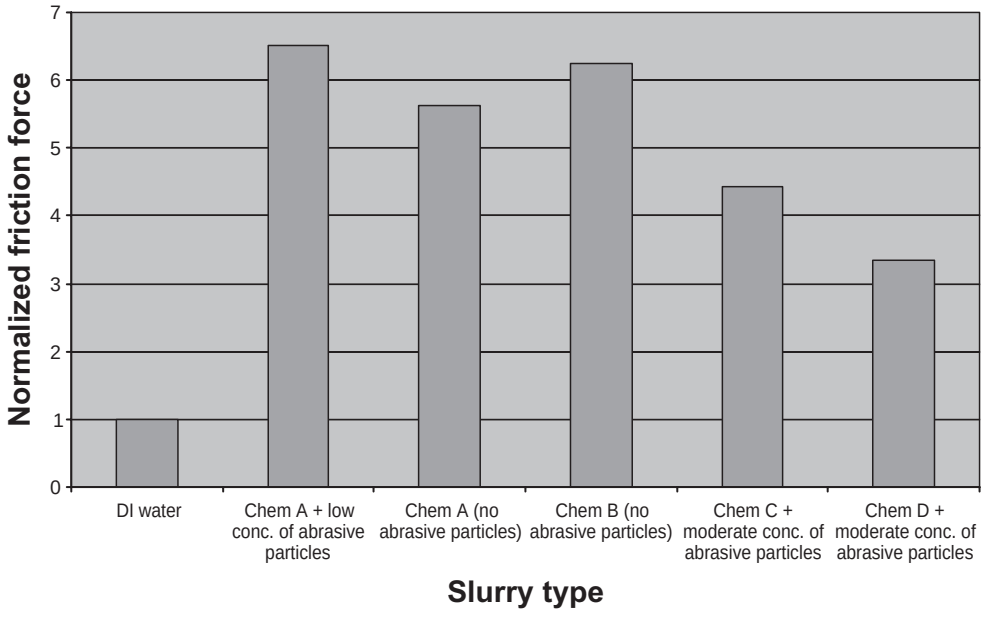

Figure 5.32 Normalized friction forces results by different slurries under the same polishing condition. (Courtesy of Philips Research, Leuven)

is the best lubricant in term of friction reduction. As soon as chemicals are introduced into the slurry (without abrasive particles) the friction force is increased dramatically. Adding abrasive particles into the slurry changes the friction force. At the very low abrasive particles concentration, it is observed that the friction force is increased. However, at a moderate abrasive particle concentration, the friction force is reduced. It is believed that the rolling of abrasive particles contributes to the lowering of the friction force.

The polishing slurry does not only influence the friction in a CMP process, it also has an impact on the speed of crack growth within a low-*k* stack, once the cracks have been generated. It has been shown experimentally that, depending on the nature of the slurry, the growth of cracks in a low-*k* stack can either be enhanced or minimized [207]. And in addition, penetration of the slurry into the low-*k* materials is yet another concern of the CMP process for low-*k* material. It has been shown that the slurry can penetrate into the low-*k* materials, pushing up the dielectric constant of the low-*k* materials [208].

Several approaches are being studied for making CMP process compatible with low-*k* materials. The simplest route is to operate the conventional CMP process at a lower down-force. Currently the preferred down-force in a conventional CMP process for low-*k* materials is between 1 and 1.5 psi. However, for a conventional CMP process, it is difficult to further reduce the polishing pressure because the removal rate of material will be very low and consequently the throughput low. In the past few years, a number of nonconventional CMP such as abrasive free CMP [209], hybrid CMP process in which fixed abrasive CMP is coupled with abrasive free CMP [210] and electrochemical mechanical polishing (ECMP) [211–215] have been proposed. ECMP appears to be the most attractive option of all for it can be operated at pressure below 0.5 psi, while still having a good planarization and high removal rate.

5.4 LOW-*k* RELIABILITY CHALLENGES

As discussed above, the continuous downscaling of chip dimensions in combination with the introduction of porous low-*k* materials has increased the number of integration challenges tremendously. In addition, the inferior properties of porous low-*k* materials compared with their dense equivalents are also thought to induce numerous reliability issues, which are in addition to the ones caused by the continuous downscaling of metal lines and dielectric spacings [18]. All of this together has an enormous impact on the reliability of the end product.

In the realm of reliability, mechanical integrity has already taken center stage for low-*k* integration at the 90 nm node and will become an area of increased vulnerability with the insertion of porous low-*k* materials at the 65 nm node and beyond, due to the decreasing mechanical strength of these materials with increasing porosity content. Interfacial adhesion and cohesive strength, and linked with that hardness, modulus, cracking threshold and intrinsic stress, are the key film properties to target successful copper/low-*k* integration and assembly. Due to the introduction of porosity into the low-*k* matrix, most of these film properties will deteriorate compared with their dense equivalents. These are exactly the properties that determine whether a material can withstand the stresses of CMP, can provide sufficient strength to be used in multiple interconnect levels, and can withstand packaging. Therefore, low-*k* packaging requires a three-fold approach: stack optimization for bulk and interface properties; design rule modification for bond pads, edge seals, etc.; and tailoring of the assembly process and materials for low-*k* compatibility [216, 217].

Dielectric reliability was only a concern for gate dielectrics; however, with the continuous decrease of intermetal spaces, together with the introduction of porous low-*k* materials and thinning down the metallic barrier thickness, the leakage and breakdown might become a serious issue in the interconnect as well. It will be an enormous challenge to get the dielectric reliability of porous dielectrics to a comparable level to that of dense equivalents. Pore sealing might become key to obtain acceptable reliability performance, although the effect on the *k* value should be kept minimal.

However, not in all case the high dielectric leakage and low breakdown strength is due to the introduction of porous low-*k* materials in the dielectric stack, but rather due to the surface condition after metal CMP. This interface seems also to be the predominant failure site for electromigration [65]. Therefore, the electromigration failure mode has probably more to do with the copper surface than with the presence of a low-*k* material in the dielectric stack. The composition of the dielectric barrier [218] in combination with pretreatments [219] (discussed in Section 5.2.2) can strongly enhance the reliability due to an improved adhesion. Alternative integration solutions, such as self-aligned metallic barriers, show extremely improved electromigration performance [220] and therefore potential to replace the conventional dielectric barriers (see paragraph 2.2.3.1).

Electromigration is known to be less predominant for copper than for aluminum. However, some authors [221] claim that electromigration behavior of copper embedded in low-*k* materials will deteriorate due to a reduced resistance against cracking (cohesive failures). And for short copper lines embedded in materials of low elastic modulus shorter electromigration lifetimes could be the result of a lower back-flow stress on the surrounding material [65, 222]. In addition, the poor thermal conductivity of low-*k* materials can have a significant impact of the metal line's current carrying capability. The upper level wide lines might not live up to their expectations for high-current applications, since the Joule heating can limit the maximum allowed current densities in these lines [223].

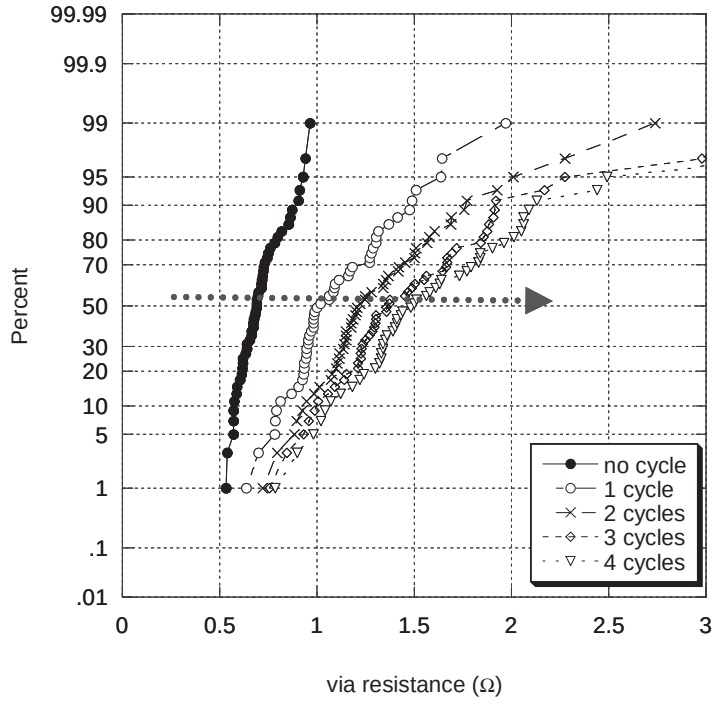

Figure 5.33 Via resistance (for a 200 nm Kelvin; a single via-structure) as a function of a different number of thermal cycles (i.e., 30 min at 400°C) for a two-metal-level stack, with porous SiLK as dielectric

Finally, most low-*k* materials (especially the organic polymers, such as SiLK^{TM}) have a higher thermal expansion coefficient (CTE) compared with the traditional 'oxides'. The latter could lead to a higher stress at the bottom of the copper via, which on its turn leads to undesirable increasing via resistances upon thermal cycling [83, 224], as illustrated in Figure 5.33. By providing a good via bottom surface, it is possible to survive thermal cycling without any loss of via yield using low-*k* materials with a high CTE [83].

As was discussed shortly in this chapter, some of these reliability challenges can be dealt by continuous innovation of materials, processes and integration approaches. It is however also well possible that different solutions, such as air gaps [225–229] and low-*k* back-fill [195], might be scalable options for future interconnects. Additionally, it might also be considered to remove speed-sensitive paths from minimum-pitch portions of circuits, whenever possible, in order to profit better from the advantages of copper and low-*k* materials, without running into their associated critical areas.

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6 ONO Structures and Oxynitrides in Modern Microelectronics: Material Science, Characterization and Application

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6.1 INTRODUCTION

Silicon oxide, silicon nitride and oxynitride films (SiO_xN_y), as well as dielectric stacks composed of these films, have been widely used in the microelectronic industry since the early 1960s. These materials have dielectric constants above 3.8–3.9 (thermal silicon dioxide) and up to 7–7.5 (silicon nitride). Until the present, silicon dioxide obtained by thermal oxidation of silicon is the primary gate dielectric and one of the most important technological layers in semiconductor processing. It ensures low density of traps at the Si/SiO_2 interface, excellent insulating characteristics, immunity to electrical stresses in device operation and high-temperature stability in fabrication processes. CVD silicon oxides, nitrides and oxynitrides have been also widely employed in semiconductor processing and in semiconductor devices. They serve as electrical isolation, sidewall spacers, capacitor dielectrics, trapping media of memory elements and passivation layers. Nitrides and oxynitrides are used as hard masks, diffusion barriers, etch stops and protection layers. For example, a layer of silicon nitride prevents oxidation of the underlying silicon in the LOCOS (local oxidation) processes.

Compared with silicon oxide, dense silicon nitride films have a solid structure without microchannels. This allows one to suppress diffusion of oxygen, even at temperatures above 1000°C. Silicon nitrides and oxynitrides can be fabricated with a very high (10^{19}–$10^{20}\,cm^{-3}$) density of electron and hole traps and, on the contrary, almost free of traps. This allows one to use the material both as gate dielectrics and in the memory devices.

Memory transistors known as MNOS (metal–nitride–oxide–semiconductor) and SONOS (semiconductor–oxide–nitride–oxide–semiconductor) employing a ~20 Å bottom oxide (BOX) use trapping in silicon nitride for information storage and direct tunneling of electrons and holes from silicon into the nitride for programing and erasing. Stacked ON or ONO (oxide–nitride–oxide) structures have been also successfully employed as the dielectric between the floating and control gates in EEPROM (electrically erasable programmable read-only memory) devices with charge storage in the polysilicon floating gate and as the dielectric of DRAM (dynamic random access memory) and MIM (metal–insulator–metal) capacitors. The stacked structures have much lower defect densities and suppressed leakages due to charge trapping in the nitride layer, compared with individual CVD films.

Interest in silicon nitrides and oxynitrides increased strongly in the last decade due to their implementation as gate oxides and novel ONO stacks in deep sub-micrometer technologies. Introduction of nitrogen into the thermally grown silicon dioxide films or direct growth of oxynitride films allows one to obtain gate dielectrics with the same specific capacitance, but with larger thickness and enhanced reliability. Also, boron penetration from the polysilicon through the scaled-down gate oxynitrides is strongly suppressed if the nitrogen concentration is high enough. Oxynitrides were also found to be advantageous for application as the trapping media in ONO memories, showing better retention properties.

Several reasons exist why the nitride memory technology with more than 30 years history is being revived now. The first reason is the availability of advanced methods of dielectric formation. In contrast to the MNOS and SONOS devices of previous generations, the thickness of the bottom tunnel oxide and its uniformity over the wafer is now much better controlled. New technologies for high-quality ultrathin nitride (oxynitride) deposition and TOX (top oxide) formation ensure high repeatability of the parameters and control of ONO trapping properties. The total thickness of the ONO memory stack is significantly decreased, making it possible to scale memory transistor channel lengths down to 0.02 μm [1]. New

promising SONOS technologies (NROM, nitride read-only memories [2]) have been developed and are rapidly spreading in the nonvolatile semiconductor memory market. Novel devices use 'thick' (>30 Å) BOX compared with traditional SONOS, 40–60 Å nitride (oxynitride) and 50–150 Å top oxide and employ local storage of charges in nitride. The new memories are free of the main limitation of the previous SONOS generations (a limited retention and high read disturb), have high yield, and are easily integrated into the core CMOS (complementary metal–oxide–semiconductor) process flows. They are advantageous over polysilicon floating-gate EEPROMs which are reaching their scaling limit due to reliability problems with BOX thinner than 70 Å, and are easier for building embedded process flows (fewer additional masks). New SONOS technologies stimulate the review of the basic properties of silicon nitrides and oxynitrides. New physical phenomena, such as lateral charge migration in the nitride layer of ONO and space-shifted trapping of electrons and holes in the programing/erasing operations raise additional questions related to the nature and parameters of trapping centers. Chemical composition and defect structure of advanced oxides, nitrides and oxynitrides as well as their geometry in the stacked configurations must be linked with the operation and reliability parameters of corresponding devices.

This chapter is organized in the following way: first, we describe state of the art oxynitride and silicon nitride fabrication techniques and the basic properties of these materials. We start with traditional deposition techniques (still used in the technology of advanced ONO stacks), offer a short review of oxynitrides for CMOS gate application, and focus on ONO stacks for advanced memories. A detailed analysis of ONO composition is provided with emphasis on correlation of the chemical content and processing technology, with parameters important for device operation. The next two sections are devoted to the atomic structure of silicon oxynitrides and the chemical nature of traps. Models of chemical bonding and correlation of the atomic structure of defects with material and device characteristics are presented, including discussions on the electronic structure of traps responsible for charge storage in memory devices. This is followed by a section on charge transport in ONO. Problems related to 'vertical' charge transport in traditional SONOS memory devices and 'lateral' charge migration in local storage SONOS are discussed. Charge transport issues important for operation of SONOS devices and engineering of ONO materials are emphasized. The last sections describe ONO applications in novel semiconductor devices. The results presented in previous sections are linked to the performance and reliability of advanced SONOS memories with thin BOX and NROM devices. Implementation of high-k material in ONO is discussed. Open material science questions important for engineering of devices with ONO dielectrics are formulated.

6.2 TECHNOLOGY AND BASIC PROPERTIES OF SILICON NITRIDE/OXYNITRIDE FILMS AND ONO STACKS

Silicon nitride and silicon oxynitride technology has advanced greatly in the last decade. State-of-the-art gate dielectrics in 0.09–0.18 μm CMOS process flows are oxynitrides with different amounts and spatial distributions of nitrogen and physical thickness below 30 Å [3, 4]. ONO stacks for memory applications contain silicon nitride and/or oxynitride as a trapping layer [5, 6]. At the same time, special ('trap-free') types of 'pure' silicon nitride were shown to be suitable as gate dielectrics for future integrated circuit generations [7, 8]. These nitrides can also serve as substitutes of bottom oxides in ONO memory structures

[9]. We use the term ONO for the stacked dielectric in memory devices; sometimes this abbreviation also stands for oxide–nitride–oxynitride multiplayer MOS gate dielectric.

Fabrication of nitrided oxides is a challenging problem for scaled-down CMOS devices. With high-k dielectrics struggling to overcome limitations connected with mobility degradation, charge trapping, uniformity, local defects and process integration difficulties, there is a strong motivation to continue application of oxynitrides at the 65 nm technology node and below [10]. Oxynitrides for gate application must have dielectric constant significantly above the 3.9 of SiO_2, a low number of bulk defects (traps), a low density of surface states at the interface with silicon and excellent thickness uniformity.

The aim of this section is to review the technology, properties and optimization strategy of silicon nitride and oxynitride for application in semiconductor devices. Though the discussion is mainly devoted to nitride storage semiconductor nonvolatile memories, nitrided oxides are also reviewed, because similar technologies are used for ONO and nitrided gate oxide fabrication. Moreover, as shown below, the bottom oxide of ONO is in most cases a nitrided oxide. We will discuss the basic deposition processes and properties of the resultant nitride and oxynitride films and ONO stacks with emphasis on the parameters important for device design and operation. Besides the technologies currently used in mass semiconductor production, we will also discuss promising new approaches.

6.2.1 Traditional deposition techniques

Depending on application, silicon oxynitride (SiO_xN_y) and nitride (Si_3N_4) films can be deposited by a number of methods. The techniques widely used in the semiconductor industry are thermal low-pressure chemical vapor deposition (LPCVD) and plasma-enhanced (PE) CVD [11, 12]. LPCVD stoichiometric nitrides are used as part of ONO memory stacks, control gate dielectrics in EEPROMs with polysilicon floating gates, dielectrics of DRAM (dynamic random access memory) capacitors, material for the sidewall spacers, implant masks, and protection layers. The formation of the LPCVD layer starts with the gas-phase reaction of silane or dichlorsilane (DCS) with ammonia, at temperatures of 620–800°C and pressures of the order of 1 Torr. Adding N_2O or NO gas allows one to fabricate oxynitride films with several at.% oxygen (higher oxygen content requires temperatures above 800°C). A typical nitride deposition reaction is

$$3SiCl_2H_2 + 10NH_3 = Si_3N_4 + 6NH_4Cl + 6H_2 \quad (1)$$

with the flow ratio of DCS to NH_3 1 : 5 and pressure ~400 mTorr in the N_2 carrier gas.

The as-deposited nitride films have refractive indexes in the range 1.9–2.1 and contain several atomic percent of hydrogen, mostly in the form of N–H and Si–H bonds [13]. The presence of hydrogen in Si_3N_4 is a consequence of its structure. In contrast to the two-coordinated O atoms in silicon dioxide, it is difficult for the three-coordinated N atom to find Si partners. Thus, the bonding structure is much less flexible. The nitrogen atoms are located almost in the same plane with the silicon atoms, in contrast to widely varying angles of Si–O–Si bonds in amorphous silicon dioxide. The properties of silicon nitride depend on how close its structure is to that of crystalline material. In a more disordered material the amount of hydrogen strongly increases. Also, the probability of finding defects connected with local deviations from stoichiometry (e.g., Si–Si bonds, Si microclusters and hydrogen-

related defects) is much higher. These defects usually act as traps for electrons and holes (Section 6.4). Some novel deposition techniques that will be discussed below, such as jet vapor deposition (JVD) and atomic layer deposition (ALD) allow one to fabricate nitrides with very low trap density [7, 8, 14] and minimum hydrogen content.

Thermal CVD nitride films are very dense ($3.0\,g\,cm^{-3}$) and highly uniform. In general, they are stable to oxidation (used as barrier layers in LOCOS processes) and chemically inert. The etch rate of nitride films in HF strongly depends on the hydrogen content. It strongly decreases for films containing a low amount of H [15, 16]. Hydrogen is usually measured by TOF-SIMS (time-of-flight secondary ion mass spectroscopy) and multiple (MIR) or Fourier transform (FTIR) infrared spectroscopy. Its amount in the nitride is of principal importance both for device operation (traps, reliability) and integration (dry and wet etch rate, hydrogen out-diffusion).

Due to the constrained bonding configuration, CVD nitride films are rigid and mechanically stressed. One of the latest applications of CVD nitride is creating stresses in the MOS transistor channel in order to increase the mobility of charge carriers (instead of or in addition to employing SiGe substrates). For this purpose stressed nitride cap layers (300–600 Å) are deposited on the salicide after transistor fabrication (before deposition of the premetal dielectric). Different nitrides are used to create stresses of different signs over *n*-channel and *p*-channel transistors [17].

Plasma enhanced CVD nitrides are fabricated at temperatures of 300–400°C from the same gas precursors as thermal LPCVD films (usually SiH_4 and NH_3) and thus are suitable for the back-end processes of microcircuit fabrication. They contain much higher amounts of hydrogen (20–30%) and display a larger variation of refractive index (depending on H content and Si/N ratio). PECVD films are used as barrier and passivation layers, etch stops in dual damascene technology and in MIM (metal–insulator–metal) capacitors. The stoichiometry of PECVD films can be varied over a wide range by changing the silane/ammonia ratio. Si-enriched films have decreased optical gaps and can be used as UV blocking layers. Usually, the thickness uniformity and defect density does not allow one to exploit them as part of gate (ONO) stacks. Nevertheless, it was recently shown that high-density plasma CVD silicon nitrides in ONO stacks had better thickness uniformity and electrical properties compared with the known plasma nitrides [18].

6.2.2 Silicon nitrides and oxynitrides as gate dielectrics

Nitrided oxides and nitride–oxide stacks have been widely used as a gate dielectric in order to reduce gate leakage currents J_g. The improvement originates from higher effective dielectric constant k (as in the case of high-k dielectrics) and features of the oxynitride band diagram. The film thickness required to obtain the same specific capacitance and thus gate electrode control over the MOS transistor channel, is higher in the case of materials with $k > 3.9$, and thus the electric field in the gate dielectric is lower. The bandgap of silicon oxynitride decreases with the increase of the nitrogen content. In the SiO_2 gate oxide, the dominant charge carriers are electrons. With increase of nitrogen content, lowering of the potential barrier for electrons has less influence on the leakage current than electrical field decrease in the nitrided oxide.

Typical parameters that characterize alternative gate dielectric films are the effective oxide thickness (EOT) and the coefficient of leakage current suppression (compared with

SiO_2 of the same EOT). A dielectric constant, k, of the order of 4.6–4.7 was reported for oxynitrides [10, 19]. Oxynitrides with large N content are sometimes called 'middle-k' gate dielectrics to distinguish them from 'real' high-k materials having dielectric constant above $k = 7.5$ of the stoichiometric SiN.

The concentration of nitrogen in MOS devices is different at the Si–SiO_2 interface with the silicon substrate and polysilicon [21, 22]. The optimum nitrogen concentration is not universal, but depends upon the history of the Si surface and the presence of hydrogen in the integration scheme [23]. Values of $1–5 \times 10^{14}\,cm^{-2}$ of N atoms at the interface are typical. Nitrogen concentration at the bottom interface must be low enough so as not to degrade the mobility of charge carriers in the transistor channel, and avoid additional surface charges. A certain concentration of nitrogen at the Si–SiO_2 interface increases immunity to hot carriers and improves the NBTI (negative bias temperature instability) [20], probably because Si–H bonds are substituted with stronger Si–N bonds, or Si–Si bonds are transformed into Si–N (this will be discussed in Section 6.3). The N concentration at the interface with the gate electrode should be much higher than at the bottom interface in order to suppress boron penetration from the P^+-doped polysilicon during the high temperature steps of CMOS fabrication. Higher breakdown voltages and Q_{bd} (charge to breakdown) were reported for oxynitride films with suppressed boron penetration compared with pure oxides with the same EOT [4, 21].

The nitrided oxide is a mixture whose stoichiometric composition is not clearly defined. It should be called nitrogen doped oxide [4] because oxynitride is thermodynamically unstable for most compositions. Nitrogen atoms can interact with Si–Si bonds, but N–O bonds are unlikely in the oxynitride. Several approaches to gate oxynitride (oxynitride stack) fabrication and nitrogen profile engineering have been developed. Most of these methods include: (i) direct oxynitride/nitride growth in NO, N_2O or NH_3 in furnaces and rapid thermal anneal reactors with subsequent treatment in oxygen-containing ambients; (ii) thermal oxidation of Si in dry and wet oxygen with subsequent thermal or plasma nitridation in N-containing atmospheres; (iii) oxide–nitride stack with nitride remote plasma deposition over the bottom ultra thin GOX [21, 23]. The last processing step is usually oxidation in oxygen, NO or water vapor. Some alternative oxynitride deposition techniques, such as N implantation into the GOX with subsequent anneal, or UV enhanced nitridation were reported to give promising results [4, 24], but they are not yet mature enough.

Nitrogen profiles can be obtained from XPS (X-ray photoelectron spectroscopy), SIMS, MEIS (medium energy ion scattering) , NRA (nuclear reactive analyses), EELS (electron energy loss spectroscopy). Back-side SIMS or angle-resolved XPS are advantageous for estimating nitrogen content at Si–SiO_2 interfaces. These techniques will be further discussed in relation with nitrogen distribution in ONO structures [5, 25]. Each of these techniques has its limitations. In particular, artifacts connected with N segregation effects at the interface have been reported [26].

Gate oxidation in nitric oxide is often performed in 0.13–0.18 μm technologies for the formation of high-quality gate oxides. This process is hydrogen free and allows one to incorporate ~$2.5–5 \times 10^{14}\,cm^{-2}$ N atoms in the gate oxide. More than an order of magnitude decrease of the leakage currents compared with the thermal oxide of the same equivalent oxide thickness (EOX) is usually obtained. Figure 6.1 shows the nitrogen profile for a typical 22 Å gate oxide used in 0.13 μm CMOS technology measured by top-side SIMS. Typical for the NO oxidation, the N profile has a rather wide peak, shifted away from the Si–SiO_2 interface due to the final oxidation step.

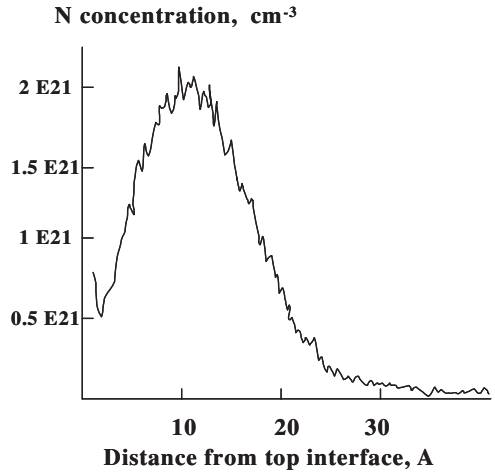

Figure 6.1 Typical nitrogen profile in the 22 Å GOX of the 0.13 µm Tower Semiconductor CMOS technology (TOF-SIMS measurements)

Annealing of thermally grown SiO_2 in NO or N_2O is another way of forming the nitrided oxide. Oxidation in NO results in more efficient nitrogen incorporation and thus allows one to utilize lower temperatures and nitridation times. A pronounced nitrogen peak at the Si–SiO_2 interface is typical of silicon dioxide films first grown and then nitrided in NO or N_2O. It is generally supposed that nitridation in N_2O occurs through its decomposition into NO, O and N_2 [4]. It is difficult to reduce the EOT below 20 Å in the NO nitridation of gate oxide due to the continuous oxide growth at high temperatures in NO, which is not only a nitrogen source, but also an oxidizer.

A controlled way to introduce large amounts of nitrogen into the GOX is thermal or RTP nitridation in NH_3. Thermal nitridation in NH_3 at temperatures as low as 750–850°C and pressures of 100–500 Pa has been reported [27]. Nitridation in ammonia was one of the first techniques employed for oxynitride formation [4]. One of the most important limitations of this technique is the high concentration of hydrogen introduced into the oxynitride films; hydrogen is bonded in complexes acting as traps. In [19, 28] ultrathin gate dielectric were produced by forming a thin nitride layer in an NH_3 ambient at 800–900°C for 30 s. After that, O_2 high-pressure reoxidation (25 atm, 850°C for tens of minutes) was performed. High stability and enhanced surface mobility was reported for the fabricated transistors. A similar approach is described in [10], utilizing water or pure oxygen reoxidation of deposited nitride at 1000–1100°C. Downscaling thickness and increasing nitrogen content in NH_3 RTP-grown oxynitrides is achieved by varying nitridation temperature and/or adjusting post-nitridation annealing. Up to 28 at.% nitrogen can be incorporated into the oxynitride films. Nevertheless, high leakage currents (10^3 A cm^{-2} for minimum EOT) still make application of films scaled down below an EOT of 10 Å (needed for technology nodes below 65 nm) questionable.

Remote plasma nitridation (RPN) does not involve oxidizers and thus is also promising for the 90-nm technology node and beyond [28, 29]. RPN utilizes a remote high-density nitrogen discharge to incorporate nitrogen into the gate oxide film. Low N atom implant

energy from the remote plasma, and high plasma uniformity are required. Otherwise, nitrogen pile-up at the silicon surface and plasma damage effects (degradation of the oxide) can deteriorate the device parameters. The total amount of nitrogen in the oxynitride films obtained by remote plasma nitridation can reach 20%. The fabricated structures are actually ultra thin ON or ONO stacks with a thin nitride film over the gate oxide [30]. For stacked nitride–oxide films formed with this approach, a 50-fold reduction in gate leakage current is observed for EOT ~13 Å [31]. RPN is to a great extent a self-limited process that preserves uniformity and quality of the initial gate oxide. Nevertheless, additional 'post-nitridation' anneals are usually performed after nitrogen incorporation to improve the Si–gate oxide interface. The level of nitrogen in nitrided oxides increases gate dielectric thinness. After integration, the N concentration is typically higher in the upper (close to the gate) part of the oxynitride, consistent with general nitrided oxides engineering strategy.

In another approach to gate dielectric engineering pure silicon nitride films are used. Several novel technologies for SiN deposition have been developed. The distinguishing features of these technologies is very ordered structure of the deposited material that enables a low density of traps and bonded hydrogen. In particular, formation of a crystalline silicon nitride layer on Si substrates by thermal nitridation in a N_2/H_2 mixture was reported [32]. The crystalline layer can also serve as the barrier between Si and high-k dielectric on top of it in engineering gate stacks with EOT < 10 Å.

Silicon nitride films produced by JVD (jet vapor deposition) and ALD (atomic layer deposition) methods are promising both for gate dielectric and ONO applications. In the JVD methodology a supersonic inert carrier gas flow (He) is formed by pumping gas through a nozzle at low (several Torr) vacuum at room temperature [6, 32]. The highly diluted precursor species (silane and nitrogen) are supplied to the surface of the Si wafer. Nitrogen passes through a region of microwave plasma. Energetic nitrogen species and silane molecules are carried by the He flux towards the surface where they form silicon nitride. The kinetic energy of the reacting species is of the order of electron volts, therefore no substrate heating is required. Deposition is localized, thus scanning of the substrate is used to deposit silicon nitride films on the product wafers. The deposition rate and film composition is controlled by the gas fluxes. A post deposition anneal in N_2 at 800°C improves the interface properties [32].

Compared with CVD-deposited Si_3N_4 films, the JVD silicon nitride has a much lower density of bulk traps (of the order of $10^{17}\,cm^{-3}$ compared with 10^{19}–$10^{20}\,cm^{-3}$ usually reported for CVD nitride). In contrast to CVD nitride films, where Poole–Frenkel (P–F) type conductivity is observed, JVD Si_3N_4 films show Fowler–Nordheim (F–N) I–V characteristics in capacitor structures, typical for SiO_2 without bulk traps. This is consistent with the low trap density (no hysteresis in C–V measurements). The oxygen content in the JVD nitride gate dielectric is only a few percent (through the whole depth). FTIR spectra show very small concentrations of hydrogen, mostly in the form of Si–H, consistent with low trap densities. MOS transistors with JVD gate dielectrics (EOT = 10.5 Å) and target leakage current of $10\,A\,cm^{-2}$ were found feasible [32]. JVD silicon nitride was shown promising not only as a CMOS gate dielectric, but also for application as a tunnel dielectric in floating gate memory devices [33]. Low deposition rates of 1–3 Å min^{-1}, and thus low wafer throughput is a limitation of this technology for mass production.

The ALD technique widely used at present for deposition of high-k dielectrics (such as HfO_2, hafnium oxynitride, etc.) has also been successfully employed for deposition of high-quality ultra-thin silicon nitride films. The technique consists in alternately supplying

reacting species to the Si substrate with consecutive reaction of adsorbed monolayers (parts of monolayers) at this substrate. High-quality silicon nitride films synthesized by sequentially supplying $SiCl_4$ and NH_3 gases were reported in [34]. The deposition temperatures are usually in the range 300–600°C, though surface activation that allows one to decrease the temperatures to <100°C has been demonstrated [35]. Post-deposition anneal in ammonia at 550°C improves the properties of the ALD silicon nitride films. Conformal, pinhole free layers with EOT of ~12 Å and dielectric constant of ~7.2 were fabricated after 20 deposition cycles [34] and subsequent ammonia anneal. This anneal was shown to increase the dielectric constant of the ALD film, probably due to termination of dangling bonds at the surfaces of microvoids, and decreasing hydrogen concentration. The distinguishing feature of the fabricated films is the absence of soft breakdown, one of the main reliability limitations of ultra-thin gate oxide films. This is attributed to the strengthened structure of Si–N bonds and high smoothness of the deposited films.

6.2.3 ONO stacks for advanced memories

Ultra-thin ONO stacks for memory application are commonly prepared by thermal growth of a SiO_2 layer (BOX) on silicon, followed by low-pressure chemical vapor deposition (LPCVD) of Si_3N_4. Subsequently, the top oxide is either grown by nitride reoxidation or deposited in a LPCVD process. The typical thickness of individual layers in the ONO stacks ranges from 1.8 to 15 nm. The critical structural and compositional parameters, that affect electrical performance of the ONO-based devices include the physical density of the amorphous oxide/nitride layers, and depth distributions of silicon, oxygen, nitrogen and hydrogen atoms. The BOX has a typical physical thickness of ~18–25 Å for traditional F–N programmed/erased SONOS and 40–70 Å for NROM devices. The BOX is usually formed by oxidation in diluted oxygen or N_2O, or other techniques that ensure a low and controlled silicon oxidation rate. Aside from furnace oxidation, RTP or ISSG (in situ steam generation) processes allow fabrication of device quality BOX [25, 36]. In the ISSG process, a mixture of hydrogen and oxygen flows into a cold-wall chamber, where the Si wafer is placed. The wafer is heated by IR radiation, as in most RTP chambers. Removal of native oxide from the Si surface immediately before BOX formation is critical when growing 20 Å tunnel oxides.

Silicon nitride is usually deposited in LPCVD processes according to Reaction (1) from dichlorsilane/ammonia precursors. The gas ratios are in the range 1/3–1/10, and temperature is usually 680–780°C. Nitride films synthesized at 680°C have lower roughness compared with those synthesized at 740–760°C. Improvement of reliability parameters were reported for smoother films [37]. Nevertheless, there is a compromise with the deposition rates (lower wafer throughputs for lower deposition temperatures). Also, excess silicon is often reported in films deposited at low temperatures. Strong nonstoichiometry is not always desirable, especially in local storage SONOS.

Pyrogenic oxidation of the deposited nitride layer is a typical way to grow the top oxide. As mentioned above, it is very difficult to oxidize silicon nitride thermally. Nevertheless, the situation is different when one carries out the process in the wet ambient created by reaction of H_2 and O_2. Hydrogen and oxygen are combusted in the pyrogenic torch and the resulting activated water vapor flows over the heated wafer. The temperature in nitride pyrogenic oxidation is typically in the range 900–1000°C, and the process lasts tens of minutes to obtain

a top oxide thickness of the order of 100 Å. The thickness of the grown oxide is approximately 150% of the consumed silicon nitride thickness. An alternative to pyrogenic oxidation is the ISSG process in a sub-atmospheric chamber that can be carried out with lower H_2/O_2 ratios. The ISSG process requires a much smaller thermal budget compared with pyrogenic oxidation making integration of ONO easier in many technologies.

Besides the thermal oxidation of silicon nitride, HTO (high-temperature oxide) was shown to be practical as the ONO top oxide in SONOS memories [38]. HTO is deposited at temperatures 800–850°C in LP CVD systems from DCS (or silane) and N_2O precursors. Nitride oxidation before HTO deposition and post-deposition anneal in oxygen is usually performed to control the ONO trapping properties and densify the HTO layer.

Extensive studies have been conducted in order to optimize the ONO properties in traditional SONOS and local storage SONOS with 'thick' BOX [39–43]. Optimization included fabrication of ONO stacks with different oxide and nitride layer thicknesses, using various nitride and oxide technologies in combination with different post-deposition anneals. The device parameters usually compared include the memory window (difference between the threshold voltage V_t of the initial and programmed states), programing and erase times, V_t shifts in programed and erased states after programing/erase cycles (endurance/retention tests) and disturbs (V_t shifts under voltage stresses in different operation regimes). It was found that thinning of the BOX layer to the minimum thickness (still ensuring high retention) was advantageous (see Section 6.6.2). At the same time, an ONO stack with a thicker top oxide (100–150 Å) has better performance both in traditional and local storage nitride memories [42]. The improvement is explained by lower electron injection from a polysilicon gate electrode through thicker TOX and lower charge necessary for programing the structures with thicker TOX to a given V_t. Thus, a smaller amount of holes is injected through the BOX when erasing the memory cells with a thick TOX [42]. Thinning of the nitride layer (final thickness in the SONOS structure) below 30 Å resulted in better retention of OTP (one-time programed) NROM, but strongly degraded the programing time and retention after cycling. This is attributed to the lower probability for electron thermalization in thin nitride films (Figure 6.2) while the total amount of traps is still sufficient for device operation.

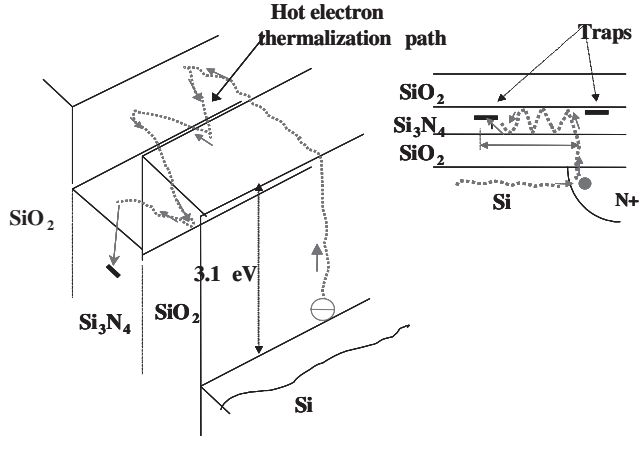

Figure 6.2 Thermalization of hot electrons locally injected into the nitride layer of the ONO structure. Very thin nitride or low trap concentration result in larger lateral shift of electrons from the injection point

Different precursors and deposition conditions were explored to improve the memory properties of the nitride layers. Changing gas ratios and deposition temperatures allows one to form silicon nitride of different stoichiometry. Nitrides fabricated in deposition systems from different vendors, and using different precursors were tested in our experiments with local storage (NROM) devices. Within the temperatures and gas ratios mentioned above, the final ONO structures have only small differences. This was manifested both in programing/erase times, memory window and 'retention after cycling' experiments [41]. Strong enrichment of nitride with silicon (ratios of DCS to ammonia of the order 1 : 1 and above) resulted in poorer NROM retention parameters, especially for specimens deposited at low temperatures. Similar experiments in traditional SONOS (thin BOX oxide, F–N programming/erase) also did not reveal crucial differences between devices with different nitrides [43]. A certain increase of trapping efficiency was reported for nitrides more enriched with silicon. This is an argument supporting the role of excess silicon in the chemistry of nitride traps. At the same time, strongly silicon-enriched nitride films were shown to have worse retention [39, 40]. Poor retention can be the result of electrons hopping between Si dangling bonds (or Si–Si bonds). This explains both enhanced leakage currents in SONOS with F–N tunneling and lateral spread of charge in NROM. Another consequence of these experiments is that most of the 'good' deep traps are introduced into ONO not at the nitride deposition stage, but during subsequent top oxide formation.

Significant efforts were aimed at the reduction of the silicon nitride deposition temperature in LPCVD processes. One option is utilization of BTBAS (tertiary-bytylaminosilane) and HCD (hexachlorodisilane) precursors, interacting with ammonia at 500–550°C. In case of memory application, these technologies still face reliability problems [43].

Besides experimenting with uniform Si–rich nitrides, attempts to improve memory performance of the ONO stack by band engineering of the trap layer were carried out [44]. The idea is to enhance electron and hole trapping by introducing shallow traps in the Si–enriched layer located within standard silicon nitride. The shallow traps in the Si-enriched layer assist the injected carriers in reaching 'good' deep traps [44]. This approach is, unfortunately, impractical in NROM memories because hopping through the silicon-rich part of the nitride layer enhances the lateral spread of trapped electrons before their final thermalization into the deep traps.

An important issue in nitride formation is processing of the BOX before nitride deposition, and anneals after ONO fabrication. Nitridation of the BOX in ammonia, or other nitrogen containing gases, was shown to improve the density of the grown nitride layer and its resistance to oxidation [45]. Post-deposition anneals (in particular, anneals inherent to integration) critically influence SONOS performance and reliability. Post-ONO-deposition anneals in dry oxygen and hydrogen in certain regimes improved endurance/retention performance of the NROM memory.

Measurements of deep trap characteristics were performed in device quality ONO by thermally stimulated exoelectron emission (TSEE) [46, 47]. In this technique the surface of silicon nitride (oxynitride) is irradiated by electrons with energies exceeding the mobility gap of the amorphous material. Secondary electrons and holes fill in the deep traps. The charged specimen is then heated at temperatures sufficiently lower than the temperature of direct thermoionic emission. Nevertheless, emission into the vacuum occurs due to energy transfer effects inside the nitride. The trapped electrons are excited over the mobility edge (conduction band) of the amorphous dielectric and then recombine with trapped holes. The energy released in this process is transferred to the other trapped electron and can be enough for vacuum emission (similar to Auger process). The observed TSEE glow curves are used

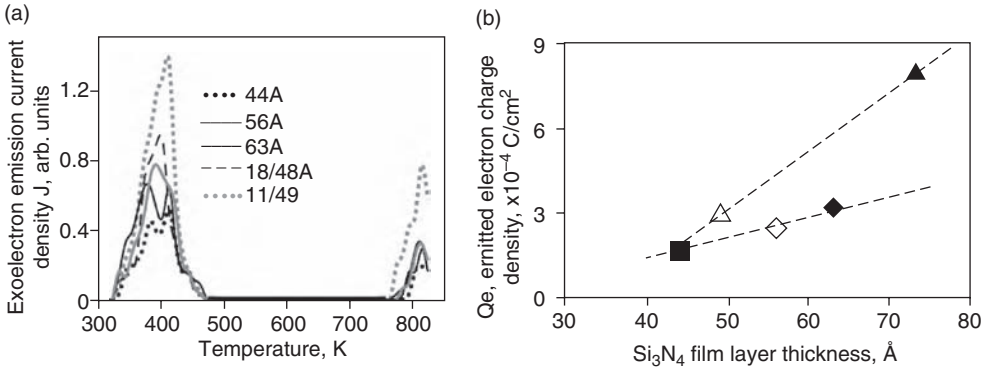

Figure 6.3 (a) TSEE spectra; (b) Integral electron emitted charge density Q_e versus Si_3N_4 film thickness for high-temperature peak. Full squares Si_3N_4 44 Å; open squares Si_3N_4 56 Å; diamonds Si_3N_4 63 Å; open triangles SiO_2/Si_3N_4 18/49 Å; full triangles SiO_2/Si_3N4 11/73 Å. (Reprinted from *Thin Solid Films*, **471**, Naich *et al.*, 166–169. Copyright 2005, with permission from Elsevier)

for calculation of trap activation energy. The electrons (with tens to hundreds of electron volts) penetrate into silicon oxide or nitride to a depth of tens of angstroms. In our space-resolved TSEE measurements $SiO_2/Si_3N_4/SiO_2$ structures were gradually etched in diluted HF acid to remove the TOX and part of the nitride film. Measurements were performed in vacuum (10^{-5} Pa) in the temperature range from 300–850 K. The temperature ramp was 10 K/min. The specimens were irradiated by electrons with energy $W_e = 50$ eV. Irradiation for tens of seconds with currents of the order of tens of nanoamperes resulted in ~1 μC/cm^2 stored charge [47]. The TSEE glow curves for different residual nitride thickness are shown in Figure 6.3(a). Emitted charge density is shown in Figure 6.3(b) as a function of the nitride thickness.

The TSEE signal strongly increases when a 10–20 Å layer of TOX is left at the surface of silicon nitride (oxynitride), indicating that a maximum concentration of traps, responsible for charge storage in ONO, is located at the interface between the top silicon oxide and silicon nitride layers [47]. The effect is more pronounced for the high-temperature peak that corresponds to deep traps with activation energies, Φ of 1.7–1.8 eV (the low-energy peak corresponds to Φ in the range 0.9–1.1 eV).

The same conclusion was reached in [48] by ellipsometry and plasmon loss spectroscopy. Figure 6.4 shows the refractive index of an ONO structure with wet thermal oxide on silicon nitride, as a function of dielectric thickness, measured by single-wave spectroscopy with $\lambda = 632.8$ nm. The refractive index as a function of thickness was obtained using layer-by-layer chemical etching. The bulk refractive index of silicon nitride at $\lambda = 632.8$ nm is equal to 1.96. The silicon oxide bulk refractive index at the same wavelength is equal to 1.46. An abnormally high value of the refractive index is observed at the nitride–TOX interface. The oxynitride refractive index that should be between 1.46 and 1.96 is actually 2.1. This value of refractive index is typical of silicon-rich alloys, such as SiN_x or Si-rich SiN_xO_y, [49]. Independent evidence for excess silicon at the Si_3N_4/thermal SiO_2 interface was obtained using valence plasmon loss spectroscopy [50].

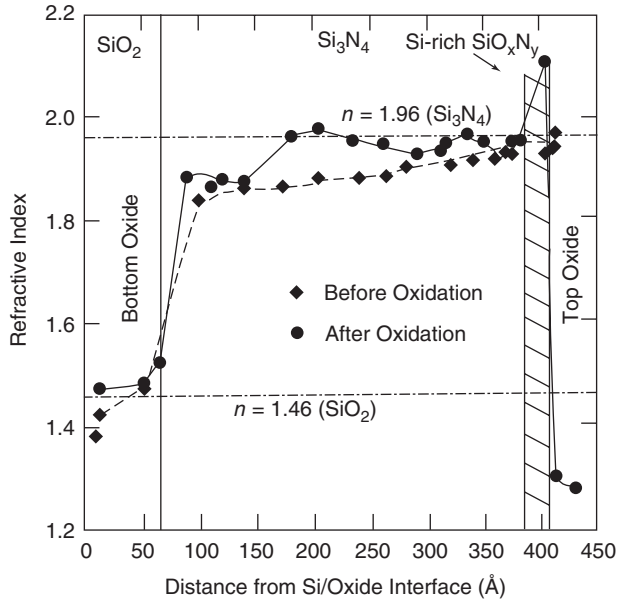

Figure 6.4 Refractive index of $Si/SiO_2/Si_3N_4$/wet SiO_2 structure at different depths [48]. (Reproduced by permission of the Electrochemical Society, Inc.)

6.2.4 Compositional analyses of device-quality ONO stacks

Few systematic studies that analyze the influence of processing conditions on composition of stacked ONO structures, and correlate composition with device parameters, have been reported. It is generally anticipated that a certain level of BOX nitridation is advantageous, similar to the case of nitrided gate oxides. The same is true for hydrogen in the nitride bulk and at the interfaces and for oxygen in nitride. The optimal (from the electrical performance point of view) elemental profiles in the bottom oxide of ONO stacks still remain a subject of debate. The same is true for oxygen content at the top interface of nitride. In this section we report on the elemental distributions in the ONO memory devices fabricated as part of research related to the Tower Semiconductor 0.18 um embedded *micro*Flash® process flow; **micro*Flash® is a trademark of Tower Semiconductor NROM memory, the first commercial implementation of the Saifun NROM™ technology, NROM® is a trademark of Saifun Semiconductors.

As mentioned above, there are limitations and possible artifacts in all techniques employed for compositional analyses of ultra-thin film stacks. To obtain reliable data, a number of characterization techniques were applied, including spatially resolved electron energy loss spectroscopy (EELS) in the transmission electron microscope (TEM), TOF-SIMS (time-of-flight secondary ion mass spectroscopy), back-side SIMS, X-ray photoelectron spectroscopy (XPS) and XRR (X-ray reflectometry) [4, 25, 26, 41, 51]. The profiles of oxygen, nitrogen and hydrogen atoms in the differently processed ONO stacks were analyzed. The ONO stacks consisted of a thermally or ISSG-grown bottom oxide (4–7 nm), an LPCVD silicon nitride layer (6–15 nm) deposited from $SiCl_2H_2$ and NH_3 mixture or in the SiNgen™ process (CVD silane + ammonia process in a special high-throughput

low-thermal-budget reactor), and a top oxide formed either by nitride reoxidation or CVD dielectric deposition (8–13 nm) [25].

X-ray specular reflectometry measurements were conducted using an automatic grazing incidence Rigaku CXR^2 X-ray reflectometer. The density and thickness of each layer in the stack, as well as the interfacial roughness, were determined by fitting to the experimental data. Cross-sectional specimens for TEM were prepared by conventional sectioning, grinding and polishing, followed by dimpling to a thickness of 25 μm and ion-polishing or ion-milling. Phase-contrast imaging was conducted in a JEOL-3010 HRTEM. Following the observations of nitrogen segregation to Si–BOX and polysilicon–TOX interfaces with EELS measurements [26], a special procedure was developed to obtain artifact-free nitrogen profiles. The electron probe (1–1.5 nm diameter) was scanned over the cleaved surface of the ONO stack, and EELS spectra containing all three Si–$L_{2,3}$, O–K, and N–K edges were recorded at each point (pixel of ≤1 nm size). For each scan a freshly irradiated area was used. The beam was scanned parallel to the interfaces, and the individual spectra were summed along the scanning direction. Finally, the distribution of integrated intensity as a function of spatial coordinate were obtained. XPS measurements were carried out using a 'Specs' RQ 20/38 hemispherical electron analyzer. The sputtering was performed by Ar^+ ions beam with energy of 3 keV. SIMS measurements were conducted in a Physical Electronics ADEPT quadrupole instrument. The detection limits for N and H were estimated to be 4×10^{18} and 2×10^{19} atoms cm^{-3}, respectively. The spatial scale of the SIMS depth profiles was normalized to the total thickness of the corresponding films, as measured by XRR and ellipsometry. TOF–SIMS measurements were done using the PHI Model 2100 TRIFT II dual beam system. Sputtering was performed by Cs^+. The analysis was made using pulsed Ga^+ primary ion beam at an energy of 15 keV. The detected fragments were: Si_2, ^{28}Si, SiN, H, SiON, and SiO_2. Estimation of the H concentration in silicon oxide, silicon nitride and silicon matrixes, was done by using calibration samples.

A typical HRTEM image of a device-quality ONO stack Si/SiO_2(6.5 nm)/Si_3N_4(5 nm)/SiO_2(10 Å) is shown in Figure 6.5. The image reveals three well-defined layers. Distributions of N, Si, O and H are analyzed over the ONO structure.

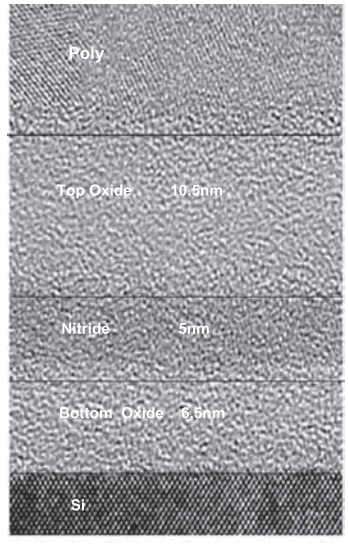

Figure 6.5 TEM image of the ONO stack [5]. (Reproduced by permission of the Electrochemical Society, Inc.)

1. Nitrogen. EELS artifact-free measurements (with the detection limit of ~2%) do not show pronounced interface segregation of nitrogen at the SiO_2–Si interface for specimens formed by TOX pyrogenic oxidation (Figure 6.6).

The spectra depend upon the direction of scanning. The nitrogen peak is detected only at the interface that is reached last. Nevertheless, the TOF–SIMS depth profiles of the same specimen (front side) show pronounced peaks related to nitrogen at the Si–SiO_2 interface. The nitrogen peak at the Si–SiO_2 interface was almost an order of magnitude smaller in ON specimens Si/SiO_2(6.5 nm)/Si_3N_4(11 nm) where no top oxide was formed, thus indicating that nitrogen was redistributed in the BOX during the top oxide pyrogenic oxidation. Nitrogen redistribution in the BOX during anneal was further confirmed by back-side TOF SIMS measurements. Silicon was removed from the back side of the wafer and SIMS profiling started from the BOX. Figure 6.7(a) shows the nitrogen profiles in the ONO sample after thermal top oxide formation and integration in the real memory device. An increase of the nitrogen concentration at the Si–SiO_2 interface (~1 at.% nitrogen) is observed in the

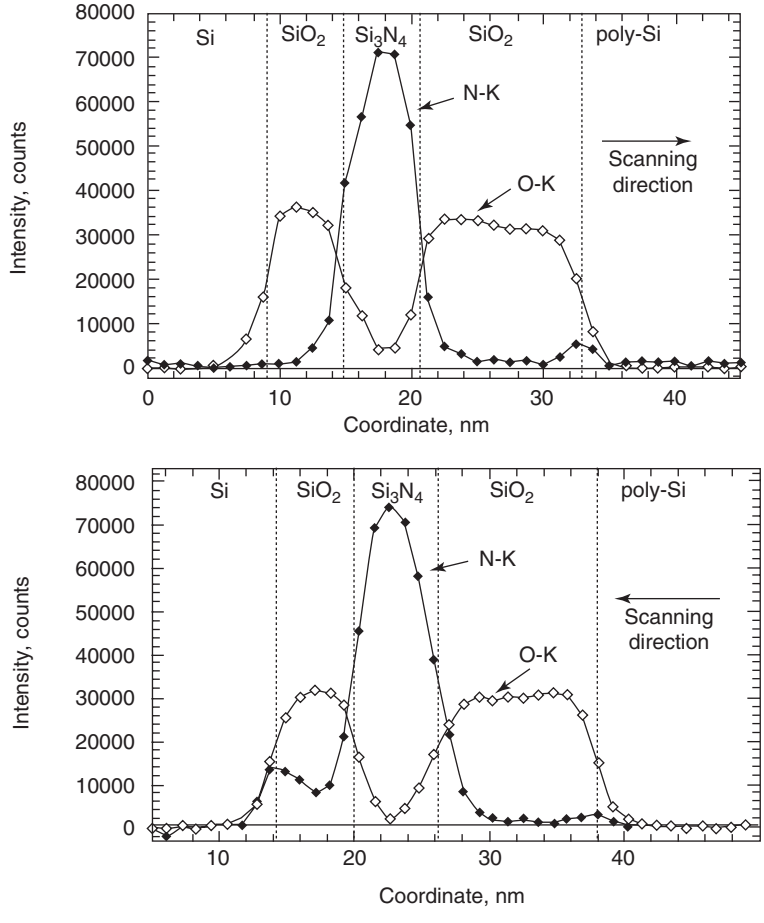

Figure 6.6 EELS measurement in HRTEM on a cleaved ONO structure. Direction of scanning is shown by the arrows [5] (Reproduced by permission of the Electrochemical Society, Inc.)

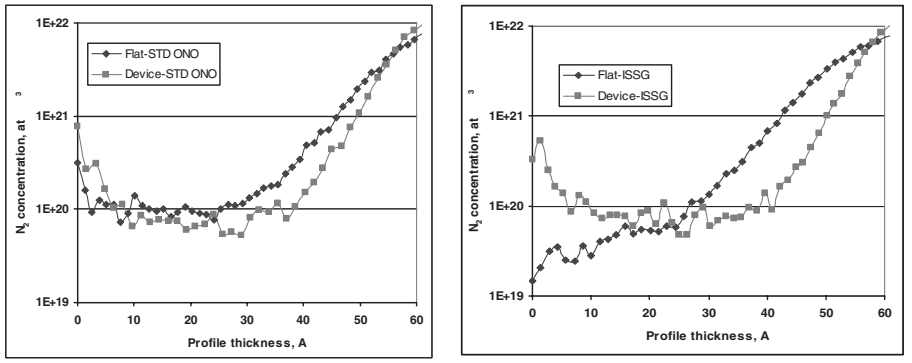

Figure 6.7 Nitrogen profiles obtained from back-side TOF SIMS measurements: (a) thermal; (b) ISSG/SiNgen ONO before and after integration [25] (Reproduced by permission of the Electrochemical Society, Inc.)

Table 6.1 Density and thickness of layers in ONO specimens [5] Copyright (2004). Reproduced with the permission of the Electrochemical Society, Inc.

Sample	Bottom oxide			Nitride			Top oxide		
	Thickness	Thickness	Density	Thickness	Thickness	Density	Thickness	Thickness	Density
	TEM	*XRR*	*XRR*	*TEM*	*XRR*	*XRR*	*TEM*	*XRR*	*XRR*
ONO-1	5.8	6.4	2.18	6.4	6.6	2.76	9.1	8.7	2.04
ONO-2	6.0	6.4	2.18	7.8	8.2	2.8	12.5	12.4	2.16
ONO-CVD	6.0	6.0	2.22	6.3	6.1	2.77	13.1	13.4	2.04

as-deposited specimens. The peak increases approximately twice after integration, and nitrogen concentration increases at the silicon nitride interface. Figure 6.7(b) shows the results of the back-side SIMS measurements for ISSG ONO (low thermal budget of top oxidation). There is no peak at the Si–SiO_2 interface after ONO formation, but it appears after integration. Similar data are observed for ON specimens. Nitrogen is introduced during silicon nitride deposition onto the BOX, and is redistributed in the BOX during high-thermal-budget operations, probably with segregation at the Si–SiO_2 interface.

Density and thickness of individual layers in different ONO specimens, measured by XRR are summarized in Table 6.1.

The first two ONO samples had pyrogenic TOX of different thickness, while the third specimen had a CVD top oxide. All specimens show very similar BOX densities (2.18 g/cm^{-3}), and all are significantly larger than the density of BOX prior to nitride deposition (2.11 g/cm^{-3}). Furthermore, fitting to the experimental XRR data suggests significant density gradient in the single BOX layer (before nitride deposition). The XRR data could be fitted much better using a nonuniform density model, with the BOX density varying from 2.22 g/cm^{-3} at the Si–SiO_2 interface to 1.99 g/cm^{-3} at the surface with silicon nitride. These results suggest strong nitridation of the upper part of the bottom oxide at the stage of preliminary

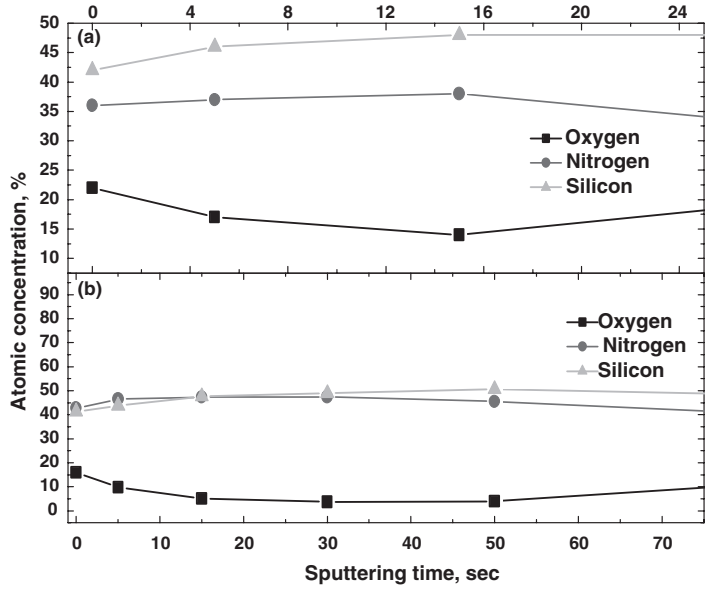

Figure 6.8 Atomic concentration of elements from XPS: (a) relative atomic concentration for ONO sample fabricated by pyrogenic oxidation of nitride after the top oxide layer was etched away; (b) oxide–nitride sample without the subsequent oxidation, as a function of the sputtering time [5] (Reproduced by permission of the Electrochemical Society, Inc.)

nitridation and during subsequent growth of the nitride. This observation is consistent with relatively easy nitridation of the BOX top surface in ammonia at 750°C [27]. The TOX density is lower than the BOX density, with much smaller amount of nitrogen.

The observed nitrogen distribution in the BOX is one of the key factors explaining excellent reliability of *micro*Flash memories. Slight nitridation of the Si–SiO_2 interface makes it stable, even in devices that employ hot holes for erase, consistent with reported results on nitrided oxides for CMOS gate application.

2. Silicon/nitrogen ratio. The concentration of elements at the surface of the silicon nitride layer (DCS and ammonia reaction), after nitride layer deposition and chemical removal of the thermal TOX, in the ONO structure are shown in Figure 6.8(a,b).

It is interesting to note that the Si/N ratio is higher at the interface compared with Si/N of the stoichiometric nitride even for the as-deposited nitride film. This ratio increases after the TOX removal, indicating additional excess silicon at the top oxide–nitride layer. Similar results were obtained in [48] by top EELS analyses and in [43] by RBS (Rutherford backscattering).

3. Oxygen. It follows from the EELS spectra that significant oxygen concentration (O–K intensity, see Figure 6.6) exists at the TOX–nitride interface, but decreases to the noise level ($3\sigma = 2$–3%) in the middle of the nitride layer (see Figure 6.6(b)). A significant amount of oxygen was also observed by EELS and TOF–SIMS at the surface of ON samples, even if the top oxide was not intentionally formed (Figure 6.9).

The sample was stored in room ambient for several days after the nitride deposition. The concentration of oxygen atoms obtained from XPS is 16 at.% for the oxide–nitride (ON)

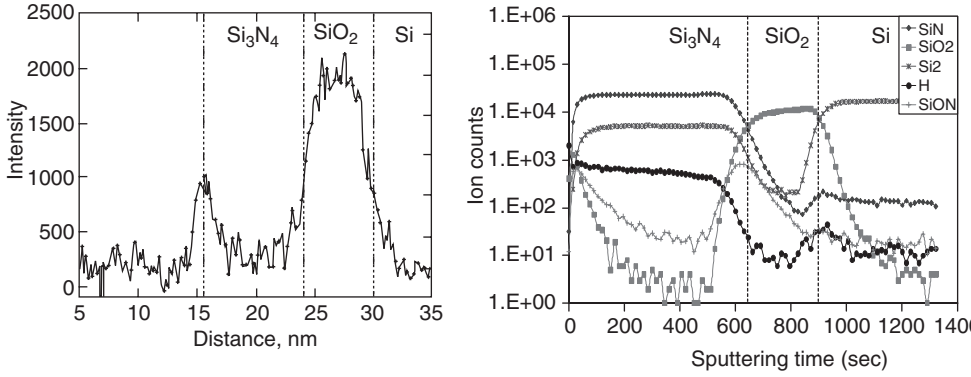

Figure 6.9 EELS and SIMS data showing large amount of oxygen at the surface of Si/SiO_2(62 Å)/Si_3N_4(111 Å) specimen (no top oxidation) [5] (Reproduced by permission of the Electrochemical Society, Inc. and reprinted with permission from *J. Vac. Sci. Tech.*, **23**, M. Saraf, R. Edrei, R. Akhvlediani, Y. Roizin, R. Shima and A. Hoffman, Chemical bonding in $SiO_2/Si_3N_4/SiO_2$ stacks obtained by thermal oxidation of silicon nitride layers. Copyright (2005) the American Institute of Physics)

specimen. This concentration increases to 23% for silicon nitride subjected to pyrogenic oxidation. For both samples there are chemical shifts in the XPS spectra relative to pure silicon nitride and silicon oxide. Therefore, oxygen incorporation into the silicon nitride both during intentional thermal oxidation or native oxidation, creates a silicon oxynitride layer. Nevertheless, oxygen is bound differently when it is incorporated by native oxidation, or thermal oxidation at high temperature. The XPS peak chemical shifts indicate that formation of O–N bonds is preferred during intentional thermal oxidation, whereas in native oxynitrides Si–O bonds dominate in the oxynitride layer. The intensities of SiO_2 and SiON fragments in the oxynitride are higher in the oxidized specimens as XPS and TOF–SIMS results show.

4. Hydrogen. SIMS hydrogen profiles for complete ONO stacks feature three well-resolved H maxima, corresponding to the bottom SiO_x/Si interface, the nitride layer and the top SiO_x/polysilicon interfaces. As follows from Figure 6.9, the hydrogen content in the nitride layer of the ON structure is higher at the top surface (~12 at.%) decreasing to 7 at.% in the bulk). Hydrogen content considerably decreases during the growth of the top oxide becoming about 1.5 at.% in the bulk of the nitride layer. Nevertheless, hydrogen concentration in the intermediate oxynitride layer remains high (about 7 at.%) after the top oxide formation. There is a strong correlation between oxygen and hydrogen content in the oxynitride layer, the hydrogen signal follows the oxygen signals in SiO_2 and SiON.

The hydrogen concentration in the ONO stack is a critical issue for device performance and reliability. Hydrogen is introduced into ONO during its formation and in the back-end processes, such as deposition of isolation layers, hydrogen anneals, etc. Measurement of memory cells fabricated with ONO containing different amounts of hydrogen indicated that trapping efficiency (programing times or size of memory window) depends on the amount of hydrogen present. Low-hydrogen-content structures were obtained by dry oxidation of nitride at 1200°C. The amount of hydrogen in nitride decreased to 0.5 at.% after this type of oxidation. It was difficult to program ONO devices with decreased amount of hydrogen [41]. At the same time, lateral charge spread of the locally trapped charge in NROM memory cells was enhanced when the amount of hydrogen entering the ONO stack from the back-end processes was too high. Substitution of hydrogen with deuterium at all stages of ONO stack

fabrication led to less pronounced degradation in subsequent TSEE tests [52], and we attribute this to differences in vibrational dynamics of corresponding bonds. The results show that hydrogen is strongly involved in memory trap chemistry. Possible candidates for deep traps are complexes including excess Si and hydrogen in the oxynitride matrix.

Summarizing this section, we want to emphasize that there are specific demands for ONO layers in NROM memories:

1. The density of traps in nonstoichiometric nitride (the upper part of the silicon nitride layer in ONO that is actually the trapping media), must be optimized. On one side it must be high enough to allow storage of a high concentration of charge in a small volume and on the other side it must suppress lateral hopping that results in retention loss.
2. The trap activation energy must be high, so as to prevent lateral redistribution of trapped electrons during anneals.
3. To achieve high endurance (number of program/erase cycles), the BOX must have high hot carrier immunity.
4. The top oxide must be dense and thick enough to suppress parasitic electron injection from the polysilicon electrode in the erase operation.

These demands are satisfied in conventional ONO layers where the top oxide is fabricated by pyrogenic oxidation of the deposited silicon nitride film at 950–1050°C and in ONO stacks with ISSG top oxide or CVD deposited HTO. Though novel approaches to ONO formation have been proposed, e.g., utilization of strongly nitrided oxides as the trapping layer [53], high-density plasma CVD nitride [54], ALD nitride [8], etc., production recipes of most SONOS memory vendors still employ DCS/ammonia nitrides. This is due to specific semiconductor industry requirements that include not only performance/reliability, but also such criteria as high equipment throughput, high uniformity on large wafers with low defect densities, and sufficient control of properties in process integration.

6.3 ATOMIC STRUCTURE OF SILICON OXYNITRIDE

Short-range order in tetrahedral solids such as Si, SiO_2, α-Si_3N_4 and β-Si_3N_4, amorphous Si_3N_4, and crystalline Si_2N_2O is described by the octahedral Mott rule as

$$N_c = 8 - n \tag{2}$$

where N_c is the coordination number and n is the number of valence electrons. The Si atom has four valence electrons ($3s^2 3p^3$), and according to Equation (2), its N_c is equal to 4. The O atom has six valence electrons ($2s^2 2p^4$). Therefore, in SiO_2 and c-Si_2N_2O, each O atom is coordinated by two Si atoms. Similarly, the N atom has five valence electrons ($2s^2 2p^3$), while in Si_3N_4 and c-Si_2N_2O, each N atom is threefold coordinated by Si atoms [49, 55]. If short-range order in 'ideal' a-SiO_xN_y is also governed by the octahedral Mott rule, the following relationship must be observed:

$$4 = 2x + 3y \tag{3}$$

where x and y are the composition parameters in the chemical formula SiO_xN_y. Thus, the number of Si bonds must be equal to the total number of N and O bonds.

The accuracy of Equation (3) was verified by plotting $4/(2x + 3y)$ versus $x/(x + y)$, where the parameter $x(x + y)$ characterized the chemical composition of a-SiO_xN_y. A deviation of about 6% from the Mott rule can be found from the plot in Figure 6.10 [55]. However, when the concentration of hydrogen bonds [N_H] was taken into account for each sample, the plot of $4/(2x + 3y\text{-}[N_H])$ versus $x/(x + y)$ deviated from the Mott rule by less than 2%, which is the accuracy of a-SiO_xN_y composition determination by X-ray photoelectron spectroscopy (XPS). The results show that the Mott rule governs the short-range order in a-SiO_xN_y for all compositions ranging from SiO_2 to Si_3N_4.

There are two extreme models for modeling the structure of tetrahedral amorphous nonstoichiometric alloys: the random mixture model (RMM) and the random bonding model (RBM). According to the RMM, the SiO_xN_y film consists of separate SiO_2 and Si_3N_4 phases and SiN_x film consists of separate Si_3N_4 and Si phases. In the RBM it is assumed that the SiO_xN_y and SiN_x films consist of a network of five tetrahedra SiO_vN_{4-v} and SiN_vSi_{4-v} (where $v = 0$, 1, 2, 3 and 4), respectively [56–59]. Figure 6.11 shows the Si 2p core level XPS of amorphous SiO_xN_y films with different compositions [57]. Experimental spectra are shown by dots while the simulated spectra from RMM and RBM models are presented by solid lines. SiO_xN_y layers of different compositions (from SiO_2 to Si_3N_4) consist of Si–O and Si–N bonds and involve five types of tetrahedral SiO_vN_{4-v} elements with $v = 0$, 1, 2, 3, 4 (SiN_4, $SiON_3$, SiO_2N_2, SiO_3N, SiO_4). The probability of finding a particular tetrahedron SiO_vN_{4-v} in the oxynitride with (x,y) composition is given in the RBM by the random statistics:

$$W(v,x,y) = \left(\frac{2x}{2x+3y}\right)^{v}\left(\frac{3y}{2x+3y}\right)^{4-v}\frac{4!}{v!(4-v)!} \tag{4}$$

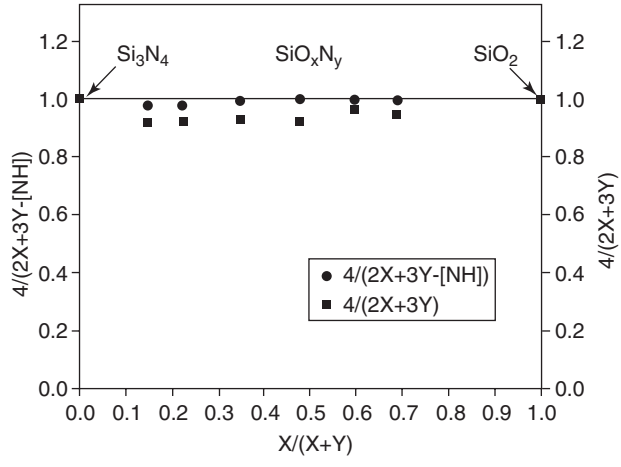

Figure 6.10 Experimentally determined relationship of the number of silicon bonds versus the sum of nitrogen and oxygen bonds in SiO_xN_y for different compositions (Reprinted Fig. 3 with permission from [55], Copyright (1998) the American Physical Society)

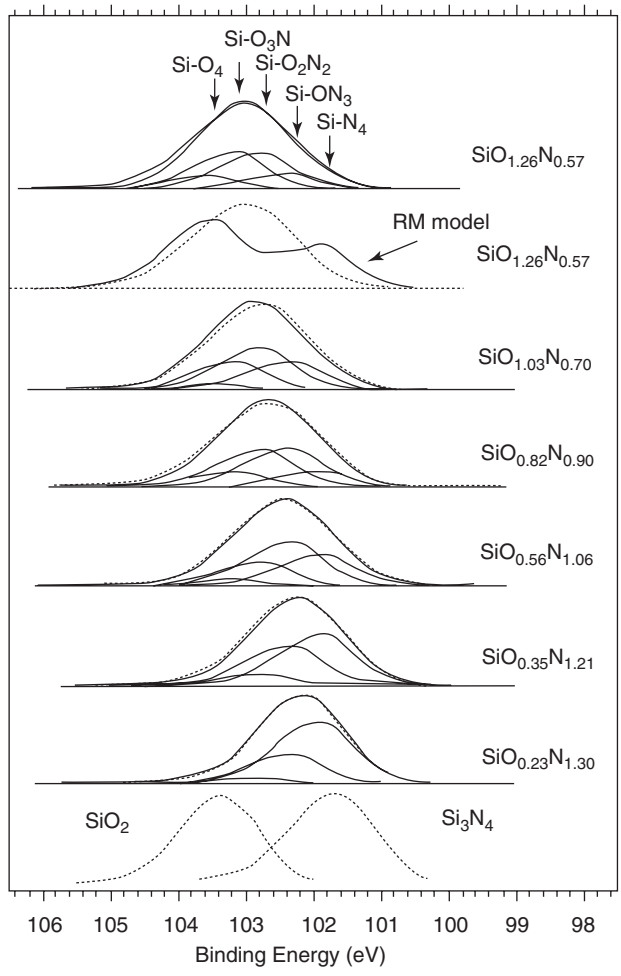

Figure 6.11 Si 2p XPS spectra of SiO_xN_y with different compositions. The experimental spectra are shown by dots and the simulated spectra are depicted by solid lines (Reprinted with permission from [57], Copyright (2002) Elsevier)

In the XPS results only one peak was observed for the six samples with different compositions (different x and y). According to the RMM model, the XPS Si 2p spectrum should have two components, corresponding to the SiO_2 and Si_3N_4 phases (Figure 6.11). Therefore, the RMM model does not describe the structure of SiO_xN_y. At the same time, it follows from Figure 6.11 that the experimental Si 2p spectra of SiO_xN_y and thus the short-range order of the oxynitride can be quantitatively fitted by the RBM model.

The octahedral Mott rule which governs short-range order in a-SiO_xN_y is the key to explaining the origin of defects and traps in the oxynitride layers. It was suggested that nitridation of SiO_2/Si system results in removal of Si–Si bonds, which are hole traps in MOS devices. The removal of hole traps from the SiO_2/Si interface during the oxide nitridation can be understood from the reaction

$$3 \equiv Si{-}Si \equiv +2N \rightarrow 2 \equiv Si_3N \tag{5}$$

As it was discussed above, Si–Si bonds can also be located in the transition oxynitride layer at the nitride–TOX interface. Device-quality ONO stacks are obtained by intentional oxidation of nitride layers, or exposure to air, followed by deposition of the top HTO oxide [46–48, 50, 60–61]. An oxynitride layer is formed at the interface between the nitride and TOX in both cases. It is strongly suggested that electron and hole trapping in ONO is connected with excess silicon in this oxynitride layer. The following reaction (consistent with the Mott rule) illustrates nitride interaction with oxygen and explains enrichment of the oxynitride layer with silicon after oxidation:

$$\begin{aligned} 2 \equiv Si_3N + 2O \rightarrow 2 \equiv Si_2O + 2 \equiv Si\cdot + 2N \\ \equiv Si\cdot + \cdot Si \equiv \rightarrow \equiv Si{-}Si \equiv . \end{aligned} \tag{6}$$

6.4 TRAPS IN THE NITRIDE LAYER OF ONO

The electron and hole trap densities in CVD silicon nitride have surprisingly close values. The density of electron traps is very high and equal to the density of hole traps $N_t^e = N_t^h \sim 10^{19}$–$10^{20}\,cm^{-3}$. This directly follows from the maximum charge that can be trapped in the silicon nitride layer of ONO. Cross-sections of electron traps are equal to the cross-section of hole traps and have an enormously high value, $\sigma_t^e = \sigma_t^h \simeq 5 \times 10^{-13}\,cm^2$, consistent with the short times required for programing and erase in SONOS devices. Thermal energy of trap ionization for electrons is equal to the ionization energy for holes $\Phi_e = \Phi_h \simeq 1.5 - 2.0\,eV$ (spread of ionization energy reported by different authors is connected with ONO technology differences and employed measurement techniques). Attempt-to-escape frequencies are also close for trapped electrons and holes, $\nu_t^e = \nu_t^h$ [62, 63]. These facts indicate that traps in silicon nitride are amphoteric, i.e., they can be in neutral, negatively charged and positively charged states D_0, D_- and D_+, respectively. Both in the as-deposited and programed device-quality CVD nitride films, there is no electron spin resonance signal, so the traps are diamagnetic [64].

Even an almost stoichiometric (within the accuracy of measurements) CVD silicon nitride can localize electrons and holes. As mentioned above, ALD and JVD nitride films, which are denser and have much less hydrogen show suppressed trapping. Polaron effects (interaction with lattice) are strongly pronounced in the energetics of nitride and oxynitride traps. Otherwise, tunneling between the deep traps (DC hopping conductivity) is manifested between traps located at a mean distance $(N_t)^{-3} \sim 30\,Å$. Nevertheless, hopping conductivity becomes pronounced only in materials intentionally enriched with silicon.

Several models to account for the observed properties of traps in silicon nitride and oxynitrides have been proposed. The intrinsic defects leading to the memory effect in amorphous Si_3N_4 were traditionally associated with undercoordinated silicon and the nitrogen bonds $N_3Si\cdot$ (K^o defect) and $Si_2N\cdot$ (N^o defect). Absence of the ESR signal is often explained by the negative correlation energy of traps [64, 65]. The negative correlation energy model assumes that the reaction $2Do = D_+ + D_-$ is energetically favorable. In this case a negatively charged center with two electrons is a hole trap and a positively charged D_+ is an electron trap for. Both are diamagnetic and thus no ESR signal is expected in equilibrium and programed states. The model predicts high cross-sections but, nevertheless,

σ_t^e and σ_t^h can not exceed $N_t^{-2/3}$. Even in the case of $N_t = 10^{19}\,cm^{-3}$ (actual trap concentrations are higher), defined cross-sections are much smaller than the experimentally observed values (5×10^{-13}–$10^{-12}\,cm^2$). An additional mechanism explaining high cross–sections is thus necessary, for example trapping of electrons and holes injected into the silicon nitride by shallow traps with subsequent thermalization into deep traps.

Various atomistic structures were considered as candidates for the negative correlation energy traps. The popular Si dangling bonds model suggested that two diamagnetic defects, a positively charged N_3Si^+ and a negatively charged N_3Si^-, could be formed from a $N_3Si\cdot$ (paramagnetic neutral defects in Si_3N_4) pair via the following reaction:

$$N_3Si\cdot + \cdot SiN_3 \rightarrow N_3Si^+ + :^-SiN_3 \tag{7}$$

The repulsive energy U_C of two electrons localized in the Si atoms is over-compensated by the energy gain U_L coming from lattice relaxation so that the effective correlation energy $U = U_C + U_L$ is negative. Nevertheless, *ab initio* density functional theory (DFT) calculations [66, 67] showed that the correlation energy U for $N_3Si\cdot$ defects was equal to +0.1 eV, and even larger if the defects were at large distances. In agreement with [66], calculations of [67] show that the isolated $N_3Si\cdot$ defect can be a trap for electrons. However, the total energy of the two neutral $N_3Si\cdot$ defects is ~2.1 eV less than the total energies of the negatively charged (N_3Si^-:) and the positively charged (N_3Si^+), when the long-range polarization is taken into account. Thus, trapping of a hole by $N_3Si\cdot$ requires high energy, and thus conversion of a pair of neutral three-fold coordinated silicon atoms $N_3Si\cdot$ into a pair of charged diamagnetic states (N_3Si^+, and N_3Si^-:) according to Reaction (7) is energetically unfavorable. At short distances $N_3Si\cdot$, the silicon dangling bonds can exchange electrons and formation of a neutral diamagnetic ≡Si–Si≡ bond from the ≡Si· defects will occur [67, 68]

$$N_3Si\cdot + \cdot SiN_3 \leftrightarrow N_3Si{-}SiN_3 \tag{8}$$

It was suggested that the diamagnetic neutral ≡Si–Si≡ defect could capture electrons and holes [50, 59–60, 62–63, 69]. To explain the absence of the ESR signal in the programed state, antiferromagnetic pairing of localized spins was proposed in [70]. Due to Coulomb repulsion, the localized electrons in silicon nitride create a quasi-periodic Wigner glass. Absence of the ESR after electron or hole localization can be related to spin pairing due to Wigner crystallization.

Another candidate for the negative correlation energy centers are pairs of N^o and K^o, which where shown to have negative correlation energy when located at close distances. Nevertheless, this configuration is problematic because the strength of the Si–N bond is hardly over-compensated by the electrostatic interaction of K^+–N^- pair [66].

Negative correlation energy configurations in silicon nitride that include hydrogen atoms are still the subject of debate. As discussed above, large concentrations of hydrogen are always present in the oxynitride trapping layers at the nitride–TOX interface of ONO structures in parallel with excess silicon. Thus, configurations of silicon and hydrogen are plausible candidates for trap centers. It was suggested that Si–H–Si and Si–HH–Si bonds could be negative correlation energy centers [71–74]. In the first case the energy of the three-bond center decreases as a result of the hydrogen atom shift to one of Si atoms in the D^- state (Si–H bond facing Si dangling bond). In the Si–HH–Si (sometimes called the $H_2\cdot$ model)

two hydrogen atoms are located at a stretched Si–Si bond: one in a BC (bond-centered) site and the other at a Si dangling bond. The Si–HH–Si and closely located stretched Si–Si bond can form a negative correlation energy pair of centers. In this case the Si–Si bond acts as D_+ and S–HH–Si as D_-. DFT calculations show that the energy gain for hole localization at the Si–Si bond is ~1 eV [67]. Trapping of electrons and holes is accompanied by hydrogen migration between S–HH–Si and Si–Si with creation of two Si–HD centers (dangling bond and Si–H complexes). Three important conclusions readily follow from the above model: (i) traps in silicon nitride are spatially correlated, i.e., larger amount of closely located pairs of traps (groups of Si–Si bonds or microscopic a-Si clusters) compared with random distribution in space; (2) attempt-to-escape frequencies of trapped electrons must be significantly lower than phonon frequencies; (3) hydrogen can be reintroduced into ONO structure annealed at high temperature, similar to the case of a-Si:H [73]. These peculiarities were observed experimentally [62–63, 75].

6.5 CHARGE TRANSPORT IN SILICON NITRIDE

Conductivity mechanisms of ONO stacks in the vertical (perpendicular to the substrate plane) direction are of principal importance for conventional SONOS devices with thin tunnel oxide programed by the F–N mechanism. For these devices programability, retention and behavior under voltage stresses strongly depend on the ionization rates of traps in the nitride layer. Vertical conductivity of ONO in NROM devices that employ thick (>40 Å) BOX is less important, but lateral migration of charges in the nitride layer, also governed by ionization of traps in nitride becomes the critical issue.

In 1938 Frenkel proposed a theoretical model for the explanation of the $I \sim \exp(\alpha F^{1/2})$ law for conductivity of dielectrics with traps (F is the electrical field in nitride) [76] that assumed a Coulomb barrier lowering effect in the electric field. Presently, it is widely accepted that the trap ionization mechanism in SiN_x is the Frenkel effect. However, trap ionization in semiconductors is accurately explained by the Frenkel model only for low ($<10^3$ V/cm) electrical fields [77]. In high fields ($>10^3$ V/cm), a multi-phonon model of trap ionization [78, 79] was considered. Figure 6.12 shows the energy diagram of a MNOS structure (no TOX, 18 Å BOX) used in the two-band model of electron and hole transport in Si_3N_4 [63]. Electrons are injected into the nitride from the negatively biased contact, and hole injection occurs from the positively biased contact. The model supposes recombination of the electrons with localized holes and holes with localized electrons. The trap occupation rates are given by Shockley–Read–Hall statistics. Electrons and holes are supposed to have equal capture and recombination cross-sections, $\sigma_r^e = \sigma_r^h = \sigma_r = 5 \times 10^{-13}\,\mathrm{cm}^2$ [63]. The continuity and Poisson's equations are solved in the regime of double injection. The kinetics of free and trapped charges in nitride is described by the equations:

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{e}\frac{\partial j(x,t)}{\partial x} - \sigma_r \upsilon n(x,t)(N_t - n_t(x,t)) + n_t(x,t)P^{(n)}(x,t) - \sigma_r \upsilon n(x,t)\,p_t(x,t) \quad (9)$$

$$\frac{\partial n_t(x,t)}{\partial t} = \sigma \upsilon n(x,t)(N_t - n_t(x,t)) - n_t(x,t)P^{(n)}(x,t) - \sigma_r \upsilon p(x,t)\,n_t(x,t) \quad (10)$$

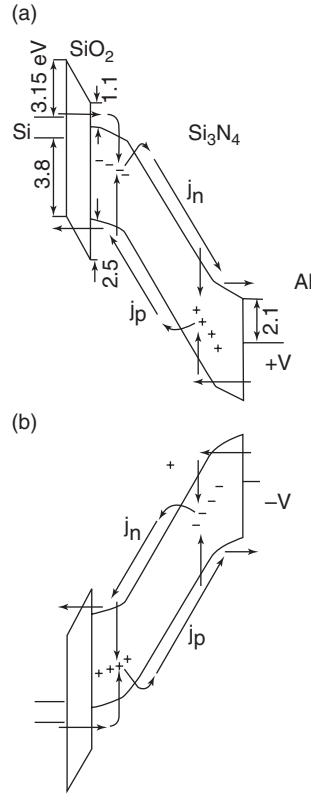

Figure 6.12 Energy diagrams of MNOS structure for two-band model of charge transport in Si_3N_4: (a) positive potential on the metal gate; (b) negative potential on the metal gate (Reprinted with permission from [63], Copyright (2006) American Institute of Physics)

$$\frac{\partial p(x,t)}{\partial t} = \frac{1}{e}\frac{\partial j_p(x,t)}{\partial x} - \sigma v p(x,t)(N_t - p_t(x,t)) + p_t(x,t)P^{(p)}(x,t) - \sigma_r v p(x,t) n_t(x,t) \quad (11)$$

$$\frac{\partial p_t(x,t)}{\partial t} = \sigma \upsilon p(x,t)(N_t - p_t(x,t)) - p_t(x,t)P^{(p)}(x,t) - \sigma_r \upsilon p(x,t) n_t(x,t) \quad (12)$$

$$\frac{\partial F}{\partial x} = -e\frac{(n_t(x,t) - p_t(x,t))}{\varepsilon\varepsilon_0} \quad (13)$$

Here, n, N_t and n_t are densities of free electrons, electron traps, and occupied traps, respectively and p and p_t are the densities of free and captured holes. We assume that the electrons and holes tap densities are equal $N_t^e = N_t^h$, $F(x,t)$ is the local electric field, e is the electron charge, $\sigma = 5 \times 10^{-13}\,cm^2$ is the capture/recombination cross-section, υ is the velocity of the electron or hole drift in the mobility band, and $\varepsilon = 7.5$ is the low-frequency dielectric constant of Si_3N_4. The electron and hole drift currents are written as $j = en\upsilon$ and $j_p = -ep\upsilon P^{(n,p)}$ is the probability of the trap ionization [s^{-1}].

Two models of trap ionization were considered [63]: a modified Frenkel model including thermally assisted tunneling (TAT) and a multi-phonon trap ionization.

The ionization probability in the Frenkel model is given by the equation:

$$P = \nu \exp\left(-\frac{W_t - \beta\sqrt{F}}{kT}\right) \qquad \beta = \sqrt{\frac{e^3}{\pi\varepsilon_\infty\varepsilon_0}} \tag{14}$$

Here, W_t is the trap energy, $\varepsilon_\infty = 4.0$ is the high frequency Si_3N_4 dielectric permittivity and ν is the attempt-to-escape frequency.

In the thermally assisted tunnel mechanism with a Coulomb trap potential, the ionization probability is:

$$P = \frac{\nu}{kT}\int_0^{W_t-\beta\sqrt{F}} d\varepsilon \exp\left(-\frac{\varepsilon}{kT} - \frac{2}{\hbar}\int_{x_1}^{x_2} dx\sqrt{2m^*(eV(x)-\varepsilon)}\right)$$

$$V(x) = W_t - \frac{e}{4\pi\varepsilon_1\varepsilon_0 x} - Fx \tag{15}$$

Here, ε is the excited energy level, m^* is the tunnel effective mass and x_1 and x_2 are the classical turning points

$$x_{1,2} = \frac{1}{2}\frac{W_t - \varepsilon}{eF}\left[1 \mp \left(\frac{eF}{\pi\varepsilon\varepsilon_\infty(W_t-\varepsilon)^2}\right)^{1/2}\right] \tag{16}$$

Electron tunneling is treated here by the semiclassical approximation and the integral over x can be expressed by elliptic integrals. Following Makkram-Ebeid and Lannoo [78], it was assumed that the empty trap is neutral and is a sort of an 'oscillator' or a 'core' embedded in the nitride lattice, which can attract the electron (the electron trap) or the hole (the hole trap). The trap is completely defined by the phonon energy $W_{ph} = \hbar\omega$, the thermal energy W_T, and the optical ionization energy W_{opt}. In the external field, the trap can decay into the empty 'core' and the free carrier (ionization process), so that the sum of their energies is equal to the initial energy of the filled trap. Usually, after the ionization process the final state of the 'core' is in the excited state and this excess energy induces other lattice vibration modes. The quantum theory [78] of this kind of trap gives the following equation for the rate of the trap ionization

$$P = \sum_{n=-\infty}^{+\infty} \exp\left[\frac{nW_{ph}}{2kT} - S\coth\frac{W_{ph}}{2kT}\right] I_n\left(\frac{S}{\sinh(W_{ph}/2kT)}\right) P_i(W_T + nW_{ph})$$

$$P_i(W) = \frac{eF}{2\sqrt{2m^*W}}\exp\left(-\frac{4}{3}\frac{\sqrt{2m}}{\hbar eF}W^{3/2}\right) \qquad S = \frac{W_{opt} - W_T}{W_{ph}} \tag{17}$$

where I_n is the modified Bessel function and the value $P_i(W)$ stands for the tunnel escape rate through the triangular barrier of W height.

Experiments [68] were performed with thick (530 Å) nitride films (0.1 DCS/ammonia gas ratio, 760°C). The current dependence on temperature and voltage were measured for both bias polarities. The current–temperature characteristics are shown in Figure 6.13 in

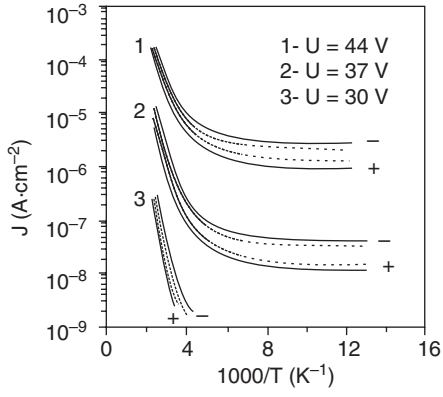

Figure 6.13 Current–temperature characteristics of MNOS at different applied voltages. Experimental data are presented by dots and theoretical results are shown by solid curves. Signs (+) and (−) correspond to the positive and negative polarities of applied voltages on the gate, respectively. MNOS geometry: tunnel oxide thickness $d_{ox} = 1.8$ nm, nitride thickness $d_N = 53$ nm (Reprinted with permission from [63], Copyright (2006) American Institute of Physics)

log J–T^{-1} coordinates. The current is approximately constant for temperatures below 200 K and rapidly increases for $T > 200$ K.

The experimental data were first fitted using the modified (including TAT) Frenkel model. The trap energy, $W_t = 1.2$ eV and equal electron and hole trap density $N_t = 7 \times 10^{19}$ cm^3 follows from the approximation of the high-temperature regions of Figure 6.13.

However, an extremely low attempt-to-escape frequency, $\nu = 6 \times 10^6$ s^{-1}, was obtained, in contradiction with the original paper by Frenkel where this value was estimated as $\nu \simeq W_t/h \simeq 10^{15}$ s^{-1} [76]. Previously, attempt-to-escape frequencies in the range $\nu = 10^6$–10^9 s^{-1} were reported for the Frenkel effect in Si_3N_4 [63]. Fitting the current values in the low-temperature data allows one to determine the effective tunnel mass. The calculated tunnel mass is different for different curves ($m_e^* = m_h^* = 4.8\ m_e$ for $V = 44$ V, $3.8\ m_e$ for $V = 37$ V, and $2.0\ m_e$ for $V = 30$ V). In all cases the calculated values are an order of magnitude higher than the known 0.3–0.6 m_e values for electrons and holes in SiN_x [80]. This means that, despite the fact that the Frenkel model formally describes the electron and hole transport in SiN_x, it leads to low, nonphysical attempt-to-escape frequencies and enormously large values of the effective tunnel mass.

Fitting the experimental data with the phonon-assisted trap ionization model allowes one to obtain reasonable parameters W_{opt}, W_T, W_{ph}, for fixed values of the tunnel effective masses $m_e^* = m_h^* = 0.5\, m_0$. The simulated current–temperature characteristics (Figure 6.13) quantitatively describe experiments for the following trap parameters: $W_{opt} = 2.8$ eV, $W_T = 1.4$ eV, $W_{ph} = 60$ meV. The current–voltage characteristics for both polarities on the gate electrode are presented in Figure 6.14. Agreement with the experiment data is achieved with the same trap parameters that were used in $I(T)$ calculations. It is important to note that the best fit of experimental $I(T,V)$ was achieved with equal densities, cross-sections, optical and thermal energies of electron and hole traps, and equal tunnel effective masses of electrons and holes. This is consistent with previously reported results for CVD nitrides [81].

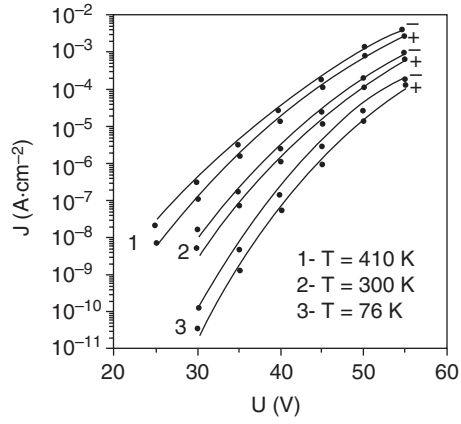

Figure 6.14 Current–voltage characteristics of MNOS at different temperatures (Reprinted with permission from [63], Copyright (2006) American Institute of Physics)

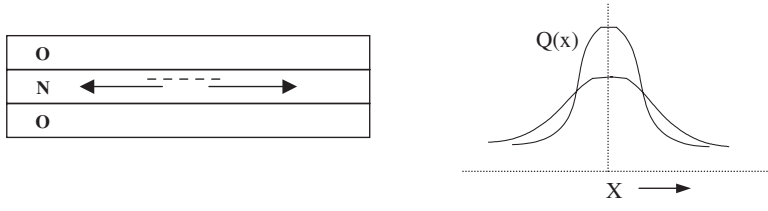

Figure 6.15 Lateral spread of charge locally stored in silicon nitride. The peak value of the Gaussian distribution decreases as a result of lateral diffusion

The phonon energy, $W_{ph} = 60\,\text{meV}$, obtained by simulations coincides with the phonon energy in $a\text{-}Si_{1-x}N_x{:}H$ films measured by Raman spectroscopy. This suggests that complexes of Si–Si bonds may play a role of electron and hole traps in silicon nitride.

Lateral (parallel to the substrate) conductivity in silicon nitride films of ONO structures was investigated in local storage SONOS memories (NROM) with thick BOX [82, 83] (Figure 6.15). A confined ($\Delta l \sim 400\,\text{Å}$ width) package of electrons was trapped in the nitride film (programing of NROM cells is discussed in the next paragraph). The solution of the diffusion equation (limited source) for lateral electron spread in nitride yields, for the charge density in the direction of the channel:

$$Q = Q_0/(\pi Dt + A)^{1/2} \exp\left[-x^2/(4Dt + A_1)\right] \qquad [Q_0]\text{C}\cdot\text{cm}^{-1}, \tag{18}$$

where A and A_1 are constants depicting the initial distribution of the trapped charge.

This predicts a $V_t(t)$ dependency of the form:

$$(V_t(t) - V_0)^{-2} \sim (\Delta V/\Delta l)^2\, \pi Dt\,, \tag{19}$$

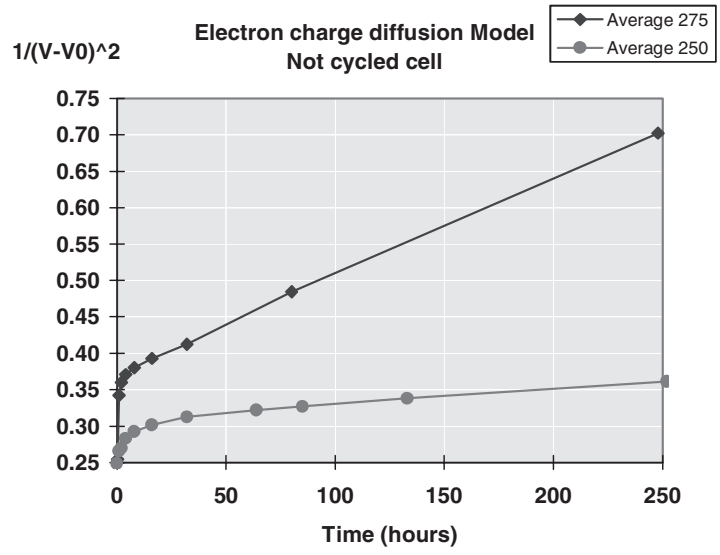

Figure 6.16 Relaxation of the memory cell threshold voltage after local trapping of electrons in the nitride layer of ONO

where the diffusion coefficient D is a function of the trap activation energy Φ, and $D = D_0 \exp(-\Phi/kT)$ with $D_0 \sim 1/4\nu N_t^{-2/3}$ (if one considers retrapping of the thermally excited electrons by the nearest deep traps, so that one diffusion step corresponds to the mean distance between the traps). V_0 is the memory transistor threshold voltage before programing (no charge in ONO). Figure 6.16 shows retention plots in $(V_t(t) - V_0)^{-2}$ vs t coordinates at 275°C and 250°C. There is good agreement between the experimental data with the lateral electron charge diffusion model for large times. The activation energy of traps is $\Phi_e = 1.7 - 1.8$ eV. The attempt-to-escape frequency calculated for $N_t = 3 \times 10^{19}\,cm^{-3}$ is of the order of 10^{11}–$10^{12}\,s^{-1}$. The initial 'fast' relaxation region is connected with Coulomb repulsion of trapped electrons and corresponding barrier lowering. The results of measurements at several temperatures (up to 300°C) imply that the energy peak of deep traps is well defined.

Similar data were obtained for the spread of trapped holes. Holes were injected into the silicon nitride in the erase operation. Gate induced leakage current I_{GIDL} in the drain junction that depends on the trapped hole charge, was used as the monitor. The value of voltage V_{tunn} corresponding to a given increment of I_{GIDL} was a measure of hole charge (V_t cannot be used as a monitor in this case because local V_t is below the initial V_0). The simple formula (Equation 18) derived above for electron lateral migration is also applicable for the thermally activated migration of holes. The obtained hole activation energy is $\Phi_h \sim 1.6$ eV.

A limited amount of trapped holes with very low activation energy (<0.3 eV) was also found in experiments with local storage (NROM) SONOS devices [41, 84]. An additional component of lateral conductivity immediately after the erase operation was observed. Hole conductivity connected with shallow traps was further confirmed in other experiments where holes were injected from a polysilicon electrode that was in direct contact with the nitride of ONO at the edge of the memory cell, and spread to the region with trapped

electrons. Closely located neutral Si–Si bonds or Si dangling bonds can be responsible for shallow traps.

6.6 DEVICE APPLICATIONS OF ONO STRUCTURES

The first metal–nitride–oxide semiconductor (MNOS) nonvolatile semiconductor memory (NVSM) device was developed in 1967 [85]. Since then, a variety of structures employing the same main principle, storage of charge in the nitride layer, have been proposed. Two main concepts are employed in state of the art nitride memories. We will call devices with thin BOX 'traditional' SONOS to distinguish them from NROM. In both approaches, the memory cell is a MOS transistor, with V_t dependent on the amount of charge placed into the nitride layer of the ONO dielectric.

6.6.1 Traditional SONOS

In 'traditional' SONOS* memories, the BOX is so thin that it allows uniform tunneling from the Si substrate over the entire channel. The abbreviation SONOS is used in the USA and Europe, Japanese and Korean authors more often employ the term MONOS. Depending on the gate polarity, charge carriers can be injected into the nitride, as shown in Figure 6.17(a). Injection of electrons corresponds to a V_t increase, whereas injection of holes and back-tunneling of electrons correspond to a V_t decrease.

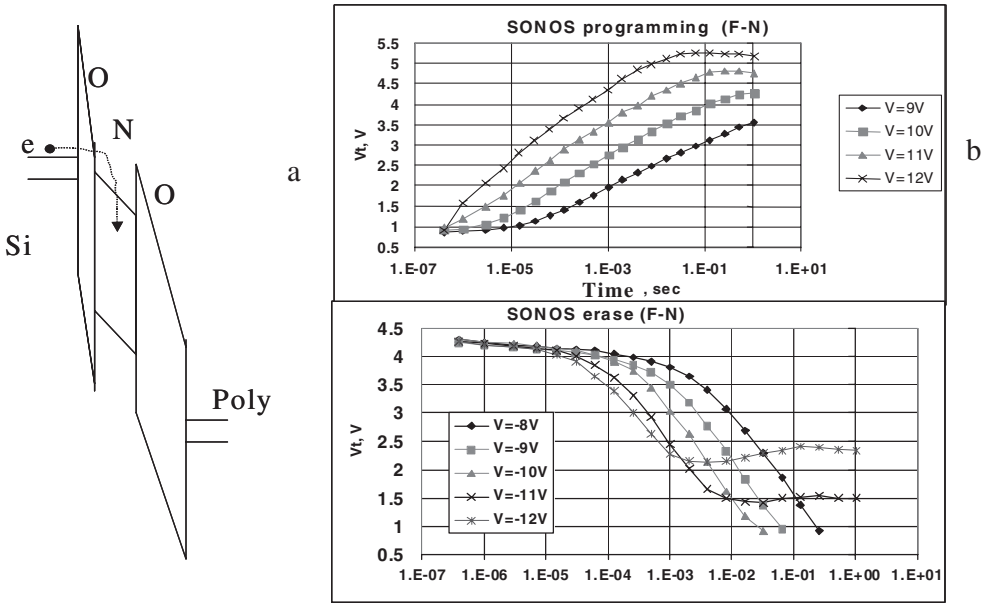

Figure 6.17 (a) Band diagram of the SONOS structure in the programming regime; (b) V_t as a function of program/erase time (20/60/55 Å). The devices were fabricated using Tower Semiconductor *micro*Flash 0.5 um technology

In typical operating regimes the tunneling barrier is composed of the BOX layer and part of the nitride layer. For large programing/erase voltages electrons are injected directly into the conduction band of the silicon nitride.

SONOS devices (with blocking TOX) are advantageous over older generations of MNOS memories because: (i) thickness of the nitride layer can be significantly scaled down (in MNOS devices it was limited to several hundreds of angstroms due to direct leakage of injected charge carriers into the gate electrode); (ii) injection from the gate electrode is strongly suppressed by significantly higher barriers of SiO_2 for electron and holes; (iii) retention is improved due to blocking of the leakage path of trapped electrons to the gate electrode. Smaller EOT of ONO is necessary to suppress short channel effects (SCE) in memory transistors. Smaller ONO thickness also allows lower voltages in program/erase operations. The minimum reported ONO EOT in SONOS devices is ~70 Å (30 Å/40 Å/20 Å) [86].

Traditional SONOS devices are very sensitive to the BOX thickness. Optimization of BOX is of principal importance because direct tunneling is used for programing/erase. There is a tradeoff between retention of the SONOS memory and programing/erase parameters. For example, the memory window is reduced 50% if the bottom oxide thickness is increased from 20 to 25 Å [87]. Thicker BOX shows better retention, but higher voltages or/and programing/erase times are needed in its operation.

SONOS devices programed and erased by F–N injection currents have very high endurance (number of program/erase cycles above 10^7), but limited retention and strong read disturb (increase of V_t in the course of read operation when voltage between V_t and $V_t + W$ is applied to the gate electrode).

Figure 6.18 shows the retention loss after a 250°C/24 h bake for SONOS capacitors with a 55 Å nitride layer and different thickness of BOX and TOX. Enhancement of

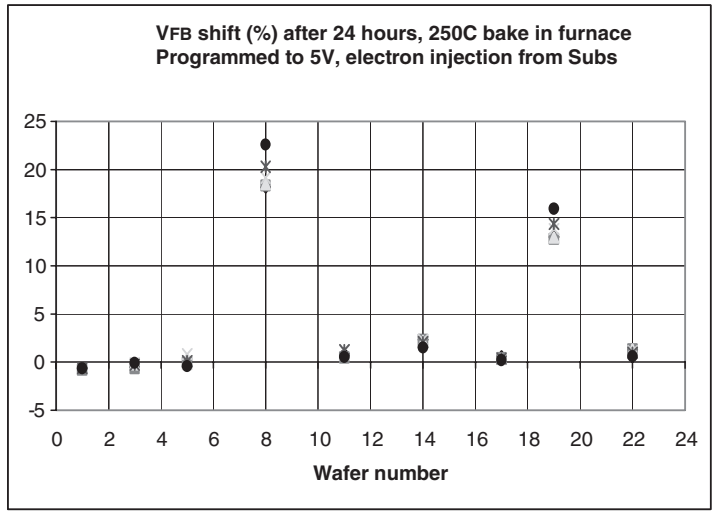

Figure 6.18 Retention loss (% of 3.5 V program window). Nitride thickness 55 Å for all splits

Waf #	1	3	5	8	11	14	17	19	22
BOX	64	55	44	29	64	64	64	29	44
TOX	90	90	90	90	38	50	59	38	50

high-temperature retention loss is manifested starting with the BOX thickness below 30 Å.

The temperature dependence of retention loss starts to be pronounced for temperatures above 100°C [87]. For lower temperatures, the tunnel component in the depolarization current dominates. SONOS devices with thin BOX can retain data for tens of years at room temperature, but retention at higher temperatures is problematic. Electrical fields above 8 MV/cm in the BOX are needed for programing/erase. With a EOT ~100 Å device, programing/erase voltages and times are of the order 10 V and tens of milliseconds, respectively (Figure 6.17b).

For large numbers of programing/erase cycles performed with single pulses, a shift of the memory window to higher voltages is observed. It is usually related to the increase of the memory transistor subthreshold swing: (i) generation of surface states; (ii) mobility degradation at the $Si–SiO_2$ interface. Additional surface states also stimulate enhanced back-tunneling of the trapped charge. Surface nitridation or substitution of hydrogen bonds with deuterium improve the stability of the $Si–SiO_2$ interface [88].

Another critical phenomena in SONOS memories that strongly depends on the BOX thickness is 'erase saturation'. Attempts to increase the BOX thickness in order to improve retention at the expense of higher negative gate voltage V_g in erase fail because of electron injection from the gate electrode through the TOX layer. The effect is especially pronounced in the end of the erasing operation (Figure 6.17b, erase voltages −11 and −12 V). Erase saturation also limits endurance/retention of SONOS devices. Increasing the erase time to compensate for parasitic injection from the gate results in $Si–SiO_2$ interface degradation. Several solutions were proposed to decrease erase saturation, including utilization of P^+ poly gate and high-*k* top oxides [87, 89].

Utilization of an alternative erase scheme that employs hot holes (similar to the one used in NROM) is discussed in Section 6.6.2. The optimum BOX thickness that accounts for the discussed tradeoff between program-erase performance and reliability varies between 18 and 25 Å. One of the reasons for the different values of BOX optimum thickness is nitridation of bottom oxide discussed in 2.2–2.3.

Traditional SONOS devices are subject to overerase (as in the floating gate EEPROM memories, the overerased cell shunts two bit lines in the NOR memory array). Thus, most designs employ SONOS transistors in series with a MOS transistor [90]. Scaling of SONOS transistor channel length is difficult because of ONO thickness limitations. Large EOT results in large SCE (drain leakage) while thin BOX and TOX do not ensure sufficient retention. Nevertheless, new types of SONOS devices were proposed where relatively large EOT can be used: (i) SONOS transistor on fully depleted SOI (silicon on insulator); and (ii) SONOS FinFET transistors [1, 88, 89, 91, 92]. In the latter case the SONOS transistor is a three-dimensional device with a vertical narrow (sub −100 Å) Si plate resembling a shark's fin. The fin is covered with ONO and wrapped with the gate electrode. Very thin Si bodies both in SOI and FinFET transistors allow one to suppress the SCE, even with ONO thickness of the order of 100 Å and above. Though deeply scaled-down SONOS transistors use uniform programming, lateral spread effects discussed in Section 6.5 are also significant. Due to scaling of device sizes, the stored charge (less than 100 electrons in ultra-small SONOS transistors) is located very close to the transistor edges where leakage paths (traps created during wafer processing as a result of plasma-induced damage) are probable. This is considered the root cause of insufficient retention in deeply scaled SONOS transistors [93].

6.6.2 NROM memories

Nonvolatile memory devices based on the NROM principle store information as electron charge in the nitride layer at the edges of a SONOS transistor (Figure 6.19a). They are programmed by channel hot electrons (CHE) and erased by hot holes generated in the drain region of the transistor by band-to-band tunneling (BBT) and then accelerated by the lateral field. It is possible to program and erase both sides of the transistor channel, and thus have two memory bits in one transistor. The read-out is performed in the direction opposite to the direction of programing. Both memory arrays without special dielectric isolation between the memory cells (field-less arrays) and arrays with STI (shallow trench isolation) can work on this principle. A typical field-less array is shown in Figure 6.19(b). It consists of diffusion N^+-doped bit lines (BL) and word lines in a cross-wise pattern. The polysilicon word line is isolated from the BL by a thick (~500 Å) bit line oxide. Mechanisms of programing and erase are illustrated in Figure 6.20(a,b).

The first NROM technology was *micro*FLASH®, developed by Tower Semiconductor Ltd. It offers the smallest Flash memory cell size in the industry combined with excellent

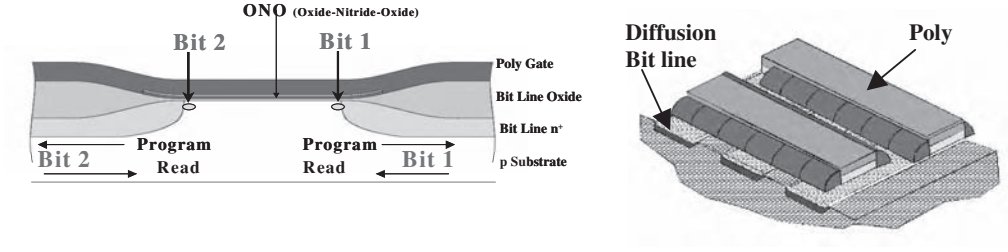

Figure 6.19 (a) Cross-section of an NROM memory cell; (b) schematic view of the memory array

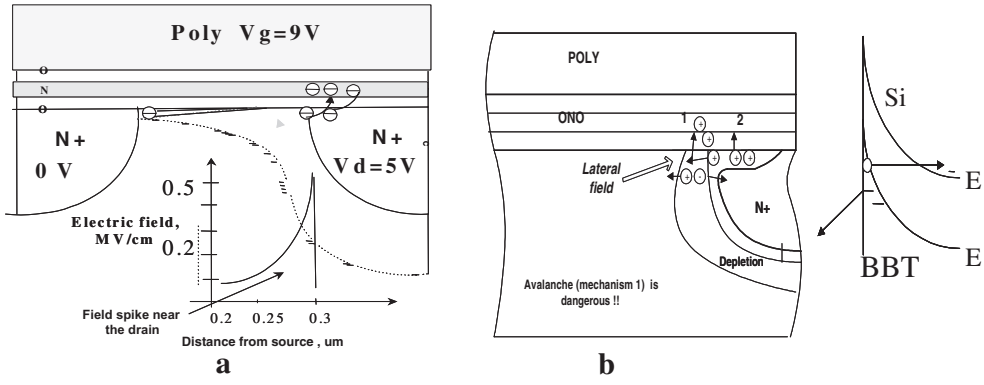

Figure 6.20 Programing and erase of NROm memory cell. (a). CHE are generated in the drain field spike, 'lucky' electrons get energy above 3.1 eV ($Si–SiO_2$ barrier) and are injected into ONO; (b) Holes are generated due to BBT in N^+ region and are accelerated by lateral field (move in the direction inside the channel). Some of holes overcome the Si–SiO2 barrier and are trapped in ONO. Erase regime: $V_g \sim -5$ V, $V_d \sim 5$ V, $V_s > 0$ to avoid punch-through [100] (Copyright 2005 IEEE)

reliability. This type of memory is now produced by different vendors under such brand names as MirrorBit™ (Spansion), NROM™ (Saifun), Nbit™ (Macronix), and TwinFlash™ (Infineon). The new memories are free of the main traditional SONOS limitations, such as poor retention and high read disturbs (parasitic programing typical of SONOS with thin BOX). NROM memories have high yield and are superior to EEPROMs with polysilicon floating gates because they do not suffer from stress-induced leakage current (SILC) channels in the BOX.

Fitting the measured NROM parameters (V_t, $I_d(V_g)$ subthreshold slope, I_{GIDL}) for different levels of programing in standard conditions (ONO 70 Å/60 Å/100 Å; $V_g \sim 9$ V, $V_d \sim 5$ V, effective channel length $L_{eff} \sim 0.3$ um) allows one to obtain information on the locally trapped charge $Q(x)$ [94]. The length of the electron packet stored in nitride at the drain N^+–p junction edge is ~400 Å. Approximately 700 electrons are trapped in one bit of the cell programed to $V_o + 2.5$ V with a Poly word line width of 0.18 um. About half of this packet length is over the drain of the SONOS transistor. The peak value of the $Q(x)/e$ distribution is of the order of 2×10^{13} cm^{-2} for the program window $W = 2$ V. Taking into account that the memory traps are distributed in the top half of the nitride layer (see Section 6.2.3), the concentration of trap is of the order of 10^{20} cm^{-3}. Nevertheless, very high retention is observed [82, 83], confirming the absence of hopping between closely located deep traps in nitride.

In contrast with traditional SONOS, NROM memories employ thick BOX. Lateral spread of electrons is the dominant retention loss mechanism of the OTP (one-time programed) products. V_t decrease remains much less than the program margin, even after 300°C anneals performed for hundreds of hours [84]. This is the best retention known for reprogramable nonvolatile memories. For cycled NROM devices, the increase of the erased state V_t with time and additional V_t loss of the programed state are registered. In contrast with 'traditional' SONOS, in the NROM cells electrons and holes are trapped in different locations in ONO. Some of the electrons are trapped far from the drain edge in the channel direction. More holes in erase are needed to compensate the electric field of these electrons. One has to increase the amplitude of erase pulses or erase time to bring the memory cell to the target V_t. Several mechanisms can contribute to electron charge accumulation far from the drain, including: (i) wide distribution of primary CHE; (ii) trapping of secondary electrons [95]; (iii) 'electron droplets' created during thermalization of electrons injected into silicon nitride [96]; (iv) in-process UV charging (in the field-less array geometry shown in Figure 6.20, electrons excited from Si and Poly by ultraviolet photons are trapped in the nitride of ONO at the edges of the word line [97]). As discussed in Section 6.5, some of the trapped silicon nitride holes have low activation energies and their migration results in V_t shifts. It has been shown [98] that up to 100–1000 program/erase cycles, the erased state V_t shift originates from the lateral motion of charges trapped in ONO. For larger numbers of cycles, injected holes result in ONO material degradation. In addition to lateral charge migration, V_t instabilities appear, originating from traps created by hot carriers in the bulk of ONO bottom oxide (BOX) and at the BOX–Si interface. Charge pumping measurements performed in combination with device simulations allow one to estimate the density of interface traps and the width of the region with generated traps [84, 99]. This width (from the drain metallurgical junction in the channel direction) increases from ~200 Å at the beginning of cycling to ~500 Å after 100 000 cycles (memory window $W = 1.6$ V, the cells were erased to the initial V_t). The density of

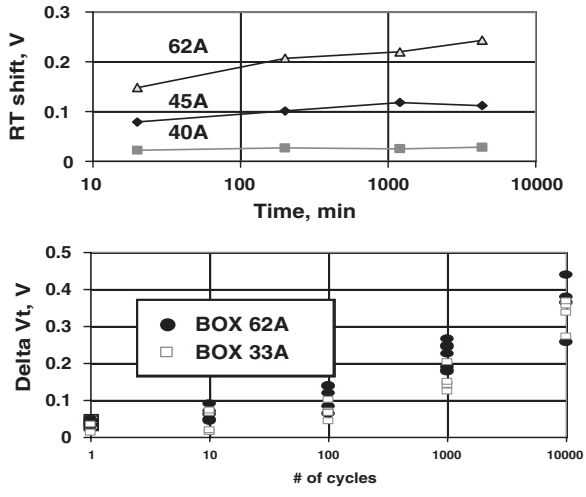

Figure 6.21 (a) RT shift (increase of the erased cell V_t of the cycled cell) vs time for different BOX thickness after 100 program/erase cycles; (b) retention after cycling for BOX thickness 33 and 62 Å. Total EOT is 190 Å for all specimens. L_{eff}/W = 0.3/0.35 um. 0.5 um *micro*Flash technology [100] (Copyright 2005 IEEE)

traps reaches ~10^{12} cm^2 eV^{-1} after 100 000 cycles and is correlated with generation of traps in the BOX.

A breakthrough improvement in the V_t shift was observed when scaling down the thickness of the ONO BOX to less than 50 Å [100] (Figure 6.21). We argue that the reason for the improvement is better alignment of electrons and holes in ONO in programing/erase operations and stronger *in situ* nitridation of the BOX.

STI (shallow trench) isolation and CMOS transistor geometry can be advantageous for scaled-down NROM memory arrays [101]. In this case narrow channel effects, in particular the above-mentioned in-process edge charging can be suppressed. Recently reported 110 nm NROM technology [102] with STI allows one to obtain record memory bit size of 0.043 um^2 and create up to 2 Gbit NOR memories suitable both for code and data storage (data storage at present is the prerogative of NAND poly floating gate EEPROMs).

Though high endurance is often considered an advantage of traditional SONOS over NROM, we demonstrated a 10^7 cycles endurance for NROM cells with BOX scaled down to ~30 Å [103]. A F–N 'refresh' (negative voltage at the gate) to remove the electrons trapped far from the drain was automatically done when V_d in erase reached a defined limit (the *micro*Flash product algorithm increases V_d in order to reach the target V_t in the erase operation).

There is a competition between deeply scaled 'traditional' SONOS (FinFET, SOI) with NROM, for memory density (area per bit). Modified 'traditional' SONOS also uses BBT (band-to-band tunneling) holes for erase (to avoid erase saturation [89]). This becomes possible due to very short channel lengths. Thicker BOX are allowed in this case and enhanced retention can be achieved. For large numbers of program/erase cycles, stability of ONO materials becomes the main endurance/retention limitation both for traditional and

NROM solutions. Read disturb (parasitic programing in the read operation) is still a problem for traditional SONOS, even for BOX thickness of the order of 30 Å.

6.6.3 High-*k* dielectrics in SONOS memories

The electric field in the TOX of SONOS is about twice as large as in nitride. Therefore, for scaled SONOS device with comparable thickness of nitride and SiO_2 top oxide, a significant part of the applied voltage drops on the top oxide during write/erase operations. Replacement of TOX with high-*k* dielectric allows for lower operation voltages and has several additional advantages [104, 105].

Simulations of write/erase processes in SONOS, with Al_2O_3 and ZrO_2 as top oxides, were performed [104]. A one-dimensional two-band model of charge transport was employed [63]. Both the tunnel (Fowler–Nordheim) and thermally assisted tunnel currents through the Si/SiO_2 and high-*k*/Poly interfaces were considered. Figure 6.22(a–c) shows the energy diagrams of SONOS with SiO_2, Al_2O_3, and ZrO_2 as top blocking dielectrics, respectively. For SONOS with Al_2O_3 we used the Si/Al_2O_3 electron barrier of 2.1 eV [106]. A bandgap of 8.0 eV was taken for Al_2O_3, so that the hole barrier at the Si/Al_2O_3 interface should be 4.8 eV. The electron barrier at the Si/ZrO_2 interface was 2.0 eV [106]. The bandgap of ZrO_2 is equal to 5.5 eV and, therefore, a hole barrier of 2.4 eV is obtained. The silicon nitride layer parameters were obtained by fitting the data for ONO with SiO_2 top oxide to the developed charge transport model [104]. Write/erase characteristics for SONOS with top Al_2O_3 and ZrO_2 are shown in Figure 6.23(a,b). For the same applied voltages, the program/erase time is less and the memory window is larger, in the case of Al_2O_3, than for SONOS with a top SiO_2. The same program/erase times can be obtained for smaller program/erase voltages (+9/−8 V, in the case of Al_2O_3, and +7/−6 V in case of ZrO_2) compared with +10/−9 V of the SONOS stack with top SiO_2 of the same thickness.

The peculiarities of the band diagrams for SONOS with a high-*k* top dielectric (ZrO_2) are demonstrated in Figure 6.24. The electric field is enhanced in the BOX and decreases in the top high-*k* dielectric, resulting in a decrease of parasitic injection from the gate.

The following advantages of SONOS with high-*k* dielectric as the top oxide, compared with the conventional SONOS devices, can be distinguished:

1. Lower EOT of ONO allows designing of transistors with smaller L_{eff}.
2. Program/erase speed can be higher at the same operation voltage.
3. The top high-*k* dielectric suppresses electron injection from the polysilicon gate, thus drastically eliminating the erase saturation phenomena.
4. For a fixed length of write/erase pulses, the high-*k* top dielectric allows thicker bottom SiO_2 layer, and thus higher retention.
5. Low operation voltages simplify CMOS peripheral circuits, which allows easier integration and decreased mask count.

A high-*k* top dielectric has an additional advantage in NROM memories. Electrons trapped far from the drain can be removed by the above-mentioned negative gate ‘refresh’ pulses for thicker BOX [103]. Holes injected from the substrate compensate the charge of

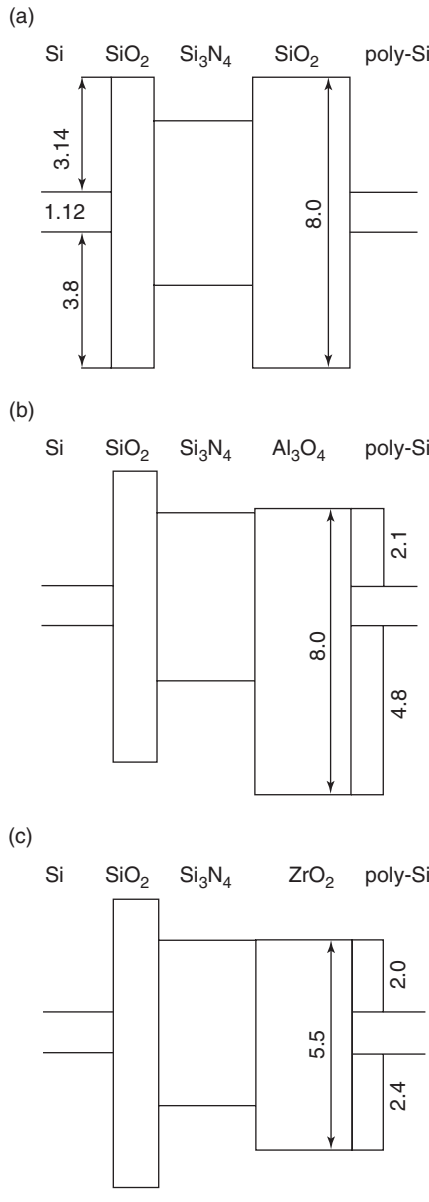

Figure 6.22 Energy diagrams of SONOS with: (a) SiO_2; (b) Al_2O_3; (c) ZrO_2 as top dielectric. Energies are shown in eV (Reprinted with permission from [104], Copyright (2003) Elsevier)

electrons trapped far from the drain. This significantly improves the endurance/retention of memories that use BBT hot holes for erase.

Implementation of high-*k* materials as ONO top dielectrics is not straightforward. Besides the process difficulties (contamination, complicated dry and wet etch, structural changes of high-*k* dielectrics in high-temperature processes), serious limitations arise as a result of

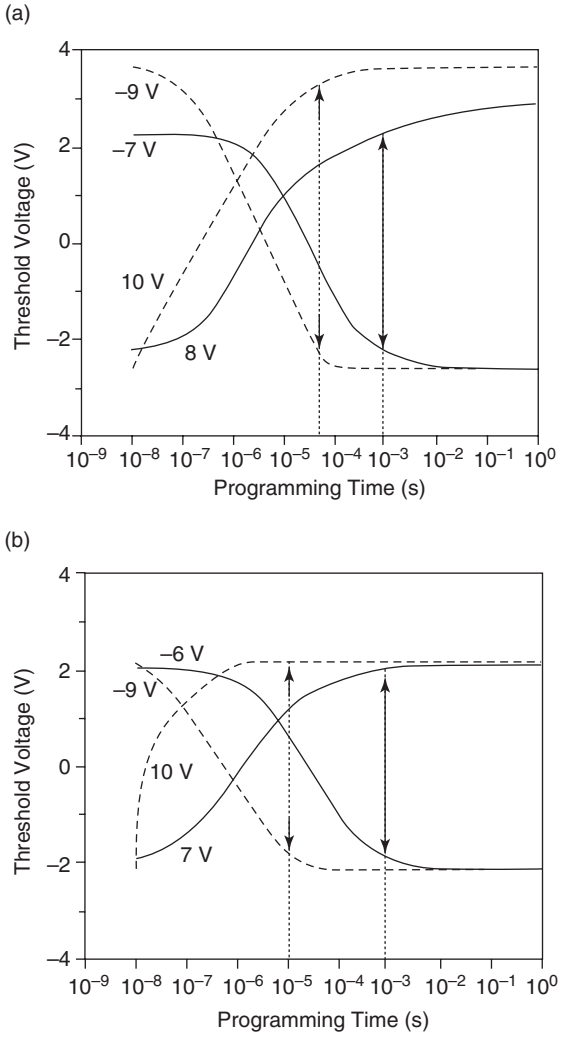

Figure 6.23 Write/erase characteristics of SONOS with different top dielectrics: (a) Al_2O_3; (b) ZrO_2. Simulations were performed for *W*/*E* voltages (+10/−9 V) (dashed lines) and for lower *W*/*E* voltages (solid lines). The last *W*/*E* voltages were chosen to get approximately 4 V memory window for pulse duration of 1 ms (solid arrow). The time position of dotted arrow shows the duration of (+10/−9 V) *W*/*E* pulse, when approximately the same memory window as in conventional SONOS with 55 Å top oxide is achieved. Parameters for simulation: $N_t = 5 \times 10^{19}\,cm^{-3}$, BOX 20 Å, nitride 45 Å, top oxide 55 Å. Hole tunnel mass in BOX $m_e^* = 0.43\,m_o$, electron tunnel mass in BOX $m_e^* = 0.5\,m_o^*$; electron and hole tunnel masses in Si_3N_4 and top oxides $m_e^* = m_h^* = 0.5\,m_o$. Electron and hole trap parameters in nitride are the same both for electron and hole. Capture and recombination cross-sections $\sigma = 5 \times 10^{-13}\,cm^2$; trap thermal energy $W_t = 1.8$ eV, trap optical energy $W_{opt} = 3.6$ eV, phonon energy $W_{ph} = 0.064$ eV (Reprinted with permission from [104], Copyright (2003) Elsevier)

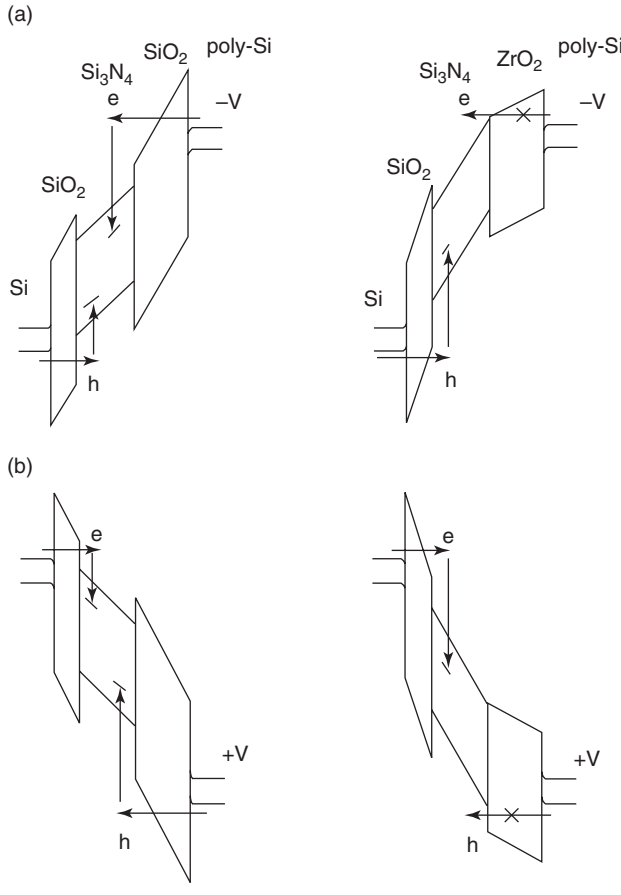

Figure 6.24 The schematic write/erase energy diagrams of SONOS structures with different top dielectrics: SiO_2 and ZrO_2. The arrows show injection of electrons or holes through the top and bottom dielectrics when the different applied voltage (+9/−8 V) are applied (Reprinted with permission from [104], Copyright (2003) Elsevier)

high trap densities in high-*k* materials. Trapping in the high-*k* layer leads to additional V_t instabilities (retention loss). Traps at the external surface of the high-*k* oxide also result in polysilicon Fermi level pinning [107]. This effect can be solved by using combinations of high-*k* with metal gates (as in the case when high-*k* materials are used as gate dielectrics in CMOS), but integration is more complicated and additional masks in the process flow are needed.

High-*k* materials were also tried as substitutes for the BOX or as a part of the BOX, and also as the trapping layer of ONO instead of nitride [108, 109]. Better injection efficiency, accompanied by high retention, was reported for high-*k* in the BOX stack (similar to the case when JVD trap-free silicon nitride is used as the BOX [108, 33]). A HfAlO trapping layer (OHO stack) demonstrated high-speed program/erase and good retention [109]. Nevertheless, large technological efforts are necessary to implement these challenging ideas into the memory products.

6.7 CONCLUSION

Modern technologies allow one to obtain high-quality ONO stacks for application in state-of-the-art nitride memories, in particular products based on the NROM principle.

The bottom oxide of device-quality ONO is a strongly nitrided oxide. This explains high reliability performance of memories that employ hot carriers for programing and erase. Trapping in ONO occurs in the silicon enriched oxynitride layer, located at the interface between nitride and top oxide. The density of deep traps with activation energies about 1.8 eV is of the order of $10^{20}\,cm^{-3}$. At present there is no consensus on the chemical nature of the deep trap. What is definitely known is that nitride traps are connected with excess silicon and their properties depend on the hydrogen content in the film. The traps are amphoteric (capture both electrons and holes). Several models that assume both negative and positive correlation energies, can explain the observed absence of ESR signals in nitride films, an issue that needs further research. Novel scenarios for nitride conductivity have been developed, in particular non-Frenkel vertical transport and lateral charge migration. The developed models are important for deeper insight into SONOS device operation and for adequate reliability prognosis.

Development of scaled-down (in particular, embedded) SONOS technologies featuring low-cost and high-endurance/retention performance is a complicated task. Low-thermal-budget ONO stacks with trapping and reliability parameters similar or superior to the existing high-thermal-budget analogs are strongly desirable. Besides developing low-thermal-budget stacks, increasing the immunity of ONO layers to hot carriers and implementing of high-*k* dielectrics as a part of ONO are challenging problems. Advanced ONO is the basis for the development of new memory products with low cost, ultra-high density, low operation voltages and enhanced endurance/retention.

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7 Material Engineering of High-*k* Gate Dielectrics

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7.1 INTRODUCTION

The scaling trend aggressively pushes the silicon process technology toward the introduction of new materials so as to overcome a number of challenges in miniaturization. Not only high-*k* dielectrics but also low-*k* dielectrics and strained silicon have been intensively investigated. Since the introduction of new materials necessarily changes process technology and equipment, material selection should be carefully made.

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Among high-*k* dielectric films reported in the literature, pure ZrO_2 was studied in an early stage of the research, but HfO_2-based materials such as pure HfO_2, $HfSiO_x$ or $HfAlO_x$, and their nitrides, are now generally accepted as viable candidates for the first high-*k* material introduced into industry. On the other hand, it has also been recognized that a number of challenges so far never encountered in scaled SiO_2-based CMOS technology are barriers to the introduction of these materials.

Figure 7.1 shows possible advantages and disadvantages of using high-*k* materials for CMOS gate dielectrics. Obstacles such as mobility degradation and threshold voltage instability are still issues, though significant improvements have been reported. The point is to differentiate between their intrinsic and extrinsic effects. It is worth noting that most of the big challenges come from fundamental properties of high-*k* materials. Namely, the ionic properties of the high-*k* films lead to a number of disadvantages as well as advantages for advanced CMOS application. The high-*k* dielectric permittivity is predominantly derived from the ionic part of the dielectric responses of those materials to an external field, while defects are intrinsically likely to exist in the ionic films. Fermi-level pinning may be also related to the ionic nature of high-*k* dielectrics.

Another point is that the high-*k* gate dielectric film will be used in the form of a nanometer-thick layer rather than a bulk material. No consensus has been reached whether there might be a difference between thin and thick films in terms of material properties. In addition, the film growth technique is much different from conventional Si oxidation in the furnace, where a good interface is naturally obtained at Si/SiO_2. So, the film growth mechanism and characteristics of high-*k* films should be carefully investigated. Furthermore, it should be mentioned that the high-*k* film is not a single layer, even in a simple high-*k* film, but consists of a stack of layers, with an interface low-*k* dielectric layer. Therefore, the interface layer quality and its formation process should be definitely clarified, because the interface layer cannot be ignored as it represents a further addition to the equivalent oxide thickness (*EOT*).

Higher-quality and/or higher-*k* dielectrics are inevitably desired for further scaling of CMOS devices. In fact, ternary oxides such as $HfSiO_x$ or $HfAlO_x$ are actively under inves-

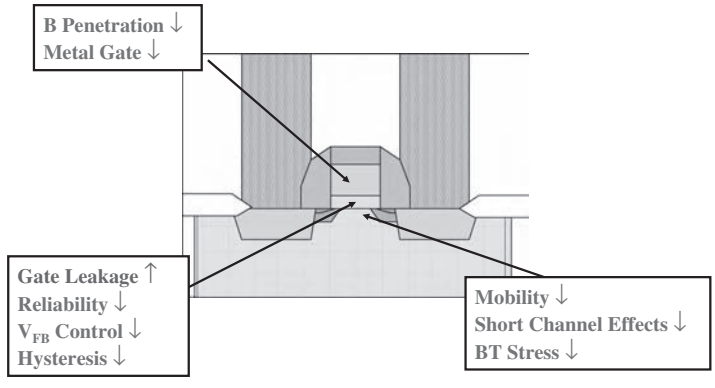

Figure 7.1 Possible advantages and disadvantages of employing high-*k* materials as the gate dielectrics. High-*k* dielectrics are beneficial for the gate leakage current reduction, but induce degradations of various device parameters at the same time

tigation, but they usually possess medium-*k* values. On the other hand, many higher-*k* materials have other challenges in terms of CMOS applicability, but will be important for achieving scaled CMOS as well as for understanding dielectric properties of existing high-*k* materials. Mechanisms for achieving amorphous high-*k* films are also important to investigate. Concerning high-*k* MOSFETs, mobility degradation and Fermi-level pinning are currently the most difficult issues to resolve. Both may be related to the bottom and top interfaces of high-*k* layers, respectively.

This chapter starts by describing the theoretical basis for understanding the fundamentals of the dielectric properties, and then discusses lattice vibration properties through far-infrared absorption studies. Interface layer formation in the Si/HfO_2 system and ternary higher-*k* materials, are discussed for further CMOS scaling, in which we will emphasize how to engineer high-*k* materials, focusing on HfO_2-based dielectric films.

A number of papers, including good review articles, have been published [1–5]. In this chapter, fundamental aspects of high-*k* gate dielectrics are mainly discussed, including the high-*k* film deposition technique, and the mobility discussion of high-*k* MOSFETs. High-*k* film reliability will not be discussed. Those who are interested in it can see references [6, 7].

7.2 DIELECTRIC PERMITTIVITY OF HIGH-*k* INSULATORS

The origin of the dielectric constant is simply reviewed to understand the high-*k* dielectric characteristics in this section.

7.2.1 General

The dielectric permittivity of a material is well understood from classical solid state physics [8]. Here let us briefly review the dielectric response to an electric field. We should first understand that the macroscopic polarization $\vec{P}$ is a volume addition of the microscopically induced polarization $\vec{m}$. By defining the local field $\vec{E}_i$, which works on the microscopic polarization,

$$\vec{P} = N_m \vec{m} = N_m \alpha_m \vec{E}_i \tag{1}$$

where α_m is the microscopic polarizability, N_m is a number density of microscopic polarization, and $\vec{E}_i$ is a local field.

On the other hand, the relative dielectric permittivity k is defined as follows, where $\vec{D}$ is an electric displacement vector.

$$\vec{D} = \vec{E} + 4\pi\vec{P} = k\vec{E}$$
$$\vec{P} = \frac{(k-1)}{4\pi}\vec{E} \tag{2}$$

Here, the difference between $\vec{E}_i$ in Equation (1) and $\vec{E}$ in Equation (2) should be noted.

The relationship between $\vec{E}$ and $\vec{E}_{\mathrm{i}}$ is usually described by the Lorentz field, as

$$\vec{E}_{\mathrm{i}} = \vec{E} + \frac{4\pi\vec{P}}{3} = \frac{\vec{E}}{3}(k+2) \tag{3}$$

This relationship is quite important for understanding what happens inside the dielectric materials. Thus,

$$\begin{aligned}\vec{P} &= \frac{(k-1)}{4\pi}\vec{E} = N_{\mathrm{m}}\alpha_{\mathrm{m}}\vec{E}_{\mathrm{i}} \\ &= N_{\mathrm{m}}\alpha_{\mathrm{m}}\left(\frac{k+2}{3}\right)\vec{E}\end{aligned} \tag{4}$$

From those equations, the following Clausius–Mossotti relation is obtained.

$$\frac{k-1}{k+2} = \frac{4\pi}{3}\frac{\alpha_{\mathrm{m}}}{V_{\mathrm{m}}} \tag{5}$$

Here, it should be remembered that the dielectric permittivity k is not linearly dependent on the molar polarizability, but that it is determined by both α_{m} and V_{m} (molar volume $1/V_{\mathrm{m}} = N_{\mathrm{m}}$). Thus, the Clausius–Mossotti relation associates microscopically defined polarizability α_{m} with the relative dielectric permittivity, k, defined macroscopically.

7.2.2 Microscopic polarization

Another important point to understand about dielectric properties is that there are microscopic origins of the polarizability of materials. These are typically the permanent, ionic and electronic polarizations. In high-k materials, it is assumed that there is no permanent polarization, but both ionic and electronic contributions should be considered.

First, let us discuss the ionic contribution to the microscopic polarization. For simplicity, suppose a two-atom system. The equation of motion of each atom with effective charge of Z^*e and mass of M^+ or M^-, as shown in Figure 7.2 is described under a certain electric field E as follows.

$$\begin{aligned}M^- \frac{\mathrm{d}^2}{\mathrm{d}t^2} X_{\mathrm{Q}}(t)^- &= -c\left(X_{\mathrm{Q}}(t)^- - X_{\mathrm{Q}}(t)^+\right) + q^- E \\ M^+ \frac{\mathrm{d}^2}{\mathrm{d}t^2} X_{\mathrm{Q}}(t)^+ &= -c\left(X_{\mathrm{Q}}(t)^+ - X_{\mathrm{Q}}(t)^-\right) + q^+ E \\ q^+ &= -q^- = Z^*e \\ p_{\mathrm{ion}} &= Z^*e\left(X_{\mathrm{Q}}(t)^+ - X_{\mathrm{Q}}(t)^-\right)\end{aligned} \tag{6}$$

$$M^* \frac{\mathrm{d}^2}{\mathrm{d}t^2} p_{\mathrm{ion}}(t) = -cp_{\mathrm{ion}}(t) + (Z^*e)^2 E \tag{7}$$

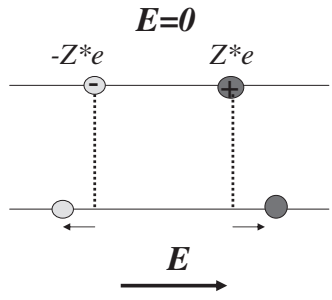

Figure 7.2 Schematic of the simple oscillator with two ions. The charges on the cation and the anion are Z^*e and $-Z^*e$, respectively. The distance between two atoms is forced to change by the applied electric field E, which induces an ionic polarization

Here, $c = M^*\omega_0^2$ and

$$\frac{1}{M^*} = \frac{1}{M^+} + \frac{1}{M^-}$$

In an equilibrium state,

$$\alpha_{\text{ion}} = \frac{(Z^*e)^2}{c} = \frac{(Z^*e)^2}{M^*\omega_0^2} \tag{8}$$

where c and M^* are force constant and reduced mass, respectively.

Thus, α_{ion} is determined by the effective charge Z^*e and the force constant c in the simplest case. This is actually too simple, but very useful for understanding and controlling the dielectric permittivity of high-k materials, as discussed in Section 7.7. Consequently, in simple ionic materials, the molar volume, the effective charge, and the force constant of ionic bonding determine the permittivity.

Infrared absorption studies are quite useful for studying ω_0. Particularly, the far-infrared absorption is a very powerful technique to investigate the softness or hardness of the bonding characteristics of relevant atoms, because typical high-k materials are heavy metal oxides and characteristic ionic vibration modes are in the far-infrared region.

Next, we consider the electronic contribution to the microscopic polarizability. This can be calculated by using second-order perturbation theory of quantum mechanics. First-order perturbation does not provide the electronic polarizability, because the polarization is linearly related to the distance and the integral should be zero. The second-order perturbation calculation gives us the polarizability as follows.

$$\begin{aligned} H' &= -\vec{p}\cdot\vec{E} \\ \varphi_m^1 &= \varphi_m^0 + \sum_{m'} \frac{\langle m'|p|m\rangle}{W_{m'} - W_m} E\varphi_m^0 \\ \alpha_e &= \sum_{m'} \frac{\langle 0|p|m'\rangle\langle m'|p|0\rangle + \langle 0|p|m'\rangle\langle m'|p|0\rangle}{W_{m'} - W_0} \end{aligned} \tag{9}$$

Here, H' is the perturbation Hamiltonian, φ^1 and φ^0 are the first and zeroth order wavefunctions of the system and α_e is the electronic polarizability.

For insulators or semiconductors, Equation (9) means that α_e is inversely proportional to the bandgap. This means that a larger bandgap implies a smaller α_e. In terms of the electronic device application of high-k films, higher-bandgap materials are desirable, but are inconsistent with a larger α_e. In high-k materials the ionic contribution is dominant compared with the electronic contribution. Thus, to achieve a higher polarizability, a larger α_e would be better, but from the viewpoint of high-k dielectric insulators for CMOS, higher α_{ion} and a smaller α_e are definitely better. As $k(\infty) = n^2$ is the well known Lorentz–Lorenz relation, the electronic contribution to the dielectric permittivity in a high-frequency region can be obtained by the optical refractive index n of a material. Finally, it should be mentioned that larger α_{ion} is often correlated to larger α_e [3].

7.3 LATTICE VIBRATION

From the viewpoint of the k value, both α_{ion} and V_m depend on the unit cell, determining the local ionic structure in the dielectrics. α_{ion} is more related to the lattice vibration, while V_m is determined by the lattice constant. Infrared (IR) absorption studies will be useful for studying the ionic bonding characteristics of the materials. In particular, far-infrared absorption studies are very informative of high-k material properties [9], since high-k materials are generally composed of heavy metal oxides, which have main absorption peaks in the far-infrared region [10, 11].

We have examined the IR absorption spectra of HfO_2 films on Si substrate. Since there is an interface layer (IL) between the HfO_2 film and the Si substrate, both absorption spectra are overlapped. Fortunately, we can differentiate one from the other in IR spectra, because the main contribution of each absorption is located in a different wavenumber region. The infrared absorption was measured by transmission mode FTIR (Fourier transform infrared) spectrometer with a range of wavenumber from 100 to 2000 cm^{-1}. The ATR (attenuated total reflection) method is often used for IR absorption study on thin SiO_2, but it is experimentally hard for the far-IR measurement. The far-IR measurement in the range 100–600 cm^{-1} was performed in vacuum, and the measured wavenumber overlaps in the range of 500–600 cm^{-1}, between the mid- and the far-infrared regions.

Figure 7.3 shows a comparison of the IR absorption spectra between HfO_2 and SiO_2 from 200 to 1400 cm^{-1} [12]. SiO_2 shows three dominant, well-known absorption peaks, while HfO_2 shows annealing-temperature-dependent absorption spectra. In the as-deposited HfO_2 sample, only a broad peak is observed in the far-infrared region, while in the annealed sample many peaks in the far-infrared region, and a small structure in the mid-infrared, are observed. It is necessary to take account of the fact that the HfO_2 spectra include underlying SiO_2 absorption peaks which are located around 1100, 800 and 450 cm^{-1}. As a whole, the relatively large 1100 cm^{-1} absorption peak is derived from the asymmetric stretching mode vibration of Si–O–Si, while the far-infrared peaks are composed of the vibration modes of the HfO_2 structure. Figure 7.4 shows XRD spectra of the same samples shown in Figure 7.3, but as a function of annealing temperature [13]. The as-deposited and 400°C annealed samples seem to be amorphous, while the annealed ones (above 600°C), clearly show the monoclinic structure, which is commonly reported for crystallized HfO_2 [14]. With the increase of annealing temperature, it is seen that the peak intensity becomes

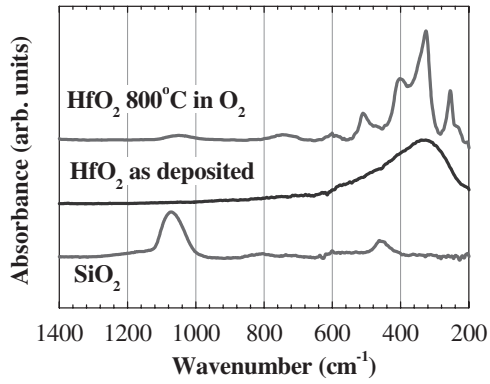

Figure 7.3 Comparison of IR absorption spectra between sputtered HfO_2 (30-nm-thick) and thermally grown SiO_2 (17-nm-thick) films. The SiO_2 film shows well-known peaks around 1100, 800 and 450 cm^{-1}. Characteristic peaks for HfO_2 mainly appear in the far-infrared region (200–600 cm^{-1}) after 800°C annealing, while only a broad peak is observed before annealing [12]

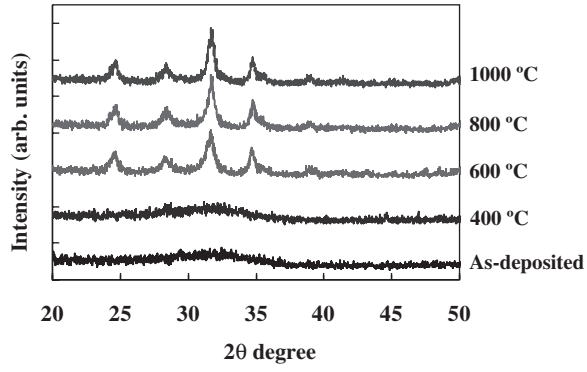

Figure 7.4 Change of XRD patterns of 30-nm-thick HfO_2 films by annealing at various temperatures. The film remains amorphous at 400°C, but crystallizes into the monoclinic phase above 600°C. The peak intensities do not increase significantly by higher-temperature annealing (>800°C), which suggests that the long-range ordering of the film does not change above 800°C [12]

sharper. Figure 7.5 focuses on the far-infrared region spectra of crystallized HfO_2 as a parameter of annealing temperature. With increase of annealing temperature, the peak-to-valley ratio also increases, even after the XRD intensity saturates. This fact implies that the local bonding arrangement increases, even after long-range ordering is attained. The main peak is centered at 320 cm^{-1}, and many peaks are clearly distinguishable in the far-infrared region. A theoretical calculation predicts that monoclinic HfO_2 has basically 15 infrared-active modes, including a few very small peaks [15], and we can assign 10 or 11 peaks for the monoclinic HfO_2 experimentally.

Figure 7.6 shows the IR absorption spectra of ultra-thin HfO_2 films. In addition to the fact that the absorption intensity absolutely decreases with decreasing thickness, it is observed that the absorption spectra shape also changes with thickness. This will be

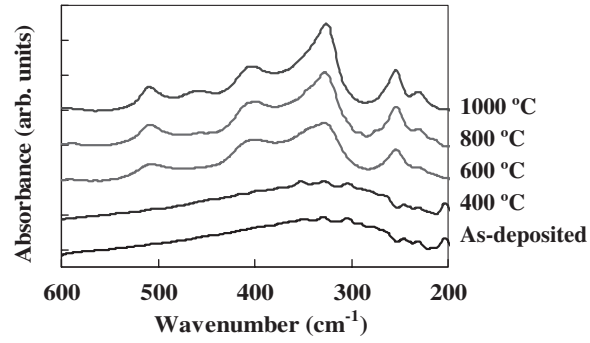

Figure 7.5 Change of far-IR absorption spectra of 30-nm-thick HfO_2 films by annealing at various temperatures. The characteristic peaks for HfO_2 are clearly observed in crystallized films (annealed at 600°C or higher temperature), while amorphous films (annealed at 400°C or lower temperature) show only a broad peak. The peaks observed for crystallized films are attributable to the lattice vibration of HfO_2 with the monoclinic structure [12]

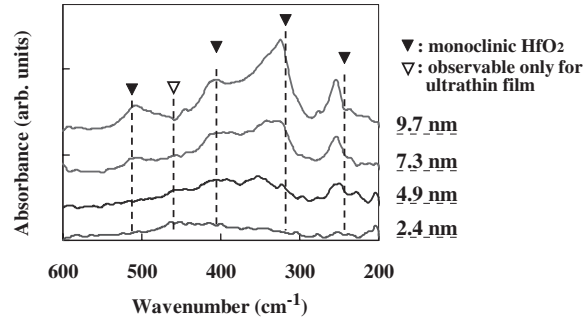

Figure 7.6 Far-IR absorption spectra of less-than-10 nm-thick HfO_2 films on Si, annealed at 1000°C in N_2 ambient. The ultra-thin films show not only the weaker absorption peaks, but also the spectra with different shape and different peak positions, probably because the Si diffusion from the Si substrate during annealing is more pronounced for ultra-thin films [13]

discussed in Section 7.7 in terms of the phase transformation of HfO_2 due to Si diffusion from the substrate. We should emphasize that the infrared-active mode is very sensitive to the crystal phase of HfO_2, as has been calculated [15, 16]. Thus, the far-infrared absorption result is informative for characterizing small changes in the bonding characteristics of high-k films.

These vibration modes contribute to the high dielectric permittivity value of HfO_2. The dielectric permittivity can be calculated through the Kramers–Kronig relation of absorption data, though a quantitative estimation is not straightforward. It is intuitively expected from the simple equation

$$\alpha_{\text{ion}} = \frac{(Z^*e)^2}{M^*\omega_0^2}$$

as discussed previously in Equation (8), that a low ω_0 phonon contribution to α_{ion} is significant.

Furthermore, it has been reported that those low-energy phonons observed in HfO_2 might be responsible for the poor high-k FET mobility, due to the remote optical phonon scattering [17]. Although the mobility degradation has not been understood clearly so far, significant roles of low-energy phonon modes should be taken into consideration for high-performance high-k CMOS from viewpoints of both the dielectric permittivity and the mobility analysis. The mobility is also discussed in Section 7.8.

7.4 ELECTRONIC STRUCTURE

High-k gate dielectrics are to be used for suppressing the intrinsic gate leakage current, and thus the electronic structure of dielectric films is critically important for characterizing the direct tunneling probability. A simple analysis in the first-order approximation shows that the direct tunneling current, J_{DT}, can be expressed as,

$$J_{DT} \propto \exp\left(-\frac{1}{\hbar}\sqrt{8m^*\Phi_b}T_{OX}\right) \tag{10}$$

in the very-low-field region, where Φ_b, m^* and T_{OX} are the energy band discontinuity against the gate electrode, the effective mass, and the physical oxide thickness, respectively.

Φ_b and m^* are substantially important, as well as the k value, in order to reduce the leakage current. The electronic energy structures of various high-k materials have been calculated, and compared with experimental results [18, 19]. The experimental bandgap and offset values are slightly different among various X-ray photoemission spectroscopy experiments [20] and the internal photoemission measurements [21]. A clear message from the calculation on transition metal oxides is a relatively low conduction band edge of the d-band states, schematically expressed in Figure 7.7 [22]. This is quite different from the cases of SiO_2 or Al_2O_3 without d-electrons. From the anion side, another important effect is that the valence band edge into high-k films is shifted upward with nitrogen introduction [23]. Thus, the bandgap of high-k films is significantly reduced to 3–6 eV, compared to ~9 eV for SiO_2.

Generally speaking, a larger bandgap causes a smaller $k(\infty)$, but $k(\infty)$ is not the main contributor to permittivity, as mentioned in Section 7.2. Thus, a smaller $k(\infty)$, namely a smaller n (optical refractive index), is better for obtaining the higher insulating barrier for the CMOS application. In addition, in the tunneling current calculation, m^* is not known at all. In any analysis, m^* is assumed to be a constant, independent of the dielectric material. In this chapter, further details of the electronic structure are not discussed, but their implications are briefly discussed.

In Equation (10) for J_{DT}, T_{OX} is the physical oxide thickness, and

$$T_{OX} = \frac{k}{k_{SiO_2}}\text{EOT} \tag{11}$$

by using the k value and EOT of high-k films, where EOT (equivalent oxide thickness) denotes the thickness capacitively equivalent to the SiO_2 thickness. Thus, it is understandable

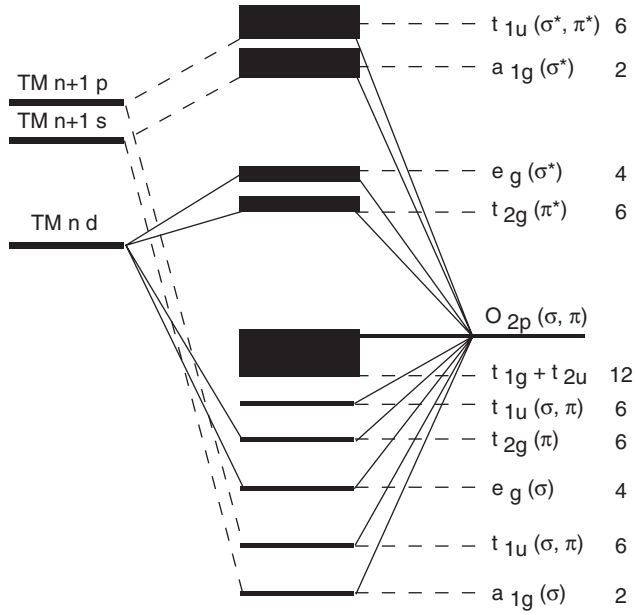

Figure 7.7 Schematic molecular orbital energy level diagram for a group IVB metal in an octahedral bonding arrangement with six oxygen neighbors. The top of the valence band is assigned to nonbonding π orbitals of oxygen atom p-states, and the first two conduction bands are associated with transition metal d-states [22]

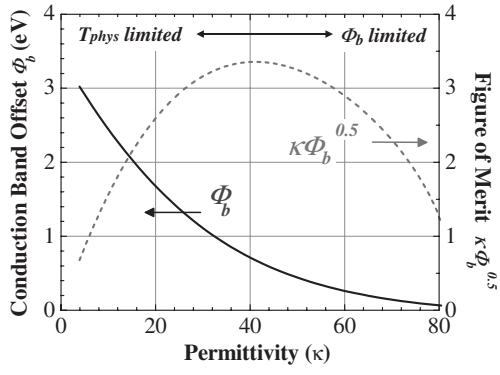

Figure 7.8 The relationship between the figure of merit ($k\Phi_b^{0.5}$) and k, estimated from the reported conduction band offset (Φ_b) values. Very-high-k will not be appropriate for Si-CMOS application, and medium-high-k will provide an optimum point

that $k\sqrt{m^*\Phi_b}$ is a figure of merit (FOM) for leakage current suppression at a certain EOT. Figure 7.8 shows the relationship between this FOM and the k value, where k and Φ_b are the values reported in the literature. It can be seen that a too-high-k value will not be appropriate for Si-CMOS application, but a medium-high-k will provide an optimum point. When the interface layer exists, it is not so simple to generalize the tunneling effect, but the

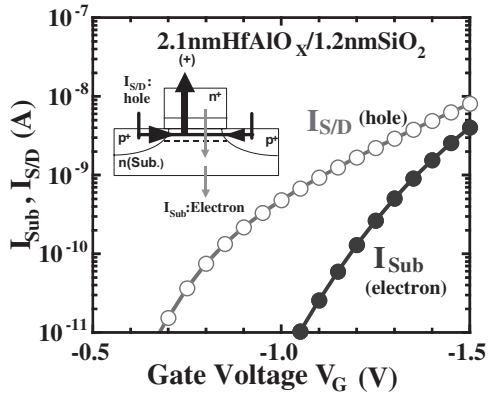

Figure 7.9 Carrier separation experiment in $HfAlO_x/SiO_2$ *p*-MOSFET. The hole current is larger than the electron one in the lower-bias region [25]

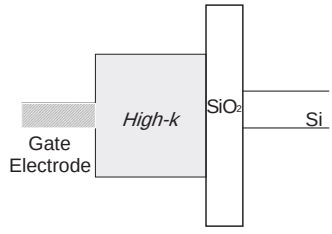

Figure 7.10 The realistic energy band structure of high-*k* MIS structure. The interface SiO_2 layer inevitably exists on Si substrate

basic trend will be true. The result in Figure 7.8 was obtained in the case of electron tunneling from the Si substrate to the gate electrode. In the case of electron tunneling from the gate electrode, the tunneling probability depends on the gate electrode metal work function as well. Furthermore, in the case of a gate dielectric film consisting of high-*k* and SiO_2 stack layers, it is easily expected that the electron tunneling probability from the Si substrate depends significantly on the interlayer thickness.

Next, the following two points should be mentioned in the leakage current analysis associated with the electronic structure of high-*k* materials.

1. We have focused on the conduction band offset (electron tunneling) so far, but it is not always true that electron tunneling is dominant compared with hole conduction. By using the carrier separation technique, we can differentiate the dominant carrier type between electrons and holes [25]. Figure 7.9 shows the results of the carrier separation in a $HfAlO_x$ film with EOT = 2 nm. Both electron and hole currents can be detected at the substrate and source and drain terminals. Also, attention should be paid to the interface layer at the Si substrate. Thus, the real energy structure should be described as shown in Figure 7.10. A sequential tunneling process is necessary to estimate the leakage current.

2. Concerning the leakage current analysis in high-*k* dielectric films, Pool–Frenkel-type conduction via defect sites in the film has often been reported from the temperature and electric field dependences of the leakage currents [26, 27]. Thus, note

that the leakage currents observed in the experiments are not always the pure direct-tunneling current.

7.5 HIGH-*k* FILM GROWTH

Many institutions have currently paid attention to atomic layer deposition (ALD) to grow ultra-thin high-*k* films with excellent uniformity and conformality, and without damage due to ion beams, for example. Physical vapor deposition processes such as sputtering or vacuum evaporation have been already well described in the litearture [28], and several review articles on ALD have been published [29, 30]; therefore, only the essential points of the ALD process are described here.

In the ALD process, the surface reaction is essential for the film growth; therefore, the initial surface condition sensitively affects the ALD film. Atomic layer deposition was introduced by T. Suntola and co-workers as *atomic layer epitaxy* in 1974 [29]. ALD is similar to chemical vapor deposition (CVD), but the reaction process is different from each other. In ALD, a surface is exposed alternately to two chemical precursors and the surface reaction is self-limited. Now research for many potential applications using ALD is underway [31].

Figure 7.11 shows that in the case of Al_2O_3 ALD, a clear growth delay (incubation time) is observed in the case of the film growth on Si, while on SiO_2 the film growth is linearly related to the deposition time without any growth delay. Figure 7.12 shows a schematic description of the Al_2O_3 ALD process, where H_2O is an oxidant gas. Usually, the ALD process is performed in the low-temperature, such as around 300°C, so residual impurities and defects left inside the films are great concerns in terms of the device reliability. Also, a densification treatment is usually required for ALD films. Therefore, the post-deposition annealing (PDA) is a key step for obtaining device-quality films. Impurities,

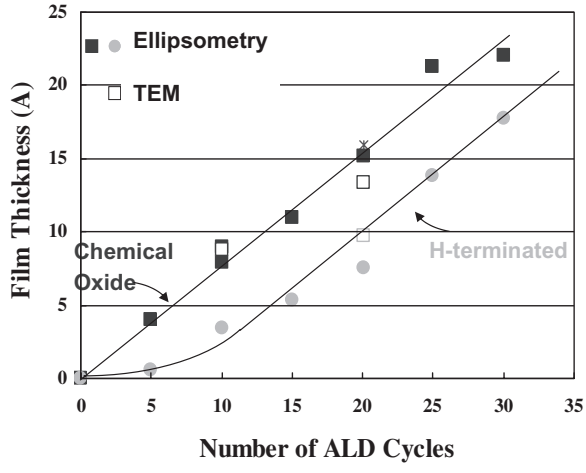

Figure 7.11 ALD-grown Al_2O_3 thickness both on chemically grown SiO_2 and on H-terminated Si surface. A clear growth delay is seen in the case of the ALD Al_2O_3 growth on H-terminated Si [MIRAI Project]

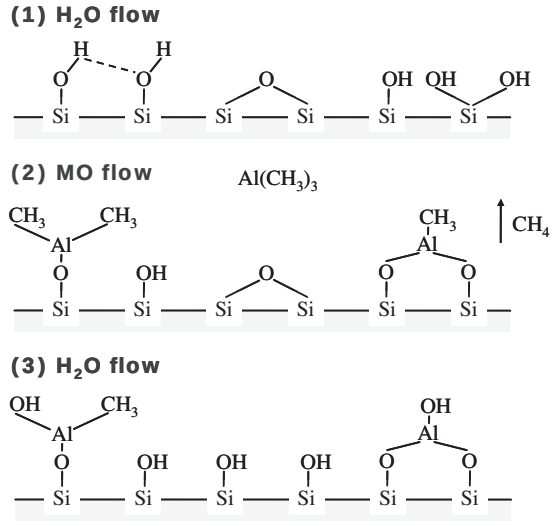

Figure 7.12 The typical film growth mechanism of ALD. H_2O works as the oxidant. The surface reaction-limited deposition dominates the film growth

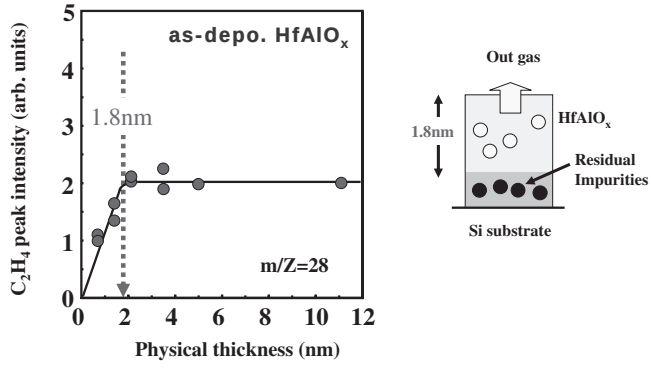

Figure 7.13 C_2H_4 desorption intensity as a function of deposited high-*k* thickness. Above a given physical thickness, the desorption intensity becomes flat, which means that impurities remaining deep inside the high-*k* film cannot be removed out by the post-deposition annealing as schematically described [32]

particularly carbon, are hard to eliminate, even after the PDA process, as shown in Figure 7.13. To solve this problem, a modified ALD system for high-*k* film deposition has been developed [32]. The point of this process is that the annealing process should be performed after ultra-thin film deposition. The layer-by-layer deposition and annealing (LL-D&A) is an ultimate case. A schematic image is shown in Figure 7.14. This process enables one to reduce the residual carbon in the film significantly [32]. It was shown that there were big differences in physical and electrical properties between LL-D&A and conventional ALD+PDA films, where $HfAlO_x$ (Hf:75 at.%) was grown using TMA, $Hf[N(CH_3)_2]_4$ and H_2O as precursors [32].

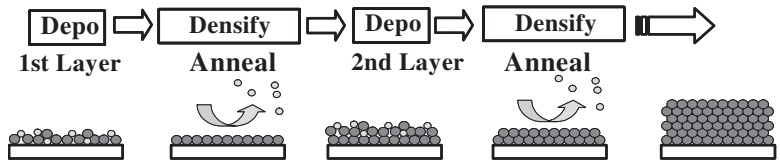

Figure 7.14 Schematic views of the LL-D&A concept for high-*k* film growth. The atomic layer deposition and the rapid thermal annealing are repeated in principle to achieve a targeted thickness [32]

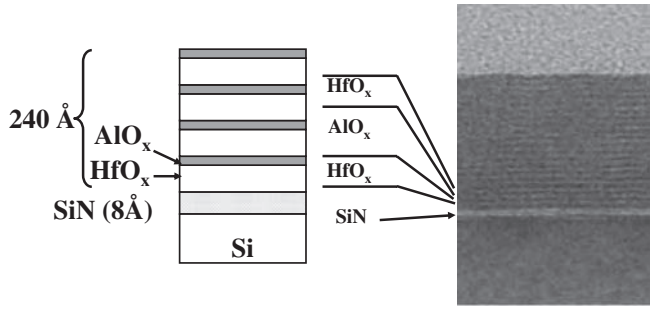

Figure 7.15 A schematic view and cross-sectional TEM picture of the as-deposited film 'superlattice' structure composed of HfO_x and AlO_x layers [33]

To understand what is going inside the films through ALD process, TEM images are helpful, as shown in Figure 7.15, where amorphous multiple HfO_x/AlO_x stack layers, like an inorganic superlattice are shown [33]. By annealing this stacked layers, each layer is intermixed to become amorphous, and then crystallized at a higher temperature, and the densification of the film (thickness decrease) is clearly seen from the thickness change in the TEM image, as discussed in Section 7.7.

Problems related to the ALD process are also precursor dependent, and the process should be carefully optimized for each dielectric material. As expected, other oxidation agent such as O_3 or O_2 plasma instead of H_2O can be used [34]. In any case, it is very important to reconsider the gate stack process so that the ALD process should be constructed coupled with the suppression of the interface layer formation for further reduction of EOT in the next generation [35].

7.6 INTERFACE LAYER

The most significant difference of high-*k* dielectric films from thermally grown SiO_2 is that the high-*k* film is deposited instead of grown, and an the interface layer (IL) is necessarily formed on the Si substrate in a poorly controlled manner, as shown in Figure 7.16. Moreover,

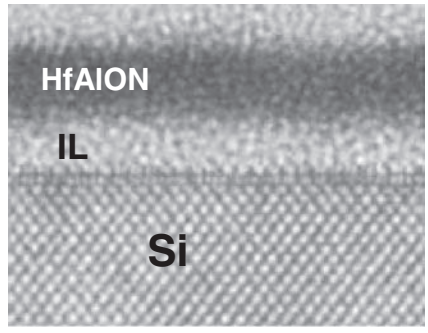

Figure 7.16 Typical cross-sectional TEM picture of HfAlON on Si substrate. IL is principally SiO_2

in order to improve the quality of both interface and bulk high-*k* layers, a thermal treatment in a diluted O_2 ambient is commonly employed as the post-deposition annealing (PDA). Thus, it is quite important to understand interface oxide quality and the oxidation process through high-*k* films from the viewpoint of obtaining highly reliable and ultra-thin EOT dielectric films. In terms of electrical properties at the interface, it was reported that the IL was needed for better performance [36]. Moreover, it was reported that Si oxidation at the ZrO_2/Si interface was accelerated, possibly due to a catalytic effect of the ZrO_2 layer [37]. Recently, nitrided ILs have been investigated for suppressing the interface layer oxide growth and achieving thinner EOT [38–40]. However, the interface characteristics are degraded by the nitridation. In this part, we focus on the SiO_2 interface layer.

7.6.1 Interface layer properties

The interface layer (IL) quality substantially determines the device performance, and depends on all parameters associated with the gate stack formation process. We first discuss IL quality by using transmission FTIR measurements, where the IL can also be investigated for the same sample, in the same experimental set-up, as HfO_2 was measured and discussed in Section 7.3. We investigated the annealing time dependence of interface SiO_2 formation in O_2 ambient at 800°C for the case of sputtered HfO_2. The characteristic Si–O–Si asymmetric stretching mode peak is observed, as shown in Figure 7.17, as a function of the annealing time. However, it is clearly observed that the absorption intensity increases with the annealing time, while the thinner IL SiO_2 shows a peak with lower wavenumber. This is the same as the thin SiO_2 film behavior, which is explained by the fact that the denser film near the interface has the smaller Si–O–Si bond angle, which leads to the lower vibration energy [41]. On the other hand, note that the absorption peak around 760 cm^{-1} assigned to the HfO_2 vibration mode changes little with the annealing time in O_2 ambient, once HfO_2 is crystallized. The results suggest that the interface layer is very similar to the thermal SiO_2 in terms of bonding network structure. Figure 7.18 compares the wavenumber for a peak between the interface SiO_2 and thermally grown SiO_2, as a function of the thickness [12]. A decrease of SiO_2 thickness leads to a decrease of the peak wavenumber and the data

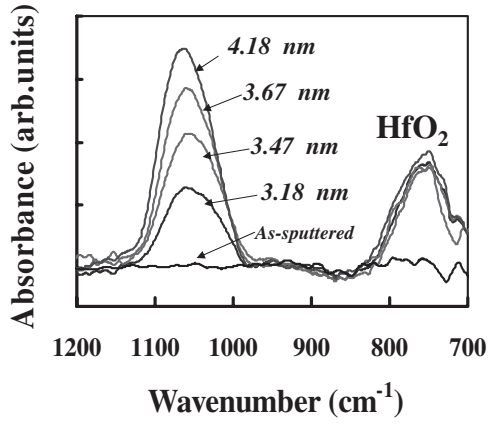

Figure 7.17 Change of IR absorption spectra with the interface layer formation by annealing of sputtered HfO_2/Si at 800°C in O_2 ambient. As the interface layer thickness increases, the peak position attributed to the interface layer shifts to the higher wavenumber, while the peak attributed to HfO_2 is unchanged by annealing in O_2 [12]

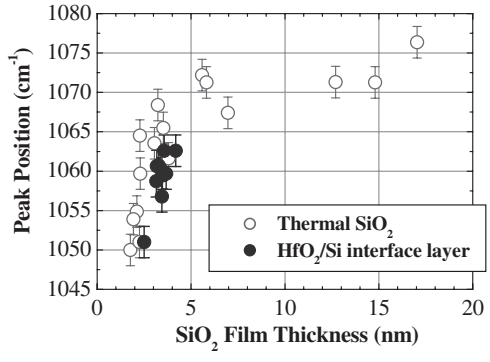

Figure 7.18 Film thickness dependence of the IR absorption peak position for both thermally grown SiO_2 and HfO_2/Si interface layer. The ultra-thin SiO_2 films show the peak at lower wavenumber on account of a smaller Si–O–Si bond angle in ultra-thin films. Since the HfO_2/Si interface layer shows the same relationship between the thickness and the peak position, the interface layer can be regarded as equal to thermally grown SiO_2 in terms of the bonding network structure [12]

in those two cases agree very well. This fact clearly indicates that the interface layer can be basically regarded as a thermally grown SiO_2 layer, in terms of the bonding network structure.

7.6.2 Interface layer formation process

The interface SiO_2 layer inevitably grows on Si in any HfO_2 formation process currently employed, although its thickness depends on the the film growth conditions. We deposited

HfO_2 films on HF-last Si wafers by RF sputtering, using an HfO_2 target. The PDA was performed in an RTA furnace filled with O_2. Various conditions such as time, pressure, or temperature were tested to understand the oxidation characteristics. HfO_2 thickness was varied from 1 to 20 nm. The oxidation rate of bare Si wafers was also measured for comparison. Furthermore, Si wafers with three kinds of surface orientations (100), (110) and (111), were simultaneously processed. In the analysis of the film growth rate, a two-layer model was employed for grazing-angle X-ray reflection (GIXR) and spectroscopic ellipsometry (SE). In fact, it is difficult to accurately determine four unknown parameters in SE analysis, namely both thickness and refractive index of each layer. Therefore, the HfO_2 layer thickness was accurately determined first by the GIXR measurement, due to the large density difference between HfO_2 and others (Si or SiO_2), while the IL thickness was determined with SE by assuming that the IL refractive index was 1.46. Then, we evaluated both the IL thickness and the refractive index of HfO_2. The results determined by the combined method were very accurately compared with those measured by transmission electron microscopy (TEM) in HfO_2/IL/Si system. This method is quite reproducible and quantitatively reliable for nondestructive analysis of the high-*k* gate dielectrics [42, 43].

First we discuss the interface oxidation process on Si in HfO_2/Si system for the relatively thick HfO_2 case. Figure 7.19 shows the oxidation rates both on HfO_2/Si and on the bare Si as a function of Si surface orientation [44]. The IL thickness before PDA is about 0.8 nm, so a very fast oxidation process is expected at the initial stage in the HfO_2/Si system. An interesting point is that the IL oxidation is very slow after the fast initial oxidation and independent of the surface orientation, while SiO_2 growth on the bare Si is significantly dependent on the surface orientation, as reported in the literature [45]. Figure 7.19 shows that the IL growth seems to have a logarithmic dependence on the oxidation time. The slope of the relationship between IL thickness and log(time) is shown in Figure 7.20 as a function of $1/T$ (T is the oxidation temperature). The slope of the temperature dependence is much

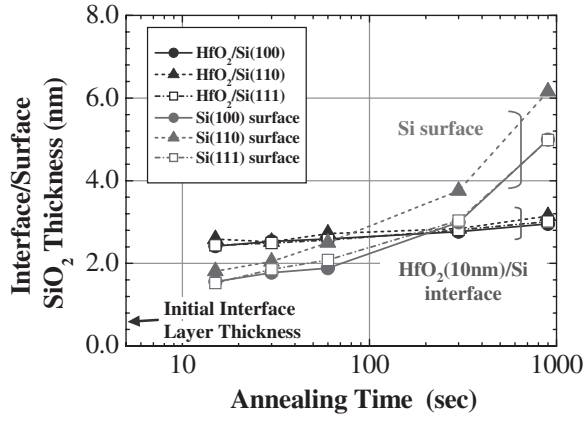

Figure 7.19 The thicknesses of both HfO_2(10 nm)/Si interface layer and thermally grown SiO_2 as a function of annealing time in logarithmic scale. The solid, dotted, and broken lines represent the results on (100), (110), and (111) substrates, respectively. The annealing was performed at 800°C in O_2 ambient. It is noted that the HfO_2/Si interface oxidation rate is initially very fast, but slows down quickly, and is independent of the surface orientation of the substrates [44]

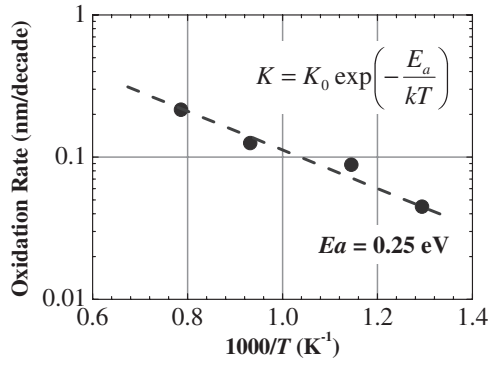

Figure 7.20 Arrhenius plot of the interface oxidation rate in log t scale for 10-nm thick HfO_2/Si. The activation energy is estimated to be 0.25 eV, which is much smaller than that of the conventional oxidation of Si surface [44]

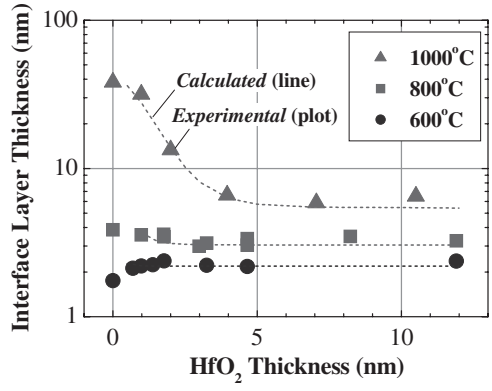

Figure 7.21 Relationship between HfO_2 thickness and interface layer thickness grown at 600, 800, and 1000°C by the annealing in O_2. Dotted lines represent the results calculated on our model where both atomic oxygen and molecular oxygen are considered. The experimental results agree well with the model calculation [44]

smaller than that of the conventional oxidation case. All of the results mentioned above clearly indicate that the oxidation mechanism at the HfO_2/Si system is quite different from that at the Si surface. Those results suggest that oxidation at the HfO_2/Si interface is initially very fast, and it is significantly suppressed with the time in O_2 [46].

Figure 7.21 shows the initial HfO_2 thickness dependence of the interface SiO_2 growth at three PDA temperatures. A very small HfO_2 thickness dependence is observed at each temperature, in the relatively thick HfO_2 region. It has been also reported that oxygen diffusion is very fast in HfO_2 [47], and it is reasonably expected that the interface SiO_2 growth is not limited by the oxygen diffusion process in the top HfO_2 layer.

Figure 7.22 shows the oxygen partial pressure dependence of the interface SiO_2 growth at HfO_2/Si compared with SiO_2 growth on bare Si. Note that a very slight oxygen partial pressure dependence is observed in the SiO_2 growth at HfO_2/Si. This suggests that the

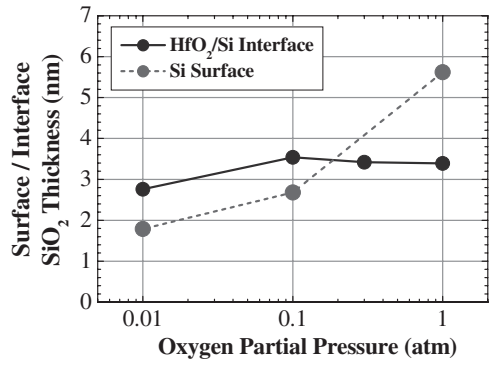

Figure 7.22 Oxygen partial pressure dependence of 10 nm-thick HfO_2/Si interface layer and thermal SiO_2 thickness, grown by annealing at 800°C for 15 min. The surface orientation of the Si substrate is (100). The HfO_2/Si interface oxidation rate shows a weak dependence on the oxygen partial pressure [44]

incorporation process of oxygen species to the HfO_2 layer does not limit the interface oxidation. Therefore, the limiting process of the IL oxidation seems to be the oxygen diffusion process within the interface layer.

Another important point of the oxidation process at the HfO_2/Si interface for the relatively thick HfO_2 region is the state of the oxygen species, both in deposited HfO_2 and in the IL SiO_2. A small temperature dependence and no surface orientation dependence of the interface oxidation growth strongly suggest that the Si substrate is oxidized by atomic oxygen rather than the molecular oxygen. It is consistent with the theoretical argument in which atomic oxygen is more stable than molecular oxygen in HfO_2 [48]. As far as the diffusion process for atomic oxygen in SiO_2 is concerned, similar experimental results for the atomic oxygen process on bare Si have been reported [49]. Moreover, we can reasonably understand the slight partial pressure dependence of the interface oxidation by taking account of the oxidation by atomic oxygen, since it is considered that the concentration of the atomic oxygen in SiO_2 layer exponentially decays due to the deactivation process. Therefore, we think that the IL SiO_2 growth depends on the concentration of the atomic oxygen at the Si surface, which leads to the logarithmic (weak) dependence with regard to the oxidation time [49].

Next we discuss the HfO_2/Si IL oxidation mechanism in the case of the ultra-thin HfO_2. Figure 7.21 shows in the ultra-thin HfO_2 region, the interface layer thickness approaches to the case of Si surface oxidation with the decrease of the HfO_2 thickness [44]. To understand a difference of oxidation characteristics between the ultra-thin and the relatively thick HfO_2 regions, the oxidation rate was again investigated for (100), (110) and (111) samples, as shown in Figure 7.23. While the surface orientation dependence is not observed in the case of the relatively thick HfO_2, it is clearly observed for ultra-thin HfO_2 and is the same as that of the bare Si surface oxidation [50].

These results suggest that interface oxidation for the very thin HfO_2 region is similar to the bare Si surface oxidation, where the oxidation species are mainly oxygen molecules. Thus, it is evident that both atomic oxygen and molecular oxygen are involved in interface oxidation for ultrathin HfO_2 layers.

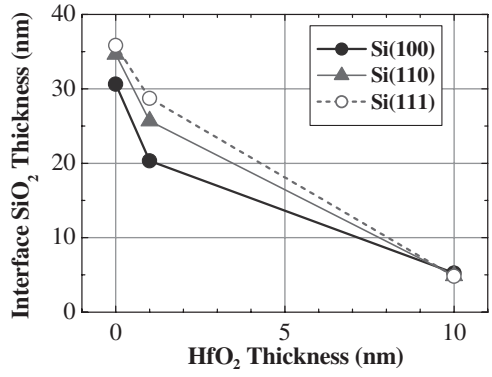

Figure 7.23 Relationship between HfO_2/Si interface layer thickness and HfO_2 thickness, grown by 1000°C annealing in O_2 for the films on (100), (110), and (111) Si substrates. In the case of ultra-thin HfO_2 films, the interface oxidation rate is strongly dependent on the surface orientation of the substrate, while 10-nm-thick HfO_2/Si interface oxidation rate shows no dependence on the surface orientation [50]

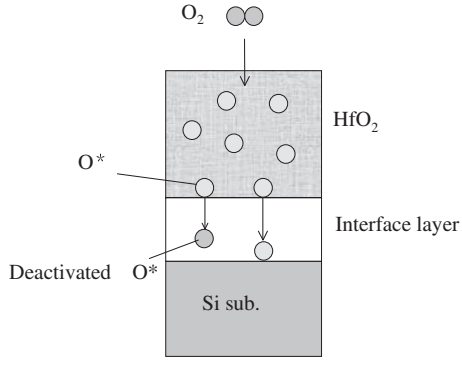

Figure 7.24 A schematic view of the mass transfer of atomic and molecular oxygen in HfO_2/IL/Si stack. We assume both atomic and molecular oxygen diffuse through the stack. The molecular oxygen can penetrate by a short, but finite length in HfO_2, but mostly dissociates into atomic oxygen in the middle of HfO_2. On the other hand, the atomic oxygen injected into IL is rapidly deactivated with a finite decay length

On the basis of those results, we propose a model for oxidation at the HfO_2/Si interface. In this model, we consider a parallel conduction model in which both atomic and molecular oxygen diffuse to the HfO_2/SiO_2/Si stack structure. We further consider a macroscopic mass transfer through the HfO_2/SiO_2/Si structure, and assume that diffusion constants are independent of film thickness. Figure 7.24 shows a schematic view of the atomic and molecular oxygen concentrations in the HfO_2/SiO_2/Si stack. We can construct a relation between the IL SiO_2 and HfO_2 thicknesses on the basis of two kinds of oxygen species diffusion with a finite decay length for the atomic oxygen. Calculated results with one unknown parameter are plotted in Figure 7.21 [44]. Good agreement can be seen between experimental and calculated results. Thus, all of the results obtained through this work indicate that the

dominant oxygen species for the interface oxidation changes with HfO_2 thickness and temperature.

7.7 HfO_2-BASED TERNARY OXIDES

We have thus far discussed HfO_2 as a high-*k* dielectric film. Recently, a number of high-*k* materials besides pure HfO_2 have been reported. Other transition metal oxides or rare earth metal oxides are typical examples. A ternary system is another approach to obtain a new high-*k* material. It is expected that the ternary system may provide a new function and/or alleviate disadvantages of the binary one. In this part, we focus on HfO_2-based ternary oxides.

7.7.1 $HfSiO_x$ and $HfAlO_x$

The most well-researched ternary systems are $HfSiO_x$ and $HfAlO_x$. Each of them is a HfO_2 film compounded with a very robust amorphous dielectric, SiO_2 or Al_2O_3. One should first refer to the phase diagram of relevant systems. Figure 7.25(a) and (b) show HfO_2-SiO_2 [51]

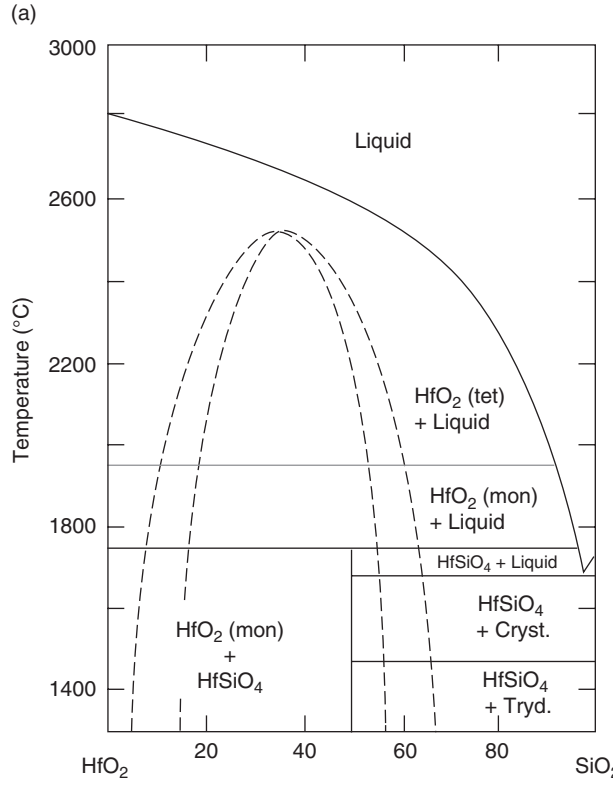

Figure 7.25 (a) The phase diagram for the HfO_2–SiO_2 compositional system, with a liquid–liquid immiscibility zone (dotted line) [51]

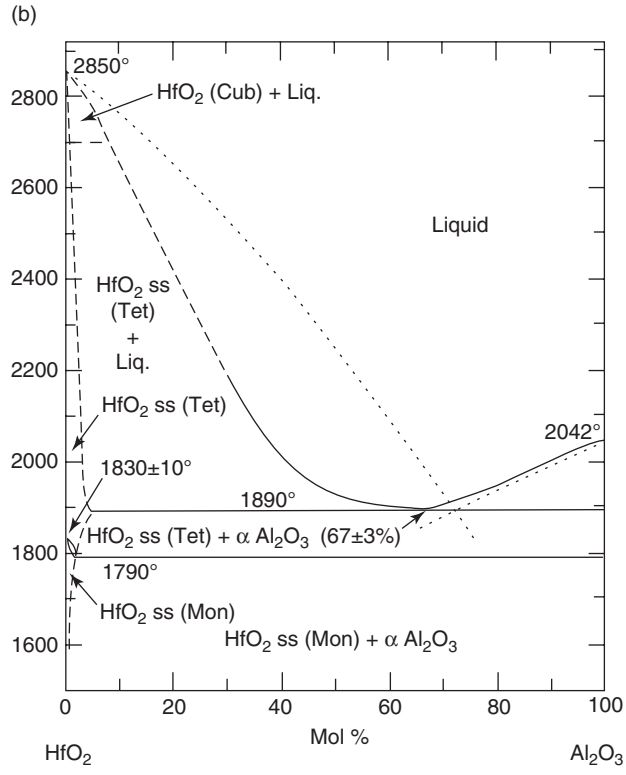

Figure 7.25 (*continued*) (b) the phase diagram for the HfO_2–Al_2O_3 compositional system [52]

and HfO_2-Al_2O_3 [52] phase diagrams respectively. The temperature employed in the ULSI process does not reach the high temperatures generally reported in the phase diagrams. In addition, very thin films are not in a thermal equilibrium, but in a quasi-equilibrium. Nevertheless, one can predict material stability trends from the phase diagrams.

A very big advantage of Hf silicate is that its ultimate limit (the lowest Hf concentration limit) is SiO_2, and its affinity with the Si substrate seems to be relatively good. The crystallization temperature increases with Si introduction into HfO_2, but a large amount of Si in $HfSiO_x$ is needed to maintain the amorphous state around 1000°C. However, it decreases the dielectric permittivity significantly and substantially reduces the advantage of the high-*k* film. Since a number of studies on high-*k* device technology have focused on Hf silicate CMOS, we will not discuss it in detail, but make two comments on this system from the viewpoints of phase separation and transformation.

It is necessary to consider the effects of crystallization and phase separation on gate dielectric properties. There seems to be no quantitative evidence for crystallization-enhanced leakage current in ultra-thin films. High-*k* dielectrics are not thick films, so we have to compare the intrinsic leakage current with the crystallization-induced leakage in the ultra-thin region. We think that an important effect is not crystallization, but phase separation in this material [53]. $HfSiO_4$ (Hafnon) in a thick (100 nm) film in XRD as shown in Figure 7.26. In fact, high-temperature optical microscope observation shows that local nucleation

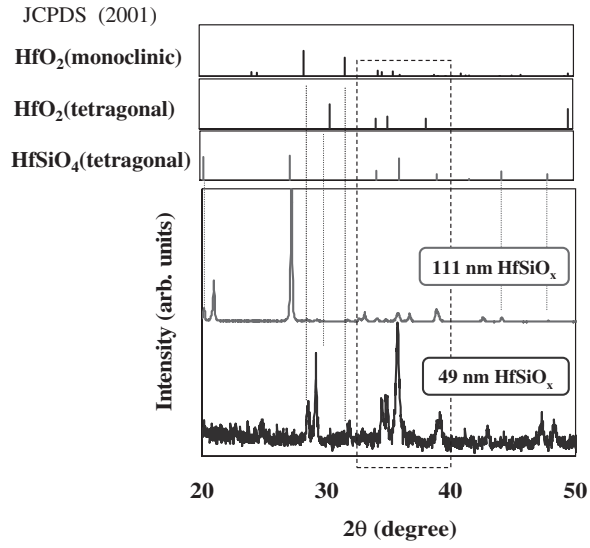

Figure 7.26 XRD patterns for 111-nm-thick and 49-nm-thick $HfSiO_x$ films with composition Si : Hf ~ 40 : 60 annealed at 1000°C in O_2. The expected peak positions for monoclinic HfO_2, tetragonal HfO_2, and tetragonal $HfSiO_4$ phase are also shown for the reference. The peaks attributed to the tetragonal $HfSiO_4$ phase appear only for 111-nm-thick film

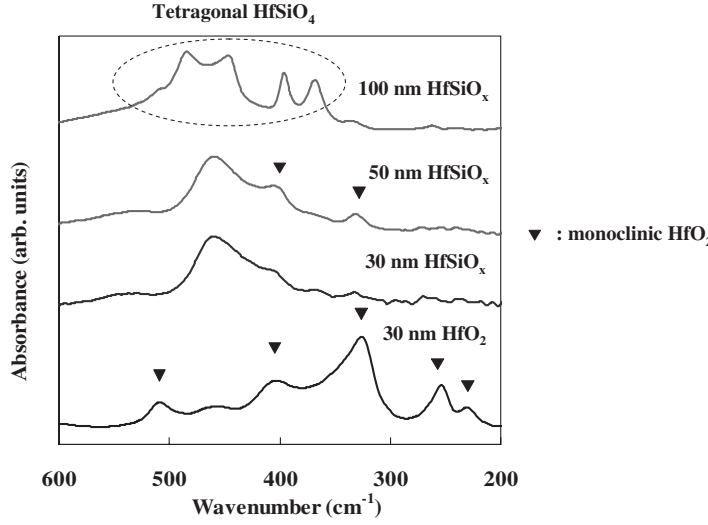

Figure 7.27 Far-IR absorption spectra of $HfSiO_x$ (Hf : Si ~ 6 : 4) films with various thickness and HfO_2 film annealed at 1000°C in O_2. 30- and 50-nm-thick $HfSiO_x$ films show a broad peak around 450 cm^{-1} in addition to the relatively weak peaks from monoclinic HfO_2. The 100-nm-thick film shows different pattern because of the formation of tetragonal $HfSiO_4$ phase [53]

in samples of $HfSiO_x$ starts at around 1000°C, and grows very clearly around 1200°C for a minute. Both HfO_2 and SiO_2 are identified in high-temperature-annealed samples with FTIR, as shown in Figure 7.27. This fact may bring about the spatial variation of dielectric properties in gate dielectric film. Thus, there is a concern that Hf silicate may cause a

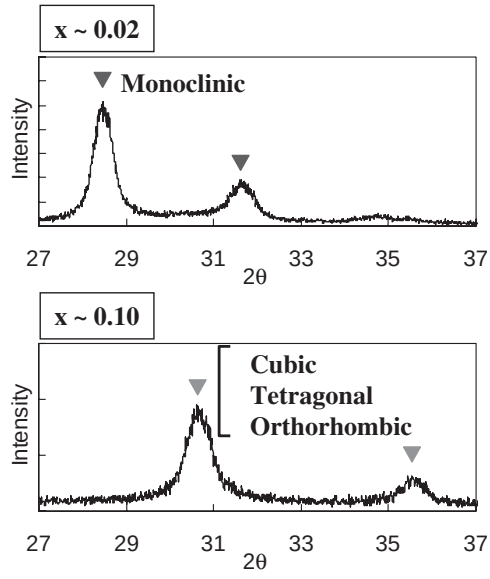

Figure 7.28 XRD patterns of 2 and 10 at.% Si-doped HfO_2 films annealed at 800°C. The crystal phase clearly changes from the monoclinic to a different one by 10 at.% Si doping. The new phase can be attributed to be tetragonal, cubic, or orthorhombic phase [54], although the main crystal phase is considered to be tetragonal from the more precise XRD analysis [13]

dielectric property fluctuation in very short channel gate length devices, which will be a big problem in the ULSI system in terms of the statistical V_{th} fluctuations.

A small amount of Si in $HfSiO_x$ has another effect on the crystallization. Figure 7.28 shows XRD patterns of 2 and 10 at.% Si-doped HfO_2 [54]. Note that by introducing 10% Si the crystallization is not to the monoclinic, but mainly to the tetragonal phase (first identified as cubic-like, but later as the tetragonal by more precise XRD measurement) [55]. FTIR results have also shown the clear structural phase transformation by introducing a slight amount of Si into HfO_2. This fact is related to the dielectric permittivity modulation as discussed in Section 7.7.3.

$HfAlO_x$ is another example of a high-temperature crystallization system. To determine the crystallization process of this system, periodically grown multistack films, as shown in Figure 7.29, were prepared [56], since not enough data on $HfAlO_x$ have been reported. Relatively thick films (~24 nm) consisting of periodically stacked HfO_x/AlO_x layers with various ratios of Hf to Al were grown by the ALD method. A SiN layer was first grown on Si (100) at 800°C in NH_3, in order to restrict the Si diffusion into the high-k film. The PDA was performed in the RTA furnace for 30 s at various temperatures in N_2. An as-deposited film has a long-range periodicity like an inorganic artificial superlattice and, by changing the cycle ratio in the growth process, the ratio of Hf to Al can be easily controlled by ALD. Figure 7.30 shows XRD patterns of HfO_x/AlO_x (3/9 Å) stacked films as a function of annealing temperature, in which a single peak around $2\theta = 7.6°$ in the as-deposited film is observed. This value corresponds to $d = 11.59$ Å, which is in good agreement with one set of HfO_x/AlO_x thickness (about 12 Å). The superlattice structure is hardly observed after annealing at 750°C, and the stacked film structure changes into a homogeneous amorphous

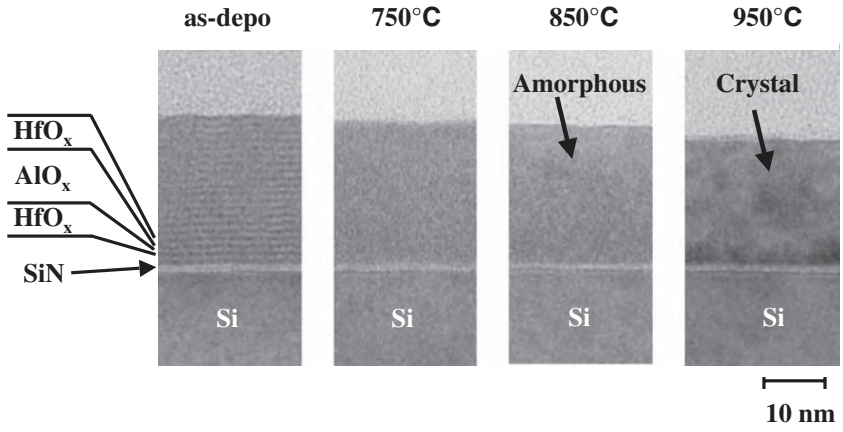

Figure 7.29 Cross-sectional TEM picture of as-deposited, and annealed films composed of HfO_x and AlO_x layers. As-sputtered film shows a supperlattice structure, while annealed film becomes amorphous, then crystallizes by 950°C annealing (MIRAI Project)

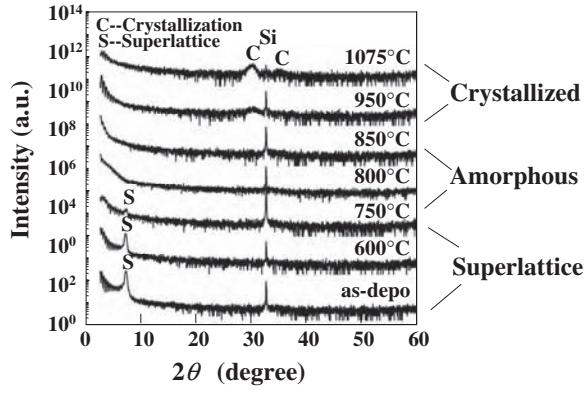

Figure 7.30 XRD patterns of HfO_x/AlO_x (3/9 Å) stacked films as a parameter of annealing temperature in N_2 for 30 s. A single peak around $2\theta = 7.6°$ in the as-deposited film corresponds to $d = 11.59$ Å, which is almost the periodicity of HfO_x/AlO_x stacked layers [56]

one. Crystal structure analyses were systematically performed as a function of the Hf/Al ratio and the annealing temperature. The phase diagram of the Hf–Al–O system was then constructed, as shown in Figure 7.31 [56]. Both monoclinic and cubic phases are observed for smaller Al contents, while the cubic phase is only observed with an increase in Al content.

7.7.2 New candidates for amorphous high-*k* dielectric films

The stability of glasses has been investigated for a long time. In the silicon microelectronics community, SiO_2 has been generally considered as a typical amorphous material. When

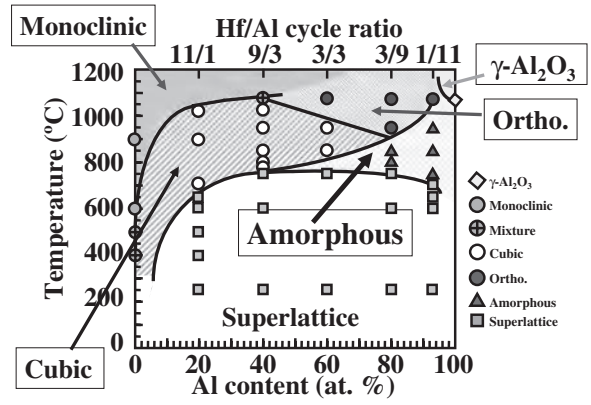

Figure 7.31 The phase diagram of the Hf–Al–O system as a parameter of temperature and Al content, which was determined by the systematic experimental results of Figures 7.25 and 7.26 [56]

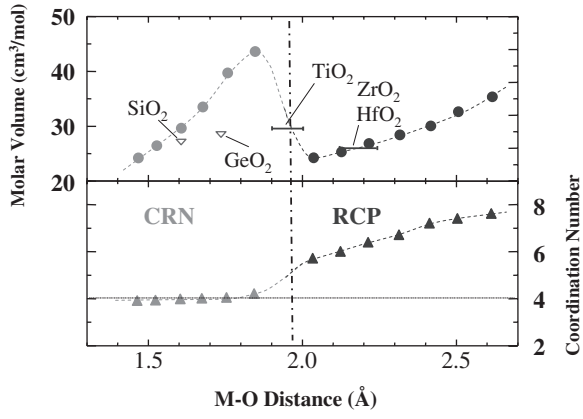

Figure 7.32 Molar volume and coordination number of amorphous metal oxides, calculated by the classical molecular dynamics as a function of metal–oxygen (M–O) distance. Shorter M–O distance gives SiO_2-like continuous random network (CRN), while longer M–O distance results in a random close packing (RCP) structure, which is basically determined by the oxygen atom packing [57]

amorphous high-*k* materials are concerned, however, it should be noted that the amorphous nature of high-*k* films is different from SiO_2 in terms of the network structure. Thermally grown SiO_2 has a continuous random network (CRN), while HfO_2 has a random close-packed (RCP) structure. The latter is basically determined by the oxygen atom packing. By using molecular dynamics calculations, the difference between the two types of amorphous structures has been pointed out from both viewpoints of the molar volume vs metal–oxygen (M–O) distance and the coordination number vs M–O distance [57], as shown in Figure 7.32. It is clearly seen that there are two types of amorphous materials, group A and B. Group A is classified into the amorphous SiO_2-like group, while group B into high-*k* materials. There is a distinct change from CRN to RCP as a function of M–O distance. This change causes a striking difference in the structural stability, and may correspond to the stability

criterion which was discussed from the viewpoint of the average coordination number balance between a freedom of space and bonding constraints for atom motion [58].

As described previously, SiO_2 and Al_2O_3 have been incorporated into HfO_2 to suppress the crystallization. In fact, HfSiO and HfAlO achieve higher crystallization temperatures, but their dielectric permittivity values decrease. Thus it is obvious that further EOT scaling requires new dielectrics with both high dielectric permittivity and high crystallization temperature. Recently, it was reported that La_2O_3 introduction to nanophase HfO_2 powders can raise the crystallization temperature (~900°C) [59]. Furthermore, it is expected that incorporating La_2O_3 will not cause the degradation of dielectric permittivity, because La_2O_3 is a more ionic oxide and has a higher dielectric permittivity in principle, in contrast to SiO_2 or Al_2O_3. Figure 7.33 shows XRD spectra of 30-nm-thick HfO_2, La_2O_3, and $HfLaO_x$ films annealed at various temperatures. Both HfO_2 and La_2O_3 films start to crystallize below 600°C, while $HfLaO_x$ films with 33 at.% La and 40 at.% La remain amorphous, even after annealing at 800°C and 900°C, respectively [60]. The XRD peak of crystallized $HfLaO_x$ films around $2\theta = 29°$ corresponds to the (222) planes of the pyrochlore $La_2Hf_2O_7$ structure [61]. A small amount of La_2O_3 stabilizes cubic HfO_2, which will be discussed later for the case of Y_2O_3 introduction. With increase of La concentration in $HfLaO_x$, the film shows higher crystallization temperature, as seen in Figure 7.34. Considering that the ionic radii of Hf^{4+} and La^{3+} are 0.71 and 1.03 Å (for six-fold coordination), a significantly large difference in ionic radius may substantially suppress the long-range ordering [62]. Thus, this is classified as the typical group B amorphous material.

Figure 7.35 shows bidirectional *C–V* characteristics at different frequencies for Au/40%La-$HfLaO_x$/*p*-Si MIS capacitors. The *C–V* curves show neither hysteresis nor frequency dispersion, indicating good electrical quality. From good linear relationships with

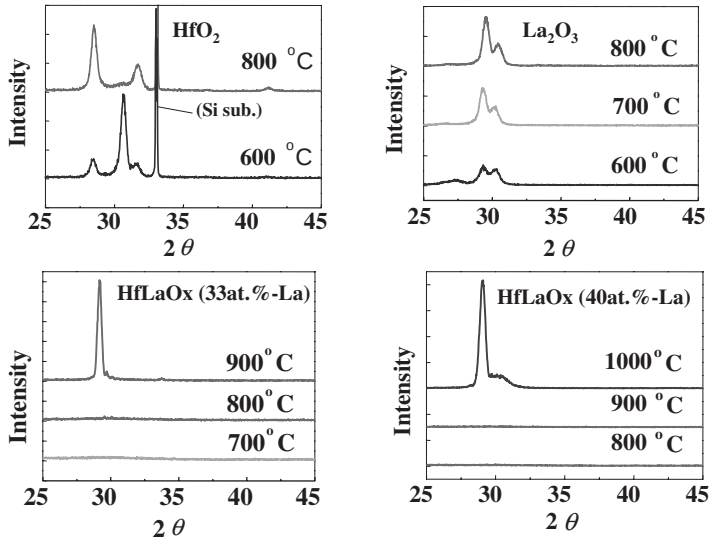

Figure 7.33 XRD patterns of 30-nm-thick HfO_2, La_2O_3, and $HfLaO_x$ films annealed at 600–1000°C. Both HfO_2 and La_2O_3 films starts to crystallize at 600°C, while $HfLaO_x$ with 33 and 40 at.% La remain amorphous, even after annealing at 800 and 900°C, respectively. The observed peak in $HfLaO_x$ films ~29° corresponds to the (222) planes of the pyrochlore $La_2Hf_2O_7$ [60]

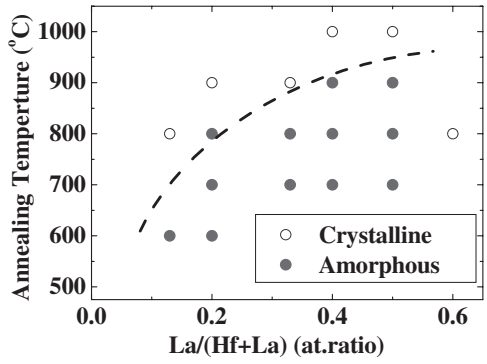

Figure 7.34 Crystallinity of $HfLaO_x$ films with various compositions and various annealing temperatures. The filled and open circles correspond to amorphous and crystalline film, respectively. The crystallization temperature increases over 900°C as the La concentration increases [62]

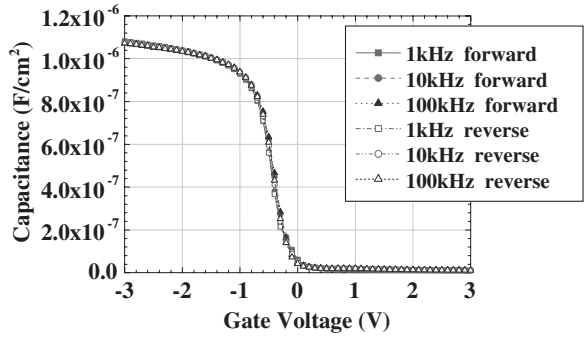

Figure 7.35 Bidirectional *C–V* characteristics of Au/$HfLaO_x$ (La/(Hf + La) = 0.4)/*p*-Si MIS capacitor annealed at 600°C. The film thickness is 8.4 nm. Almost no hysteresis nor frequency dispersion is observed [62]

a very small dispersion in the CET vs physical thickness, *k* values are estimated to be 20–22 for all of the samples. The dielectric permittivity value of $HfLaO_x$ as a function of La concentration in $HfLaO_x$ is plotted in Figure 7.36. The *k* value of $HfLaO_x$ is roughly constant above 20, which is advantageous in terms of very small dielectric fluctuation [60]. It was also reported that $La_2Hf_2O_7$ was a promising material for amorphous medium *k* value (much below 20) dielectric film, due to its lattice parameter match to the Si substrate. [63, 64]. These results shown in this section suggest that the $HfLaO_x$ system will be a potential candidate for advanced CMOS application.

7.7.3 Dielectric permittivity engineering

It is well known that there are several crystalline structures of HfO_2. Since the low-temperature phase of HfO_2 is monoclinic, the XRD pattern for the pure HfO_2 films generally shows the monoclinic structure even after annealing at relatively high temperatures in ULSI

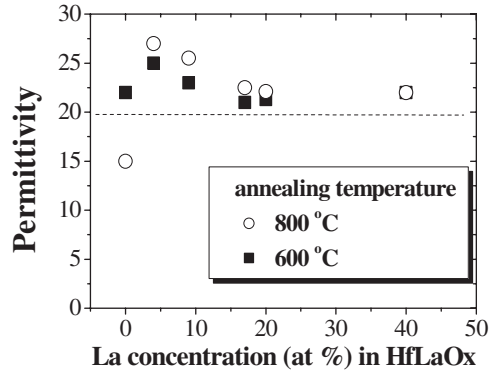

Figure 7.36 Relative permittivity as a function of La concentration in $HfLaO_x$ films, evaluated for MIM capacitors ($Au/HfLaO_x/Pt$). The films were annealed at 600°C and 800°C. By <10 at.% La doping, *k* increases drastically because of the molar volume shrinkage through the crystallization into a cubic structure. With >20 at.% La, the films are amorphous but *k* ~22 is maintained [62]

process. This characteristic is also observed in the IR absorption spectrum, as discussed in Figure 7.5.

Concerning the dielectric permittivity of a ternary oxide, by a rough estimation it could be an average permittivity of two oxides. However, as mentioned in Figure 7.21, the unit structure can be changed by mixing two binary oxides. Thus the ternary oxides can have a different phase, which may hopefully enable one to create a new higher-*k* material. In the remaining part, we discuss possibilities for dielectric permittivity engineering by modulating the microscopic origin, as discussed in Section 7.2.

Phase transformation

Much research concerning ZrO_2-based ternary oxides has been reported in the ceramics community. The typical example is YSZ (Yttria–stabilized zirconia), which has a cubic structure. Since we are interested in the cubic rather than the monoclinic HfO_2 from the viewpoint of dielectric permittivity [15], Y-doped HfO_2 may be an interesting material system to investigate.

Y-doped HfO_2 (YDH) was grown on HF-last (100) Si or 100 nm Pt deposited on SiO_2/Si, by co-sputtering HfO_2 and Y_2O_3 targets in Ar, followed by thermal annealing in 0.1% O_2 for 30 s at various temperatures. Au and Al electrodes were evaporated for top gate and bottom contact, respectively. The dielectric permittivity was determined using both MIS and MIM structures.

Figure 7.37 shows the dielectric permittivity of YDH as a function of Y atomic concentration in HfO_2 [65], where there are several characteristic features to notice. The first is the *k* value increase with Y concentration increase. The second is that the *k* value has a peak as a function of Y concentration. Finally, the pure HfO_2 *k* value decreases with crystallization into the monoclinic phase. These facts are difficult to explain by a simple effective media model, because the Y_2O_3 *k* value is around 12 [66]. Figure 7.38 shows XRD

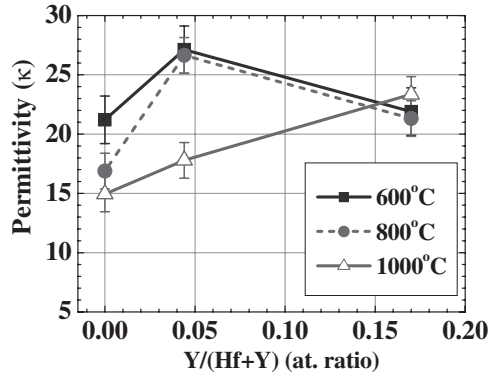

Figure 7.37 Change of relative permittivity by Y-doping into HfO_2 films annealed at 600–1000°C evaluated for MIS capacitors (Au/Y-doped HfO_2/Si). For the films annealed at 600 and 800°C, the permittivity jumps up by Y-doping ($k \sim 27$) and it gradually decreases by further Y-doping. The k value for the films annealed at 1000°C does not have a peak, but increases gradually [65]

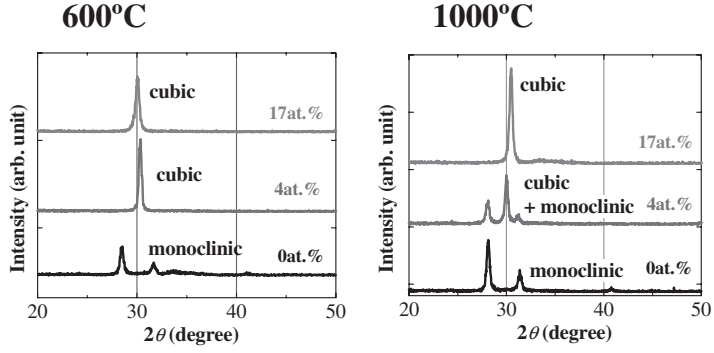

Figure 7.38 XRD patterns for the Y-doped and undoped 30-nm-thick HfO_2 films annealed at 600 and 1000°C in 0.1% O_2 + N_2 ambient. At the temperature as low as 600°C, the films show a clear phase transformation from the monoclinic to the cubic phase by Y-doping. The 17 at.%-doped film shows a peak at slightly lower angle than that of 4 at.%-doped film, since the increase of Y concentration induces a gradual lattice expansion. At 1000°C, on the other hand, they show a phase separation by 4 at.% Y-doping [65]

patterns for pure HfO_2 and YDH, where a big structural difference is observed between them. By annealing at 600°C, the pure HfO_2 is crystallized to the monoclinic phase, while YDH tends to the 'cubic' as expected in the phase diagram. This fact points out that a structural transformation from the monoclinic to the cubic phase induces a change of the dielectric permittivity. The theoretical calculation of HfO_2 predicts a higher dielectric permittivity for the cubic phase than that for the monoclinic one [15]. Nevertheless, it is expected that the increase of Y ratio in HfO_2 eventually brings about the decrease of the dielectric permittivity in the effective media sense.

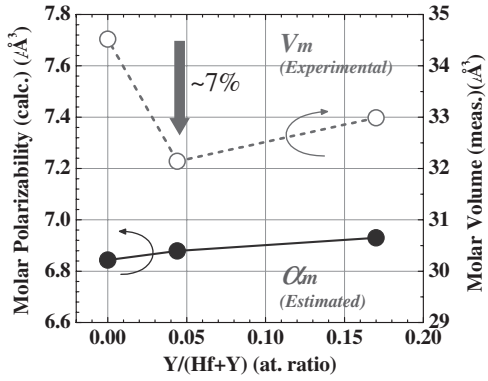

Figure 7.39 The molar volume V_m and molar polarizability α_m change by Y-doping for films annealed at 800°C. The V_m values are determined experimentally from XRD measurements, and the α_m values are estimated by substituting the experimental k and V_m values into the Clausius–Mossotti relation. V_m shrinks drastically by the transformation from the monoclinic to the cubic phase, while it is seen that α_m does not change significantly [70]

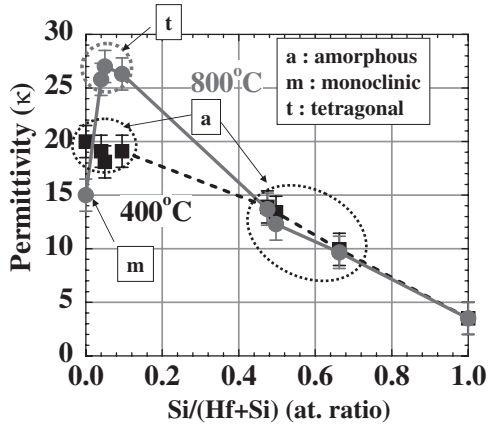

Figure 7.40 The relative permittivity of $HfSiO_x$ films annealed at 400 and 800°C in 0.1% $O_2 + N_2$ ambient. By 5–10 at.% Si-doping $HfSiO_x$ films show a phase transformation from the monoclinic to the tetragonal phase, and a drastic increase of the permittivity at 800°C, while the films are amorphous and do not show a permittivity jump at 400°C [68]

Figure 7.39 shows both V_m and α_m as a function of Y content, where α_m was calculated from both k and V_m using the Clausius-Mossotti relation. It clearly shows that k enhancement is dominantly due to the V_m reduction rather than α_m enhancement [67].

In the case of the Hf–Si–O system, a structural transformation was also observed, as shown in Figure 7.17, and the dielectric permittivity in this case should be also affected by the phase transformation of HfO_2. Figure 7.40 surprisingly shows that the dielectric permittivity increases up to 27 with a slight Si introduction into HfO_2 [55]. The k value increase can be also explained by the V_m shrinkage in the Clausius–Mossotti relation [68]. Although there is a big difference between Y_2O_3 and SiO_2 from the viewpoint of the unit structure

and of bonding characteristics, the doping effect on the dielectric permittivity seems to be the same in the case of a small amount of Y_2O_3 or SiO_2 doping. Namely, the dielectric permittivity of those ternary system is determined by the HfO_2 inherent property structurally modified by the 'doping'.

Polarization modulation

Another way to change the k value is to modulate the ionic polarizability by decreasing the force constant of the ionic system. Since in typical high-k materials, each atom is fully ionized and the force constant is $M^*\omega_0^2$, lighter metal oxides and/or the lower vibration frequency materials would be better. Here we consider two examples; TiO_2 and CeO_2, because it is well known that the valence is not stable in both materials (we expect that the bonding strengths of such materials will be weak). In addition, the metal atom mass is lighter in the case of Ti.

Figure 7.41 shows IR absorption spectra of TiO_2, CeO_2 and HfO_2, and typical absorption peaks of those oxides are located in the far-IR region as expected [69, 70]. Figure 7.42 shows the relationship between dielectric permittivity and Ti ratio in HfO_2 for samples annealed at 600 and 800°C [69, 70]. It is clearly shown that the k-value depends on the Ti concentrations for both cases. We can also divide the k-value of Hf–Ti–O system into the molar polarization α_m and molar volume V_m contributions as for the YDH case. The result indicates that the molar polarization increase is the origin of the k value enhancement. The dielectric permittivity simply increases with Ti content increase up to around 40, for the case of the 800°C-annealed sample with 60 at.% Ti in the Hf–Ti–O system. However, it should be noted that there is a drawback, the energy bandgap reduction. This severely degrades the leakage current. On the other hand, the frequency dependence of the k value was observed in the Hf–Ce–O system due to a significant dielectric loss [70, 71], though a high permittivity is obtained in the low-frequency region. This might suggest that the

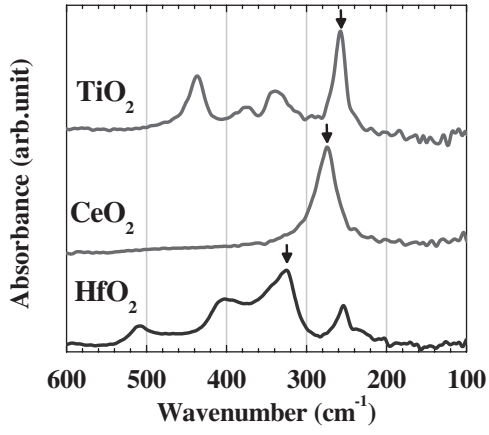

Figure 7.41 Far-IR absorption spectra for 20-nm-thick HfO_2, CeO_2, and TiO_2 films, annealed at 800°C. Those films show the peaks in far-IR region, which is a direct evidence of the low-frequency lattice vibration in these films [70]

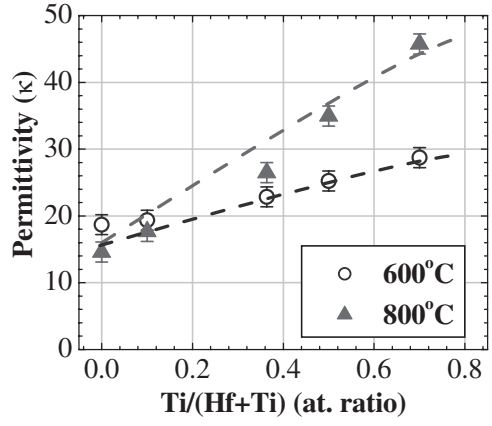

Figure 7.42 The relative permittivity of $HfTiO_x$ films annealed at 600 and 800°C. The permittivity increases monotonically up to $k \sim 30$ at 600°C, and $k \sim 45$ at 800°C. The films with Ti/(Hf + Ti) = 0.36, 0.5, and 0.68, are crystallized in orthorhombic $HfTiO_4$ phase at 800°C, but are amorphous at 600°C. The introduction of Ti into HfO_2 films enhances the molar polarizability and increases the permittivity [70]

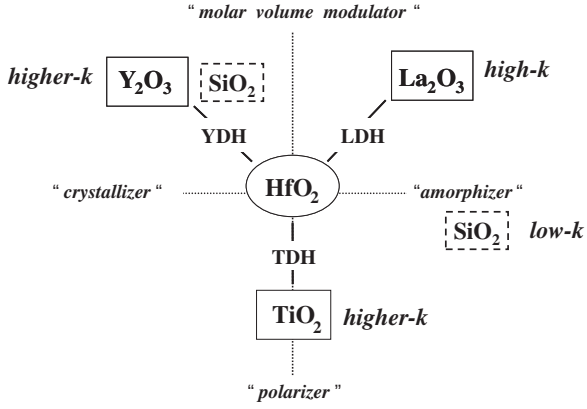

Figure 7.43 A schematic diagram for designing higher-*k* materials based on HfO_2. The role of the additives for HfO_2 can be classified into four groups, '*crystallizer*', '*amorphizer*', '*molar volume modulator*', and '*polarizer*'. The former two groups enhance/retard the crystallization, and the latter two groups can enhance the permittivity by molar volume shrinkage/molar polarizability enhancement, respectively [70]

smaller force constant leads to a structural instability, even though the static *k* value is relatively high.

Throughout those results and discussions, we can illustrate a schematic diagram to engineer high-*k* film properties (*k* value increase and/or a selection between amorphous and crystallization) by doping other oxides into HfO_2, as shown in Figure 7.43. Y_2O_3 and La_2O_3 play roles as the molar volume modulator with easier and tougher crystallization, respectively. This diagram provides a guideline for designing new ternary or more complex materials for advanced higher-*k* CMOS [67, 70].

7.8 HIGH-*k* MOSFET

High-*k* dielectrics will be used for scaled CMOS, and a comfortable match with scaled properties in CMOS trend should be maintained. The impact of high-*k* gate dielectric films on the short-channel effect has been studied on the basis of numerical simulations [72], while key device parameters concerning the scaling down are the carrier mobility and the threshold voltage, which are discussed in this section.

7.8.1 Inversion layer mobility

It is reported that FET performance is still determined by the carrier mobility, even in ultra-short-channel MOSFETs [73], so thin *EOT* FETs employing high-*k* dielectrics should not allow the carrier mobility degradation. However, the fact is that the mobility in high-*k* FETs is degraded compared with that in conventional SiO_2 FET's [74–76]. This is mainly due to the poor quality of the present high-*k* films; high-*k* films possess a huge amount of charged scattering centers inside them. So, the effective mobility μ_{eff} in the low effective field E_{eff} is significantly degraded, as typically shown in Figure 7.44 for several EOT MOSFETs [56], where the universal relationship for SiO_2 MOSFET's is also shown. In actual CMOS operation, any μ_{eff} at any E_{eff} contributes to the dynamic performance of CMOS circuits, but μ_{eff} at high E_{eff} is much more effective than μ_{eff} at low E_{eff}. So, relatively high-field mobilities are in general compared with each other, and μ_{eff} at E_{eff} = 0.8 or 1 MV/cm is often used for the technology comparison. Early in high-*k* research, μ_{eff} was very poor for any field, but has recently improved greatly due to film quality improvements. In the MOSFET mobility analysis, three major scattering mechanisms are generally considered. They are: (1) coulombic scattering; (2) acoustic phonon scattering; and (3) interface roughness scattering [77]. It is true that the peak mobility is obviously degraded by the coulombic scattering centers, both at the interface

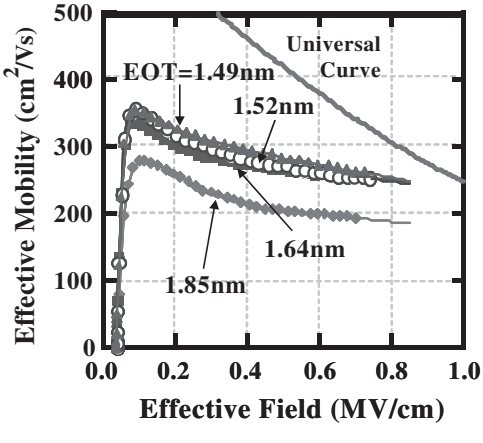

Figure 7.44 Effective electron mobility μ_{eff} as a function of effective field E_{eff} of HfAlON MOSFETs for four kinds of EOTs. Compared with the SiO_2 MOSFET, high-*k* MOSFET mobility is degraded, especially at lower E_{eff}. [56]

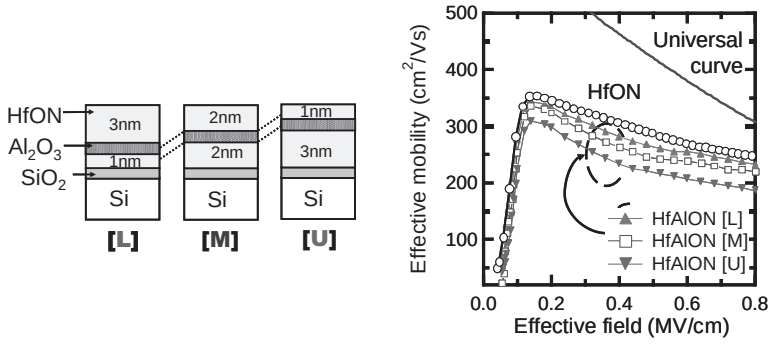

Figure 7.45 A schematic view of Al-profiled HfON. (L), (M), and (U) stand for the location of Al in HfON, respectively. μ_{eff}–E_{eff} relationship is a parameter of the Al position in HfON. Note that μ_{eff} is degraded in spite of the Al position far from the Si interface. The results show that the mobility is more sensitive to N profile rather than to Al [80]

and inside the high-*k* film. It is interesting to consider that, in high-*k* MOSFETs, a new scattering mechanism related to the ionic characteristics of high-*k* films has been proposed [17], the remote optical phonon scattering. Based upon the temperature dependence of the mobility or upon the metal gate stack performance, some reports maintain that the remote optical phonon scattering is the major mobility degradation mechanism [78, 79]. In fact this mode of the μ_{eff} degradation may exist, but it is not sure that this scattering mechanism may be quantitatively a major degradation mode for actual high-*k* MOSFETs. We need more accurate mobility analysis of thinner EOT high-*k* MOSFETs to clarify the effect of this scattering mechanism on Si CMOS devices.

Recent high-*k* films often introduce nitrogen to suppress crystallization, which also further degrades the mobility. Thus, the nitrogen profile in the film is also critical for optimizing the mobility [80], as shown in Figure 7.45. Furthermore, it is worth mentioning that the mobility value should be compared by taking account of the gate leakage current, because 'SiO_2-like high-*k*' definitely shows high mobility, but also high leakage current at a given EOT. So, a fair comparison of the mobility values among different high-*k* materials processed differently should be done as functions of EOT and the leakage current. This is a major challenge for sub-nanumeter EOT generation CMOS, where the remote optical phonon scattering might be of a great concern.

Concerning the mobility analysis of high-*k* MOSFETs, it is necessary to take care of the measurement technique in order to eliminate parasitic effects in the quantitative analysis. In the conventional mobility analysis, the split *C–V* technique is employed, where *C–V* and *I–V* measurements are performed independently in a steady state. In the case of dielectric films with a huge amount of traps, a *C–V* characteristic does not provide an accurate inversion charges [81]. Recently the pulsed *I–V* technique is proposed for the accurate measurement without any trap-filling effect [82]. Another issue is how to accurately determine the inversion layer mobility of short-channel MOSFETs, where many parasitic effects are involved in addition to the intrinsic properties, even in conventional MOSFETs. The double mask length method has been recently proposed for short-channel MOSFET analysis [83]. Since each technique may not be perfect for the present, it should be stressed that a very careful analysis is needed to discuss the inversion layer mobility quantitatively.

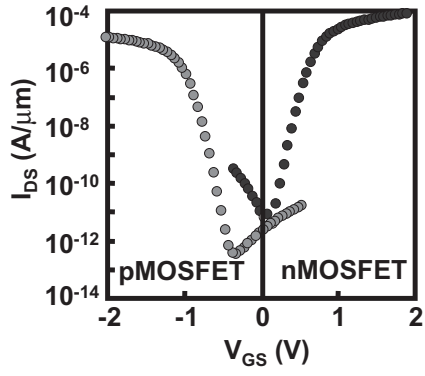

Figure 7.46 An asymmetric V_{th} between n^+-poly-Si and p^+-poly-Si HfO_2 MOSFETs, which might originate from the Fermi-level pinning at poly-Si/HfO_2 interface. V_{th} in p^+-poly-Si HfO_2 MOSFETs is more significantly shifted from the ideal value (MIRAI Project)

7.8.2 Threshold voltage

For the low-power supply voltage operation, the threshold voltage V_{th} control becomes more important in achieving high driving current. A V_{th} asymmetry between n^+-poly-Si and p^+-poly-Si gate MOSFETs was observed for the case of using Hf-based high-k dielectric films [84]. A typical example is shown in Figure 7.46. This is problematic from the viewpoint of short-channel CMOS operation with a low-power supply voltage. Very recently, this issue has been discussed from the viewpoint of the Fermi-level pinning at the gate electrode/high-k interface [85]. It is noted that the Fermi-level pinning also appears in the case of metal silicides [86]. This fact indicates that doped FUSI (fully silicided) technology [87] is not applicable for V_{th} tuning [88, 89], though the origin is not fully understood yet. In the case of metal gate electrodes not including Si it has been reported, the V_{th} behavior due to the Fermi-level pinning appears different [90]. As is the case for the Schottky barrier height, it is inferred that interface dipoles may have something to do with the Fermi-level pinning [91], but the dipole origin is still under investigation. There are typically two types of model for the Fermi-level pinning in the poly-Si gate HfO_2 MOSFETs. One is due to Si–Hf bonding-related dipoles [85], and the other is due to the charge balance originating from oxygen vacancies in the film [92]. In both cases, the pinning is related to intrinsic properties of the high-k materials.

From the material engineering point of view, it is expected that high-k dielectric materials might also affect the Fermi-level pinning characteristics. In fact, it has been recently found that the flat-band voltage V_{FB} of $HfAlO_x$ MOS capacitors changes with Al concentration, as shown in Figure 7.47 [93]. Here, Al introduction is one example modifying the Fermi-level pinning at gate electrode/high-k interface. This fact suggests that one can consider ternary high-k dielectrics from the viewpoint of tuning V_{th} as well as attaining higher-k films.

7.9 SUMMARY

This chapter has mainly discussed the dielectric properties of HfO_2-based films and the interface layer on Si substrate. On the basis of those results, we have proposed both interface

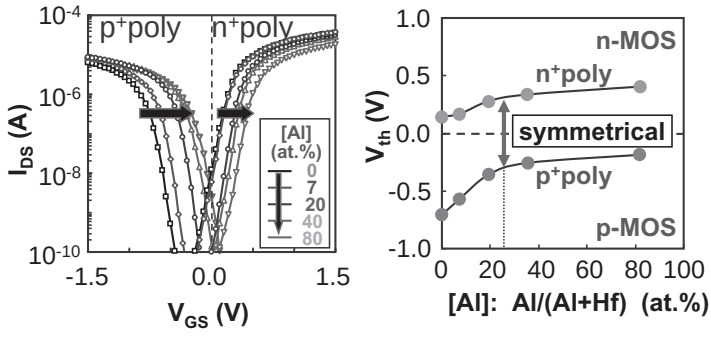

Figure 7.47 (a) I_{DS}-V_{GS} characteristics as a parameter of Al concentration in both n^+-poly-Si and p^+-poly-Si $HfAlO_x$ MOSFETs; (b) V_{th} values determined from the results in (a). V_{th} asymmetry is reduced with Al introduction and becomes symmetric at ~25 at.% Al in $HfAlO_x$ [93]

layer growth model at high-*k*/Si and design methodology for HfO_2-based dielectric film synthesis through the ternary metal oxide system. Y is chemically similar to La, but its doping effect on crystallization is dramatically different, possibly due to a large ionic radius difference between them. The Si-doping into HfO_2 has enhanced the *k* value, contrary to conventional expectations. When HfO_2 is considered to be the mother material, 'dopants' are classified into three categories such as '*crystallizer*', '*amorphizer*', and '*polarizer*'. This will be a useful guideline for preparing new dielectric materials.

Nitrogen effects, oxygen vacancies, and rare-earth oxides are now under investigation and will be reported in the near future.

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8 Physical Characterization of Ultra-thin High-*k* Dielectric

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8.1 INTRODUCTION

The scaling of silicon integrated circuit devices to smaller physical dimensions has been the primary activity of advanced device development since the start of this technology. This is pushed both by the need for higher performance, i.e., faster switching speed, and by the need to increase manufacturing profitability. As early as 1965, Gordon Moore observed that the number of bits on a memory integrated circuit was quadrupling every two years. This exponential increase of the density still continues today, but has now been reduced to a 3–4 yr cycle.

In metal–oxide semiconductor devices, the switching speed is proportional to the transistor drive current and inversely proportional to the load capacitance of the circuit

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($\sim I_{drive}/C_{load}V$). The drive current is the current flowing from the source to the drain and is written in the saturation regime as:

$$I_{drive}^{sat} = \frac{W}{2L_g}\mu_{eff}C_{ox}(V_G - V_T)^2$$

where W and L_g are the width and length of the channel, μ_{eff} is the effective channel mobility, C_{ox} is the gate oxide capacitance per unit area of the gate and V_G and V_T are the gate and threshold voltages. Ignoring quantum mechanical and depletion effects from the substrate and the gate, the oxide capacitance can be written in terms of the physical and electrical properties of the oxide as

$$C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}}$$

where ε_{ox} is the dielectric permittivity of the gate oxide and d_{ox} is the thickness of the gate oxide. Hence, the improvement of the transistor performance can be achieved by decreasing the gate oxide thickness, increasing the dielectric constant of the gate oxide, reducing the size of the transistor and/or increasing the mobility.

Historically, the gate oxide has always been SiO_2, and the thickness has been decreasing from the range 50–100 nm for the 4K NMOSFET DRAM to value of 1.2–1.5 nm equivalent oxide thickness (EOT) for leading edge MPUs. At these thicknesses, the total gate oxide is only a few atom layers thick, leading to large direct tunneling which increases exponentially with decreasing layer thickness. This leads to large leakage currents that are unacceptable. For instance, at a gate bias of 1 V, a decrease of the gate oxide thickness from 3.5 to 1.5 nm leads to an increase of the leakage current from 10^{-9} A/cm^2 to 1 A/cm^2. This led to the conclusion that SiO_2 needed to be replaced by another material with a larger dielectric constant, that would allow a larger physical thickness while keeping a low electrical thickness.

However, the requirements for new gate oxide materials are very stringent. Indeed, while the integration of SiO_2 with poly-Si requires only interfaces between Si and its oxide, the introduction of foreign material adds the presence of additional interfaces (Figure 8.1) that have to be controlled through the whole processing cycle. In addition, the high-k material has to fulfill a number of requirement such as:

- good thermal stability in contact with Si, preventing the formation of silicide at the interface and limiting the interfacial SiO_x layer,
- good thermal stability in contact with the gate,
- good thermal stability of the material itself, no phase separation for a binary oxide, for instance,
- large bandgap, symmetric on both sides of the Si bandgap preventing high leakage current both for holes and electrons,
- low interface trapped and fixed charge density in order to have a sufficient lifetime of the dielectric layer and high mobilities of charge carriers in the channel,
- deposition in very thin and uniform films.

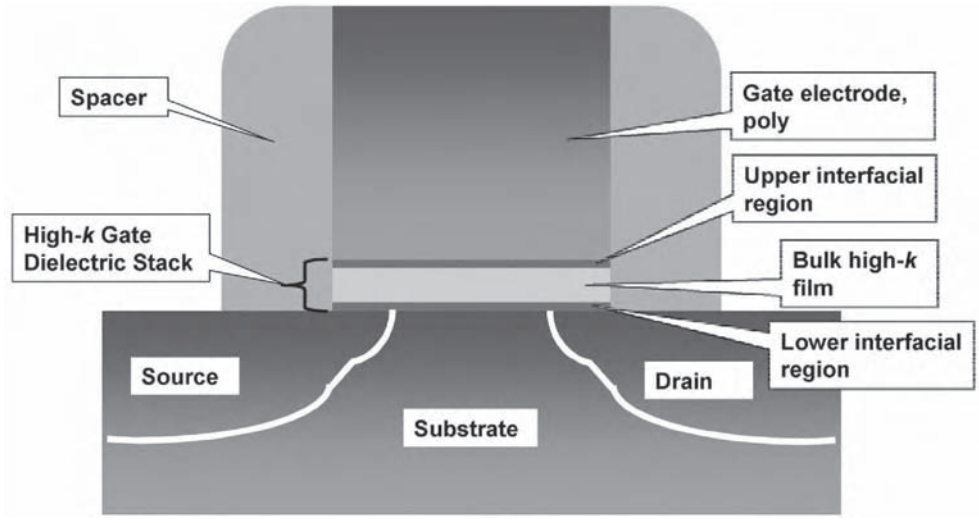

Figure 8.1 Schematic representation of a MOSFET transistor [82] (Reproduced with permission from Elsevier)

Due to the complex structure of the gate stack, and its influence on the electrical properties of the device, a detailed understanding of interfacial phenomena and of the quality of the grown layer is of primary importance. Considering, for instance, only the deposition of high-*k* layer on Si, one sees that the quality of the interface between the high-*k* layer and the Si substrate is fundamental for the achievement of the SiO_2 replacement. Si–O or Si–metal bonds at the interface would result in an interfacial layer with a lower *k* and/or a large density of traps. A low-*k* interfacial layer limits the scaling capabilities; the gate oxide is then composed of a low-*k* and a high-*k* layer and the total capacitance C_{ox} is limited by the lowest k layer $C_{low\text{-}k}$:

$$\frac{1}{C_{ox}} = \frac{1}{C_{low-k}} + \frac{1}{C_{high-k}}$$

The equivalent oxide thickness of the stack is then given by

$$EOT = d_{low-k}\frac{\varepsilon_{SiO_2}}{\varepsilon_{low-k}} + d_{high-k}\frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}}$$

hence, the minimum achievable EOT will never be less than the one of the lowest-*k* layer. As the target for high performance application is sub-nanometer EOT, the thickness of this interfacial layer has to be limited as much as possible.

Further, the interfaces are the preferential locations for trapping and a high density of traps at the interface would shift the threshold voltage to an unacceptable value. The quality of the interface is thus also crucial.

The first approach for the deposition of the high-*k* material on the Si substrate has been to grow it directly on the Si substrate in order to avoid the interfacial layer. However,

H. Bender *et al*. [1] have demonstrated the poor quality of the high-*k* layer deposited directly on Si. The density of the film is lower than the bulk density and it grows in an island mode, leading to pinholes in the film. Furthermore, it has been established that a high-quality Si-SiO_2 interface helps maintain a high channel mobility, as channel mobility degradation is reduced with increasing interfacial oxide thickness [2]. Even though the presence of the interfacial layer thickness limits the scalability, its presence has some beneficial effects. Similar reasoning applies to the oxide–gate interface.

This chapter will be structured around the main physical properties of the high-*k* system. We will successively analyze the surface preparation of the Si substrate, the growth mode of the high-*k* layer, the determination of its thickness, its composition (including contaminations) and its density. Then, we will look at interfacial characterization, contamination, determination of bandgap and band offset, crystallography and finally, the presence of defects.

8.2 SURFACE PREPARATION

Surface preparation is a crucial parameter for the final electrical characteristics of the gate stack. Ideally, in order to enable maximum scalability, one would like to grow the high-*k* layer on bare silicon and to keep the interface 'silicon oxide free'. However, this is seldom possible if high-quality layers are to be obtained. In addition, the optimal surface preparation will strongly depend on the technique that is used to grow the high-*k* layer. We will present here the influence of surface preparation for three different systems that pose different challenges: HfO_2 on Si by ALCVD, $SrTiO_3$ on Si by MBE and HfO_2 on Ge by MOCVD. The use of (sometime complex) surface preparation is needed to achieve high-quality high-*k* layer formation.

8.2.1 HfO_2 on Si by ALCVD

Due to its alternative saturating reaction mechanism, ALCVD seems to be an ideal technique for growing ultra-thin layers. However, as observed on Figure 8.2, large differences are observed in the amount of Hf deposited at each growth cycle as a function of the starting surface preparation [3–5]. In fact, the slowest growth is obtained on HF-last surface preparation (hydrogen-passivated, oxide-free surface) and the largest growth per cycle is observed on a chemical oxide interface, due to the presence of a large number of hydroxyl groups at the Si surface. The influence of surface preparation on the growth mode and the high-*k* layer quality will be discussed in more detail in subsequent sections. However, the presence of a silicon oxide interface is detrimental in view of the maximum scalability towards low-EOT layers.

It is thus important to optimise surface preparation in order to minimize the interfacial oxide thickness while preserving a large amount of hydroxyl group in order to preserve good growth quality.

The expected best method to cover the Si surface by a monolayer or more of hydroxyl is through the growth of a wet chemical oxide [6, 7]. When an ozone-based chemical oxide is formed, good thickness control can be obtained by controlling dip time, ozone concentration, temperature and additives. Figure 8.3 shows, for instance, the SiO_2 growth profile as

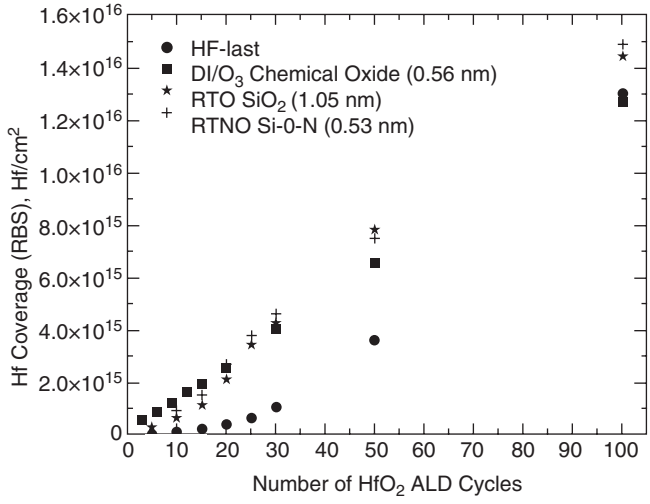

Figure 8.2 Hf coverage (atom/cm^2) as a function of HfO_2 ALCVD cycles for different surface preparation methods [3] (Reproduced with permission from the American Institute of Physics)

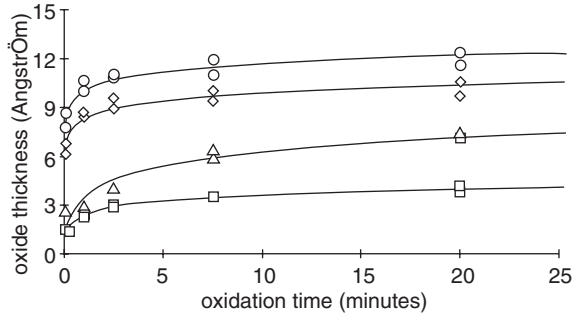

Figure 8.3 Growth profile of SiO_2 as a function of the ozone concentration under the following experimental conditions: T = 22 C, pH = 4.6, and 1 (squares), 5 (triangles), 15 (diamonds), 17.6 (circles)mg/L (Reproduced from J. Electrochem. Soc. 147(3), 1124–1129 (2000) with permission from ECS—The Electrochemical Society)

a function of the dip time and the ozone concentration. Using this kind of chemical oxide, very thin SiO_2 layers can be controlled reproducibly and low EOT can be achieved on Si surfaces [8]. It also shows the importance of the measurement technique for the determination of the SiO_2 thickness. Indeed, while ellipsometry is traditionally used in the semiconductor industry for thickness measurement, systematic errors are present for very thin films, due to the presence of airborne contamination on the wafer surface. Other methods are thus required, such as the molybdenum blue method [9] which is very precise, but only gives an average of the layer thickness on the whole wafer, or XPS [10], that can also be used for wafer mapping. For very thin layers, up to a factor of two can be observed between the thickness determined by ellipsometry and XPS [8].

8.2.2 $SrTiO_3$ on Si by MBE

While amorphous films are prime candidates for high-*k* materials as replacement for SiO_2, fully epitaxial layers are also considered as possible gate oxides for future generation of ICs. A common method for the growth of epitaxial layers is MBE (molecular beam epitaxy), although not so often for epitaxial oxides. Perovskite-type oxides such as $SrTiO_3$ are possible candidates for epitaxial high-*k* on Si as it has a high dielectric constant (~300 at room temperature) and a lattice mismatch of 1.7% with Si(100) when rotated 45° [11]. However, epitaxial growth requires careful surface preparation. Indeed, the direct deposition of $SrTiO_3$ on Si results in island-like growth [12] due to the growth of Sr silicate. Several approaches can be followed to circumvent this problem. First, Ishiwara proposed the deoxidation of the Si surface followed by the deposition of a thick SrO buffer layer [13]. Another technique is based on the desorption of the native Si oxide followed by the reaction of metallic Sr with the Si surface to form a stable strontium silicide that plays the role of a template for further epitaxial growth of the $SrTiO_3$ [14]. In addition, theoretical evidence suggests that precise control of the interfacial oxygen content is essential to obtain favorable band offsets for $SrTiO_3$ epilayers on Si(100) [15]. However, the Sr coverage window is relatively small and precise control of the amount of deposited Sr is crucial. This can usually be achieved by techniques such as RHEED, or XPS [16]. More recently, Norga *et al.* [17] have shown by a combined XPS–RHEED study on the Sr–Si system, with further deposition of BaO that the deposition of Sr at two different temperatures, an almost complete inhibition of Si oxidation is possible while growing the high-*k* layer.

8.2.3 HfO_2 on Ge by MOCVD

Another example where the importance of surface preparation is very clear is in the growth of HfO_2 on a Ge substrate. The main motivation for using Ge instead of Si in planar CMOS is its high mobility, required for high-performance applications [18].

As for Si, the growth of the high-*k* layer should start on an oxide-free Ge surface for the case of epitaxial growth (or possibly MOCVD), but the presence of a thin oxide layer may be important as a starting surface for ALD growth. In addition, the development of chemistries for Ge cleaning is also more complex due to the water solubility of GeO_2. A detailed XPS study of the oxidation/etching of Ge and GeO_x has been performed by Onsia *et al.* [19]. They show that a water treatment allows for the removal of most of the oxide layer (Figure 8.4), leaving the surface in a favorable state for ALCVD growth, with minimal interfacial layer thickness. On the other hand, the use of hydrohalogenic acids allows one to obtain an oxide-free Ge surface that could be favorable for epitaxial growth (Figure 8.5).

These Ge starting surfaces were tested for growth by ALCVD and MOCVD HfO_2 [20]. In addition, oxygen free Ge surfaces with an additional NH_3 pretreatment, in order to form GeO_xN_y, were evaluated. In all cases, high growth rates, without measurable inhibition at the start of the growth, were observed by RBS. However, the growth quality as observed by TEM varies greatly as a function of surface preparation. While uniform and smooth surfaces/interfaces are obtained for ALCVD layers, good-quality MOCVD layers are obtained only on GeON interfacial layers (Figure 8.6). It was shown by TOFSIMS that the low-quality MOCVD layers were due to extensive diffusion of Ge into the HfO_2 layer. The GeON layer thus plays the role of a diffusion barrier during the growth.

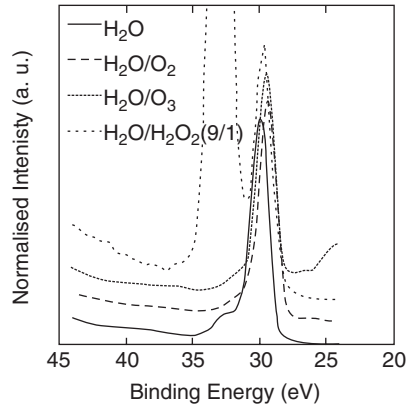

Figure 8.4 Ge 3d spectra of the Ge surface after various oxydizing treatments [19] (Reproduced with permission from Trans Tech Publications)

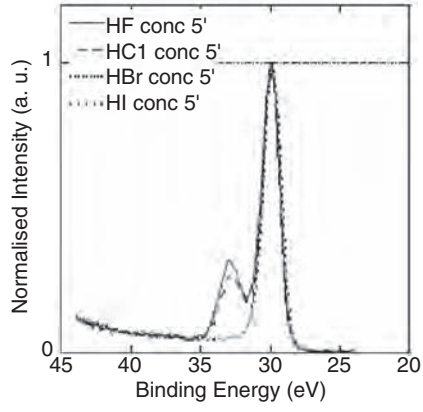

Figure 8.5 Ge 3d spectra from Ge surfaces treated with various hydrohalogenic acids [19] (Reproduced with permission from Trans Tech Publications)

8.3 GROWTH MODE

As seen earlier the quality of the layer grown on the substrate is heavily dependent on the surface preparation and growth technique. While many analysis techniques can give information about the growth quality, few can give detailed and fast real-time information on this growth quality. As a test case, we will present here the analysis of the ALCVD growth of oxide layers on Si substrates.

The first approach to look at growth quality is to investigate the growth curves, i.e., the evolution of film thickness as a function of time. However, this leads to the fundamental question of how to measure layer thickness, to be dealt with in the next section. In this section we will consider only the amount of material deposited, as can be measured absolutely by RBS, XRF or ICP-OES. This allows one to define the growth per cycle, i.e., the amount of deposited material after each cycle.

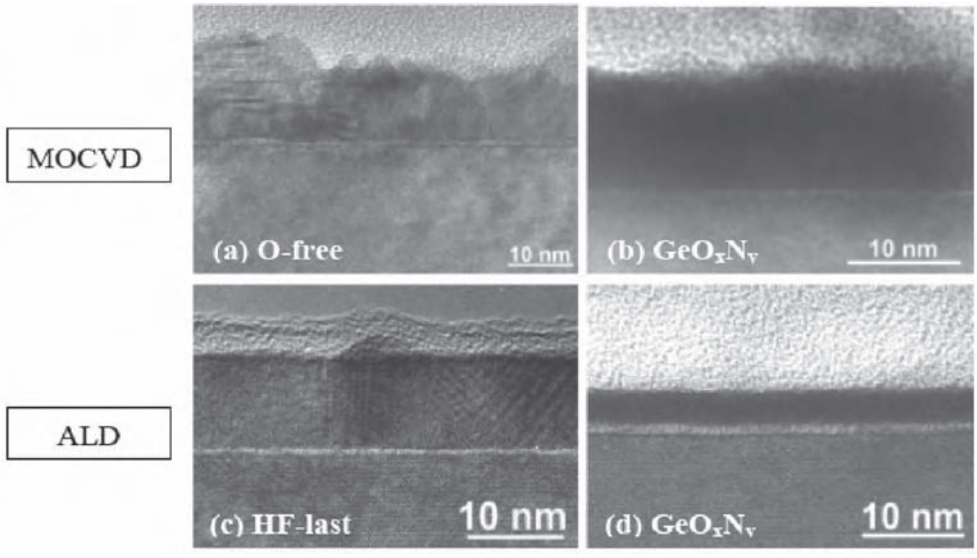

Figure 8.6 Cross-sectional TEM images of MOCVD HfO_2 on: (a) O-free (similar for HF-last) Ge; (b) MOCVD HfO_2 on NH_3 annealed Ge; (c) ALCVD HfO_2 on HF cleaned Ge; (d) ALCVD HfO_2 on NH_3 annealed Ge [20] (Reproduced with permission from Trans Tech Publications)

As has been shown in Figure 8.2, the evolution of the Hf coverage as a function of the number of cycles is strongly dependent on the Si surface preparation. This is a generally observed characteristic of ALCVD growth, but the main question is to determine how the layer quality is related to the different growth curves. An extensive study of the growth mode has been performed by Puurunen and co-authors [3, 21–24].

In order to determine the actual growth mode of the ALD films, a measurement of the surface coverage is needed. A powerful technique to achieve this measurement is LEIS (low-energy ion scattering), which can theoretically determine quantitatively the surface coverage of the high-*k* on Si. However, it also suffers from its surface sensitivity, as it requires special sample preparation to remove hydrocarbon surface contamination (for non-*in-situ* measurement), and is a rather slow measurement. Nonetheless, it has been shown that in the growth of ZrO_2 on Si, good linear anticorrelation between the Zr and Si signal was observed (Figure 8.7a), demonstrating the absence of a matrix effect in the ion intensities, and their possible use for surface coverage quantification.

Figure 8.7(b and c) show the calculated surface fractions S_{sub} and S_{ZrO2} as a function of the number of ALD reaction cycles, and the surface fractions as a function of ZrO_2 coverage, together with the theoretical calculation using either a two-dimensional growth model, or a random growth model. Obviously neither of the two models fits the experimental data correctly. It can be shown that an island growth mode gives a better description of the growth of ALD the ZrO_2 layer [21].

In some cases, the islanding during the growth of ALD layer can also be directly observed in TEM images such as in Figure 8.8.

The use of either LEIS or TEM to determine the growth mode is rather time consuming. From a technological point of view, a more qualitative analysis is often sufficient in order

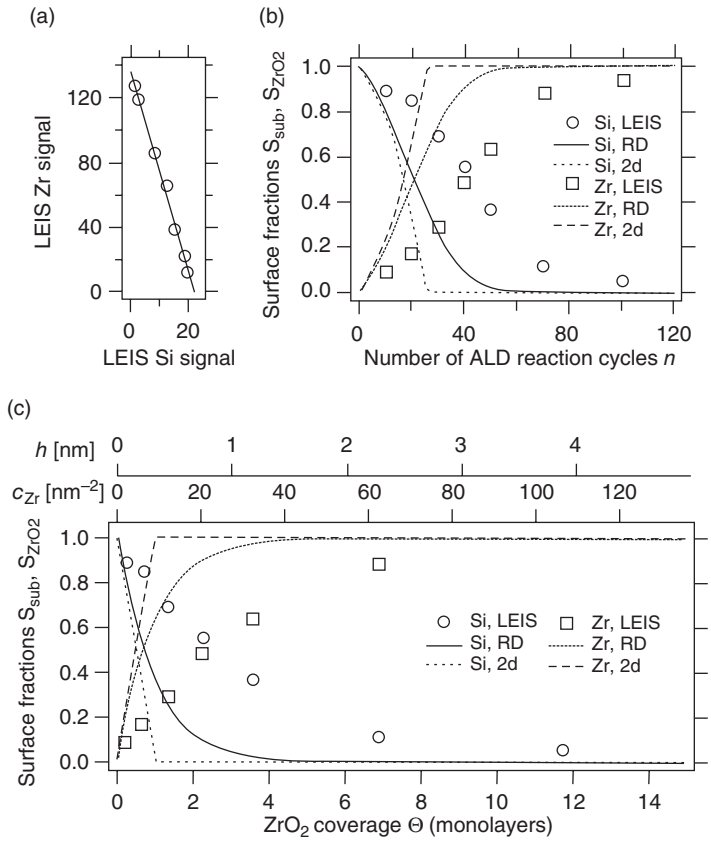

Figure 8.7 Results of LEIS measurements for ZrO_2: (a) linear dependency between the Zr and Si signals; (b) the calculated surface fractions S_{sub} and S_{ZrO2} as a function of the number of ALD reaction cycles; (c) the surface fractions as a function of ZrO_2 coverage. 2d refers to two-dimentional growth; RD random growth. In (c), the upper *x* axes show the amount of ZrO_2 deposited c_{Zr} (nm^{-2}) and the average film thickness h (nm) assuming $r = 5.6\,g\,cm^{-3}$ [21] (Reproduced with permission from the American Insitute of Physics)

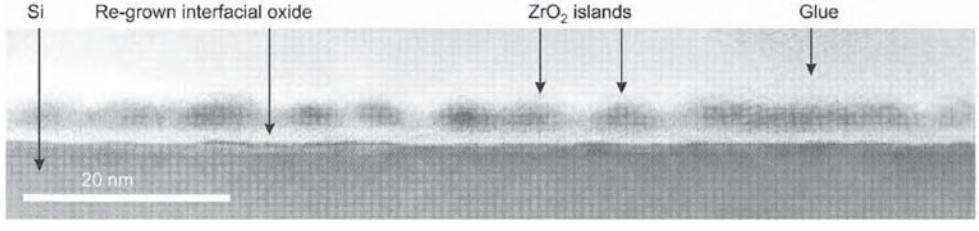

Figure 8.8 Cross-sectional TEM image for ZrO_2 deposited in 60 $ZrCl_4$/H2O cycles at 300°C on hydrogen-terminated silicon, pretreated with H2O at 300°C for 5 min. Reoxidation of the silicon substrate has taken place due to exposure to ambient air [21] (Reproduced with permission from the American Institute of Physics)

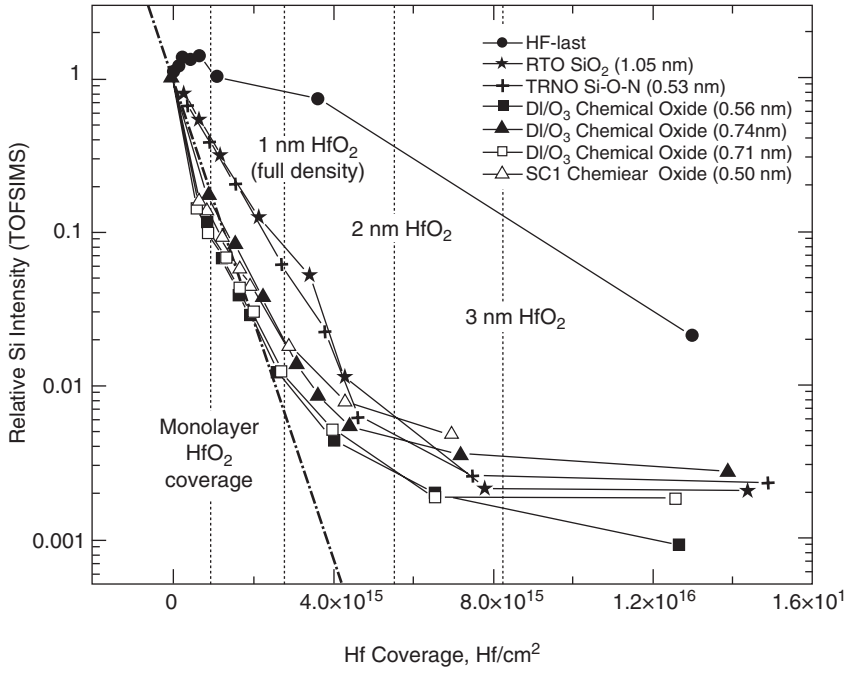

Figure 8.9 Si TOFSIMS profiles for ALD HfO2 films grown on various underlayers. The dashed line at left is the expected decay of the Si intensity for perfect two-dimensional HfO_2 film growth, using an escape depth of 0.2 nm for the secondary ions [3] (Reproduced with permission from the American Institute of Physics)

to determine how far the growth process can be scaled down in thickness. The use of TOF-SIMS has thus been developed in order to allow a fast screening of the growth quality of a given material on different surfaces [25]. Similarly to LEIS, TOF-SIMS allows one to determine the closure of thin layer due to the limited escape depth of the ions. During the growth of an overlayer, a fast decay of the substrate intensities will thus be observed as soon as this overlayer fully covers the substrate. This technique has been applied successfully for the analysis of the ALCVD growth of HfO_2 on Si, which showed a good correlation between the amount of OH–groups at the surface of the Si and the decay of the Si intensity (Figure 8.9) [3].

8.4 FILM THICKNESS

Thickness control is a key parameter to monitor any deposition process, either in a production line or for process development. This is especially true for gate dielectric thickness monitoring, as the gate oxide thickness is a fundamental parameter to control in order to achieve high device performances. Ellipsometry has always played a prominent role for thickness control of dielectrics because it is fast, nondestructive and very accurate for layer thicknesses above ~10 nm [26]. Spectroscopic ellipsometry in the UV range is theoretically more accurate than in the visible for thin layers, but in practice, below 30 Å, practical

problems arises from the presence of surface contamination and modification of the refractive index for thin layers, even in the case of SiO_2.

When introducing alternative gate dielectrics, the ellipsometry problems became even more serious, due to the presence of compositional changes in the gate dielectric, and to the presence of multiple (interfacial) layers forming the gate dielectric [27] leaving the metrology of, even silicon oxynitride, for example, an unsolved problem.

The most commonly applied techniques for thickness measurement (besides SE) are XPS, RBS, TEM, XRR and XRF. Unfortunately, each of them measures a different parameter from which film thickness is inferred. For instance, while TEM provides a direct measure of the physical thickness, it is rather insensitive to film density. On the other hand, RBS and XRF directly measure the number of atoms/cm^2, which can be converted to thickness if the density is known. Ideally, XRR provides film thickness and density simultaneously; however, for a thin film, a single-layer fit usually yields a reasonable value, even for a multiple layer, and even more in the presence of surface/interface roughness [27]. The problems of density measurements will be exposed in the next section.

With X-ray photoelectron spectroscopy the thickness of thin overlayers can be calculated by the measurement of the overlayer and substrate signal, taking into account the attenuation of the signal with the distance travelled, i.e., the overlayer thickness [28]. Major parameters playing a role in these calculations are the effective attenuation lengths, which, notably, depend on the material densities. The thicknesses obtained by XPS are usually much lower than by ellipsometry, mainly for very thin layers, suggesting that the properties of the layer are different from the bulk materials. An extension of the XPS thickness measurement is possible for multilayer system when performed in an angular resolution mode.

Rutherford backscattering (RBS) and elastic recoil detection (ERD) yield surface coverages of the elements which can be converted to thickness values if the material density is known. RBS is applied to measure the Hf coverage using 1 or 2 MeV He^+ (Figure 8.2) or 40 MeV Cu^+, while the H, O and C content are obtained with 40 MeV Au^+ ERD.

ATR-FTIR is also usable for thickness measurement, but only after calibration for conversion of the absorbance to thickness values.

One of the major issues of ellipsometry is shown in Figure 8.10, which shows optical parameters for HfO_2 layers deposited by ALD or MOCVD. These data were obtained from

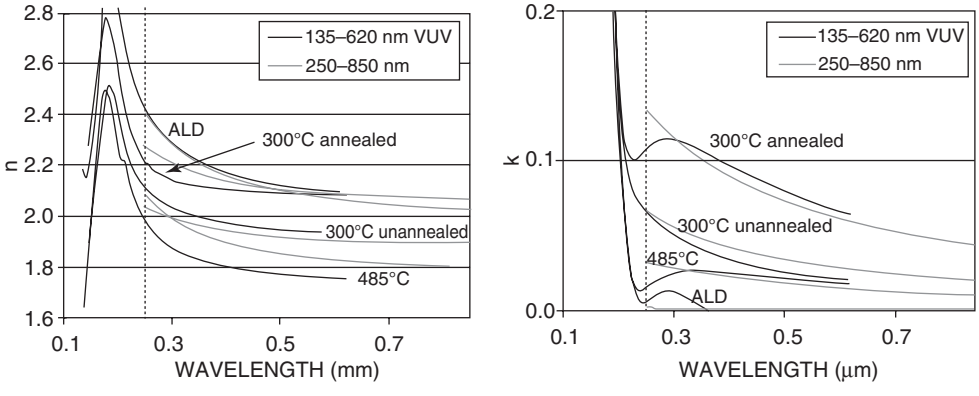

Figure 8.10 Optical parameters n,k as determined by spectroscopic ellipsometry in the range 250–850 and 135–620 nm for thick HfO_2 layers deposited by ALD and MOCVD (deposited at 300 and 485°C) [83] (Reproduced with permission from the Electrochemical Society, Inc.)

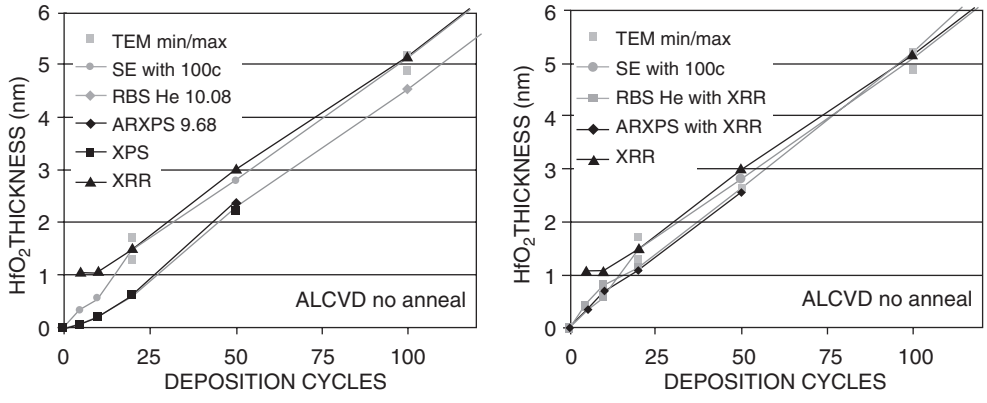

Figure 8.11 ALD HfO_2 thickness versus the number of deposition cycles, as analyzed by (a) TEM, SE using optical data derived from 100-cycle samples, RBS with He beam, single angle and angular resolved XPS, and XRR fitting both the thickness and the density; (b) after recalculation of the RBS and ARXPS data with the densities as obtained by XRR for each sample [83] (Reproduced with permission from the Electrochemical Society, Inc.)

thick layers (50–100 nm). The results of Figure 8.10 show that three different classes of materials can be considered with high, medium and low refractive index values, respectively. Correlation with XRD and TEM shows that these layers are crystalline (cubic or monoclinic), amorphous/nanocrystalline, and highly textured porous with a monoclinic phase, respectively. The parameters determined for these thick layers can then subsequently be applied to determine the thickness of the thin layers, which are prepared or annealed under similar conditions (Figure 8.11). For the VUV-data the starting values for the thickness are taken from the XRR analysis, which is performed with the same instrument [6]. Doing so, ellipsometry shows weak incubation of initial growth for the ALD layers, and linear growth for the MOCVD layers. However, this fully neglects the possible presence of an interfacial layer.

An example of the comparison of the thickness determined by different measurement techniques is shown in Figure 8.11. Using the bulk density of crystalline HfO_2 leads to a wide spread of the thickness obtained with the different techniques. Except for XRR, all growth curves show incubation in the initial growth stage. For the thickness range considered in this graph the density is lower than the bulk density and is thickness dependent (Figure 8.12).

Recalculation of the thickness with these deposition cycle dependent densities results in a much-improved correspondence between the different techniques. For the thicker layers the agreement between SE, TEM, RBS (He), ARXPS and XRR is excellent. For the thinner layers the incubation effect is now compensated by the much lower density obtained by XRR for these layers. The XRR thickness for the thinnest layers seems to be higher than for the other techniques, suggesting that the analysis model should be changed. Similar improvements for the agreement between the various analysis techniques are also obtained for the MOCVD layers. The discrepancies remaining for very thin layers measured by SE is due to the presence of surface contamination.

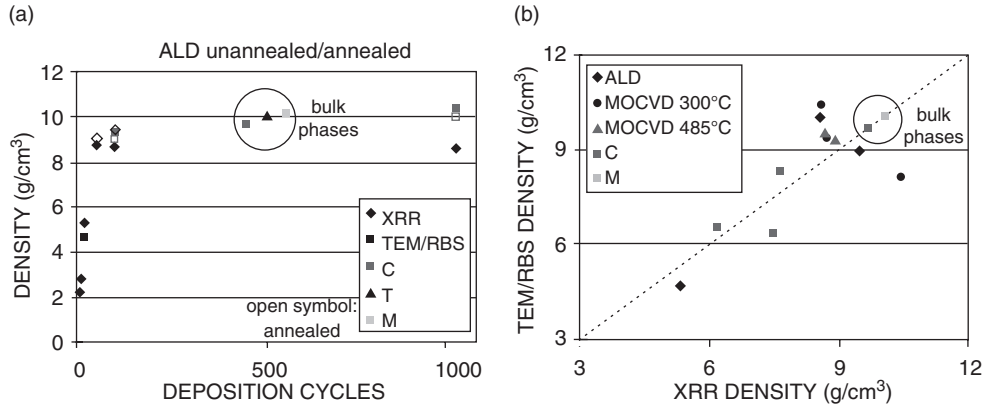

Figure 8.12 (a) Density versus number of deposition cycles for ALD HfO_2 as determined by XRR and TEM/RBS; (b) comparison of the XRR and TEM/RBS densities for ALD, and MOCVD samples grown at two different temperatures. The calculated density for cubic, tetragonal and monoclinic HfO_2 are indicated for comparison [83] (Reproduced with permission from the Electrochemical Society, Inc.)

8.5 DENSITY

As seen for the thickness determination, knowledge of the density of the thin gate oxide is a crucial parameter both for physical characterization purposes and also from a technological point of view. For example, low film densities could lead to enhanced layer modification upon annealing, thereby favoring the presence of trapped charges, which are detrimental for electrical performances. From a physical characterisation point of view, it is also a crucial parameter, as it will influence many measurements. Most techniques, except TEM and XRR, rely directly or indirectly on the material density to determine other parameters such as the layer thickness. As a consequence, these two techniques are usually used for density determination [83, 29]. The density of the films is strongly influenced by the deposition method, film thickness and other process parameters [83, 30]. For instance, Figure 8.12 shows the density increase observed for ALD HfO_2 films as a function of the number of deposition cycles. It shows that for all thicknesses technologically relevant for the gate oxide application, the density is significantly lower than for the bulk phase. The bulk phase density is reached only for very thick films. The comparison of the densities obtained by XRR and TEM/RBS is presented in Figure 8.12(b) for films grown by both ALCVD and MOCVD at different temperature, and shows a reasonable correlation between the two techniques. Some of the data points show a poorer correlation, but these data points are for the thinnest films. However, for very thin films, the XRR spectrum shows little structure and the correlation between the different parameters becomes questionable. As most of these films have low impurity concentrations, the low densities are expected to be due to noncontinuous layer structure in the form of island growth or pores.

However, even the densities determined as above may be questionable. A very detailed analysis of density data for very thin films was performed by Puurunen *et al.* [31]. It was indeed observed that, despite the low density measured for thin ALD films, no change was observed in the dielectric constant of HfO_2 films, as measured by *C–V*, even for the thinnest films. In fact, it was shown that the low observed densities have their origin in a number

of errors made in the determination of the layer thickness by TEM. These factors include:

- roughness of the substrate film bottom interface,
- roughness of the top surface of the film,
- island-like morphology of the ALD-grown films,
- impurities in the bulk of the film,
- impurities at the film/substrate interface,
- airborne contamination at the surface of the film,
- mixing of the bottom interface between the HfO_2 and the Si substrate.

When all these factors are taken into account, an overestimation of the layer thickness by TEM is evaluated to be at least 1.05 nm. This value is large enough to explain the low observed densities and thus shows that these low observed densities are mostly an artifact of the measurement technique. It can thus be concluded that no adequate technique is available for a good characterization of the densities of thin films.

8.6 COMPOSITION

Compositional analysis of high-*k* dielectrics is another challenge in the physical characterisation of high-*k* layers. Indeed, while a wide range of techniques can be applied to retrieve compositional information on layers, none covers the whole range of sensitivity/depth resolution needed. Compositional determination is not only needed for thin homogeneous layers, but also for multilayers, or layers with a gradient in their composition. Further, the presence of contamination in the layer, even at a very low level, can induce large changes in the electrical characteristic of the layers. We can divide the compositional analysis into three different applications: bulk composition analysis (main matrix elements); analysis of the layer contamination; and finally, the characterization of the interfacial layer. If the interfacial layer could be considered as part of the bulk composition analysis, the specific problems arising from possible interaction with the substrate deserve special attention [4, 5, 11, 29, 30, 32–47, 59, 68, 72, 74].

8.6.1 Bulk composition

While binary oxides such as HfO_2 or ZrO_2 were the main focus of high-*k* research, their low crystallization temperature led to the study of mixed oxides (aluminates, silicates), or to the incorporation of other elements such as nitrogen. The advantage of ternary oxides is illustrated in Figure 8.13, which shows the changes in crystallization temperature, bandgap and dielectric constant as a function of Al_2O_3 concentration for HfAlO oxide. Even moderate incorporation of Al_2O_3 leads to a significant increase of the crystallization temperature. It then becomes important to determine the composition of the layer and/or composition variation in the thickness of the film.

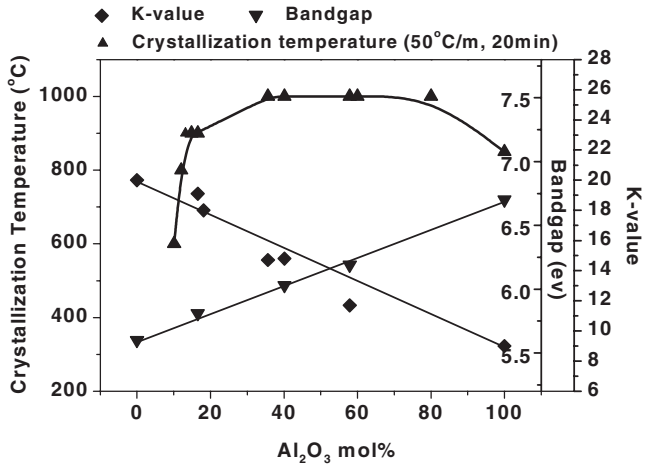

Figure 8.13 Changes of crystallization temperature, dielectric constant and bandgap for HfAlO oxide as a function of Al_2O_3 concentration [84]

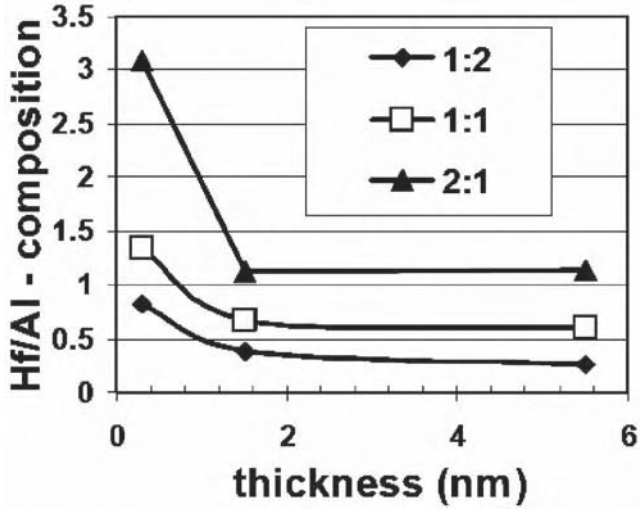

Figure 8.14 Composition of the HfAlO films grown by ALCVD as a function of the film thickness for different cycle ratios [85] (Reproduced with permission from the American Institute of Physics)

For instance, in ALD, the mixed oxides are grown with alternating cycles of the individual components. As the growth rate per cycle is much lower than one monolayer, mixing occurs on an atomic level, and homogeneous films are expected. However, the growth rate is also dependent on the surface composition, and the composition at the interface may not be identical to the bulk composition in the bulk of the sample. In fact, when the composition of the film is determined by XPS or RBS, a dependence of the composition is observed on film thickness (Figure 8.14); it shows a strong preferential deposition of Hf at the beginning of Hf–Al–O growth. However, these techniques do not have sufficient depth resolution

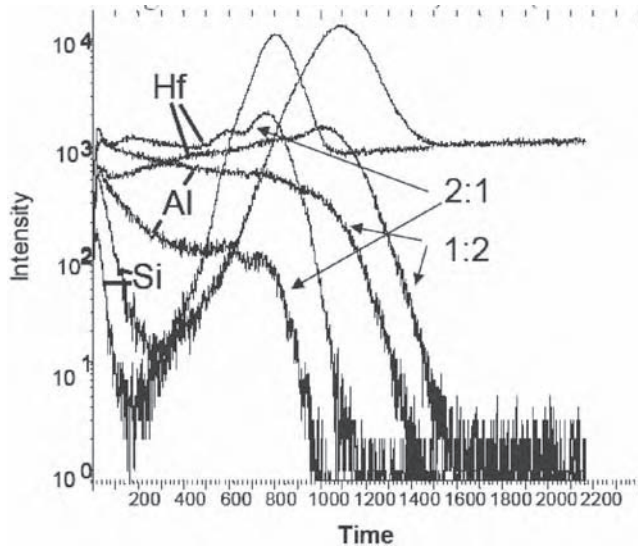

Figure 8.15 TOF-SIMS depth profile for HfAl oxide films (cycle ratio 1 : 2 and 2 : 1) [85] (Reproduced with permission from the American Institute of Physics)

to determine a real depth profile. Only a few techniques have the potential to achieve the needed depth resolution: TOFSIMS, ERDA, MEIS, and possibly Angle resolved XPS.

Figure 8.15 shows a profile obtained by TOF-SIMS using low-energy (500 eV) sputtering ions. It shows a strong nonuniformity of the layers, with enrichment at the interface with Si, and sloped profiles for both Al and Hf. However, despite a reasonable agreement with the results expected from the XPS and RBS data, from the nonlinearities of the SIMS signals with composition it is observed that only a limited variation of the Hf signal is present. The nonlinearity must be linked to changes of ionization probability with layer concentration. These are likely to be smaller for Al than for Hf, as the ionization potential for Al is smaller than that of Hf, making the ionization less sensitive to surface chemistry.

In order to overcome the limitation of TOF-SIMS profiling, nuclear techniques such as MEIS or ERDA allow for quantitative profiling of the layers [5, 41, 43, 46, 47] and subnanometer depth resolution can be obtained. Figure 8.16 shows such a profile obtained using a high-energy (40–170 MeV) heavy element (I-Au) used to elastically scatter lighter elements out of the target. A depth resolution of ~0.5 nm/decade can be obtained, and the sloped profile of the Al and Hf concentration is easily observed. It also shows that the surface of the layer is Hf-free, suggesting that some phase separation occurs, resulting in some Al floating on the surface. The different slopes of the Hf and Al concentration also show surface migration of Al and Hf, leading to an Hf-rich interface. Similar phenomena had already been observed in ZrAlO by ARXPS [64].

Another alternative technique for high-resolution depth profiling is ARXPS. Due to the angular dependence of the effective electron mean free path, the angular dependence of XPS intensities can be converted to a quantitative depth profile. An example of such a reconstruction is given in Figure 8.17 for a HfO_2/Al_2O_3 bilayer grown by ALCVD on a

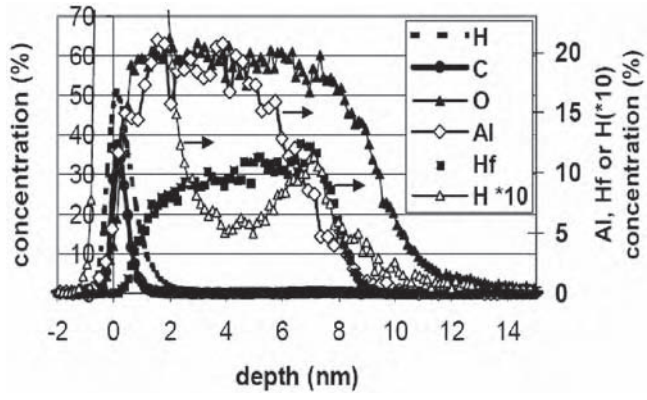

Figure 8.16 ERDA profile of a HfAlO oxide [85] (Reproduced with permission from the American Institute of Physics)

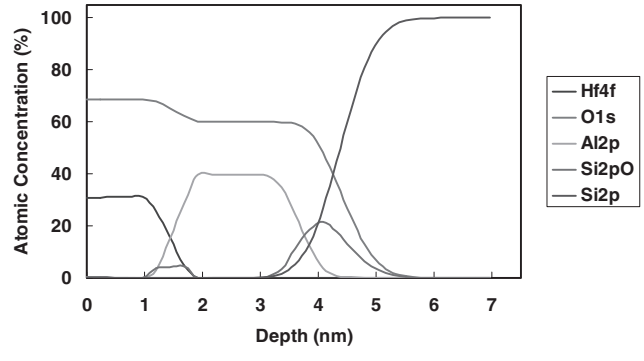

Figure 8.17 Reconstructed depth profile from a HfO_2/Al_2O_3 by layer deposited on a chemically formed SiO_2 interfacial layer [88] (Copyright Thermo Electron Corporation)

chemically formed SiO_2 layer. Very good depth resolution is obtained, together with a clear profile. It should however be mentioned that, due to the complex mathematical procedure required to obtain the depth profile, this technique is not universally applicable.

8.6.2 Contamination

In most chemical vapor growth techniques, a chemical reaction of the precursor gives rise to the high-*k* layer formation. The chemical reaction can lead to the presence of precursor's residue in the films and the inclusion of impurities. It is thus necessary to perform contamination analysis. As changes in the impurity distribution in the film can lead to modification

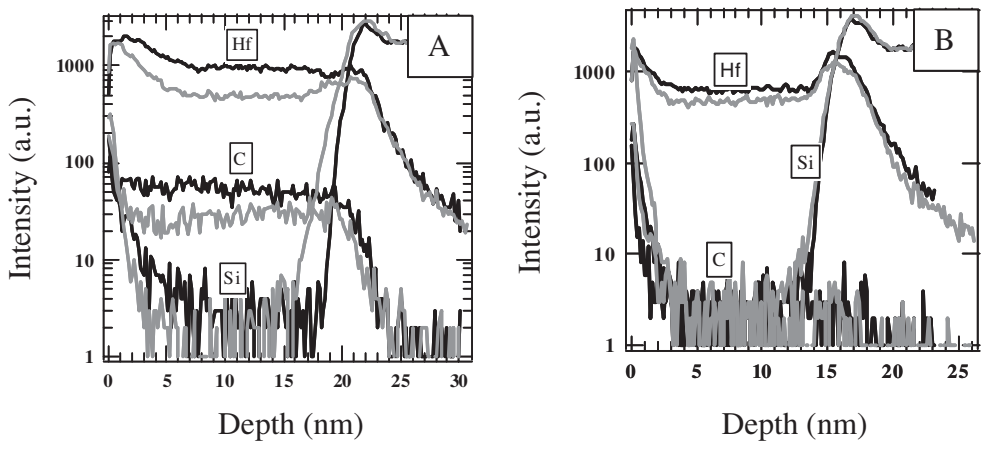

Figure 8.18 TOF-SIMS depth profiles for HfO_2 layers deposited at 300 (A) and 485°C (B) before (black curves) and after a 5 min, 900°C N2 anneal (gray curves) [86] (Reproduced with permission from the Electrochemical Society, Inc.)

of the electrical performances, both a good depth resolution and a high sensitivity is needed. Contamination analysis is thus often done by TOF-SIMS [36, 40].

Figure 8.18 shows TOF-SIMS depth profiles obtained on MOCVD grown HfO_2 layers at two different temperatures, and with/without post-annealing. A clear C profile was recorded throughout the sample deposited at 300°C, while the C signal for the 485°C sample was below the detection limit. The lower C levels at higher deposition temperatures can most likely be explained by a more efficient oxidation of the precursor.

Additional information can also be obtained from nuclear techniques (Figure 8.16), mostly for light elements such as hydrogen that cannot be well quantified by TOFSIMS, or by TXRF, for heavier elements when no depth profiles are needed [36].

For Cl-based ALD extensive studies are made on the presence of chlorine in the films. They show, that process parameters such as length of the pulse, purge time and process temperature have a major influence on the Cl concentration both in the bulk of the layer and at the high-*k*/Si interface [48].

8.6.3 Interfacial layer characterization

One of the critical issues in obtaining high-quality high-*k* films with very low EOT is control of the interfacial oxide. Ideally, no silicon oxide should be present, as this will impact the available capacitance budget for the high-*k* film. However, as seen before, the presence of an interfacial oxide can have a positive impact on the growth of the high-*k* film, and also on the enhanced mobility obtained with the stack. As such, analysis of the interfacial layer thickness and composition could be seen as part of the analysis of the high-*k* layer; however due to its specific importance, it is dealt with independently here. A good metrology of this interfacial layer must be developed.

Due to the thickness of the gate stacks, XPS is one of the most important characterization techniques; it yields both chemical and thickness information for the full stack.

The formation of the interfacial layer is strongly influenced by both the growth method and post-processing of the high-*k* stack. As an example, Figure 8.19 shows the interfacial layer thickness measured by XPS during MOCVD HfO_2 growth. It is observed that both on a starting SiO_2 surface and an oxide-free surface, an interfacial layer arises during growth, and it consists of a silicate-like layer, as interpreted from the binding energy shift of the Si 2p photoelectron peak. One must be careful in interpreting binding energy shifts, since charges at the high-*k*/Si interface can also induce a significant shift of the Si 2p peak, as has been shown by Opila *et al*. [49]. Using synchrotron radiation and angle-resolved XPS, higher energy resolution and a better chemical analysis of the stacks can be obtained

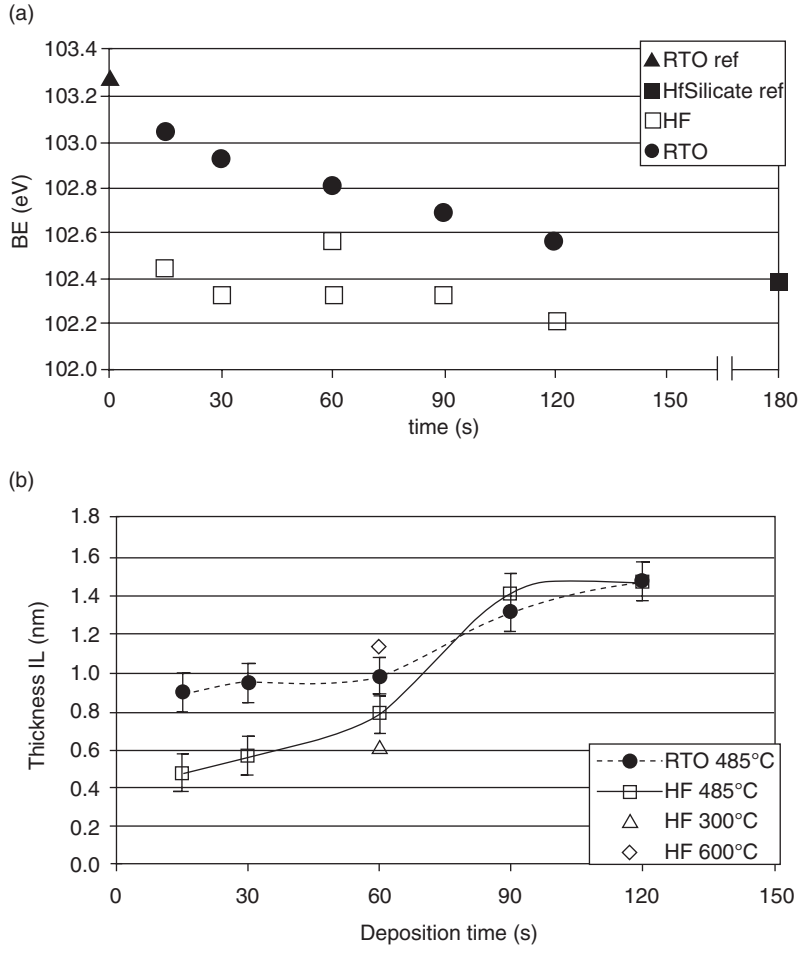

Figure 8.19 (a) Maximum value of the BE of the oxidized Si 2p peak as determined from the XPS spectra, plotted as a function of the MOCVD HfO_2 deposition time. All layers were deposited at 485°C; (b) thickness of IL as a function of deposition time for an RTO and HF-last starting surface. Thickness of the IL is calculated assuming the IL to be pure SiO2. IL thickness increases as a function of deposition time for both starting surfaces [87] (Reproduced with permission from the Electrochemical Society, Inc.)

and this technique was used to characterize the $HfO_2/SiO_x/Si$ stack (Figure 8.20) [45]. This study concluded that the HfO_2/Si interfacial layer for ALCVD grown HfO_2 is formed by a SiO_x layer underneath a Si-rich Hf silicate layer. This interfacial layer grew upon annealing due to remaining OH groups from the ALCVD growth.

Unfortunately, photoemission as a mean of understanding the interfacial layer has a number of limitations. For example, during the annealing of AlZrO oxide under nitrogen, the experimentally determined thickness of the interfacial layer appeared to increase, while when measured by TEM [65] it appeared to decrease (Figure 8.21). A multi-technique approach lead to the conclusion that in-diffusion of Si occurred upon annealing, that led to an apparent decrease of the interfacial layer, as measured by TEM, due to the change in contrast and to the apparent increase of the XPS thickness as a consequence of the larger Si–O intensity.

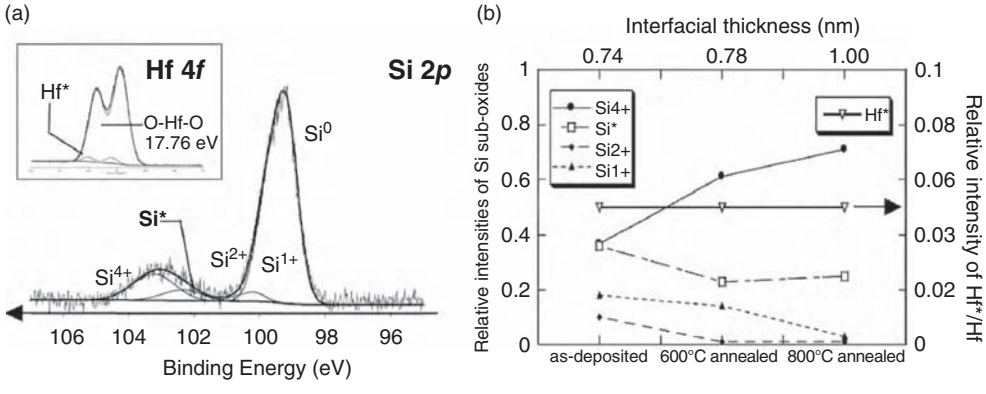

Figure 8.20 ARXPS analysis of *p*-Si/SiOx/2.5 nm HfO_2 stacks. (a) Si 2p and Hf 4f core-level spectra after annealing at 600°C; (b) estimation of interfacial layer thickness and interfacial layer structure by the evolution of the relative intensities of the spectra component as a function of treatment [45] (Reproduced with permission from Elsevier)

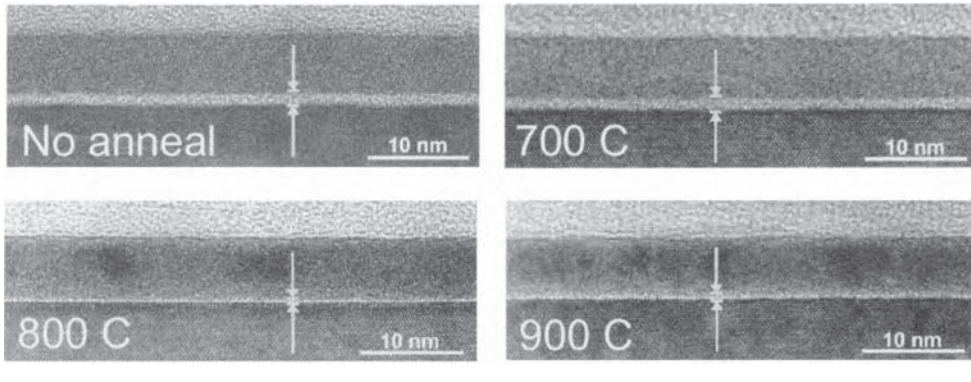

Figure 8.21 TEM pictures of 50 cycles AlZrO on 0.5 nm RTO annealed at different temperatures [65]

In order to improve layer thickness/composition analysis of the interfacial layer, one has thus to look for a depth profiling technique. The most common ones are ARXPS, MEIS and/or XRR [74, 88]. In this case, diffusion of the Si into the HfO_2 layer upon annealing can be clearly observed (Figure 8.22).

One of the main limitations of XPS/MEIS/ERDA, is that high depth resolution is limited to very thin layers and that they cannot be applied on real devices due to poor lateral resolution. When devices have to be characterized, one must therefore rely on TEM, which combined with EELS provides insight in the interface chemistry. An example of the power of this technique is shown in Figure 8.23, which shows a thin SiO_x at the substrate interface, and no low-*k* layer at the HfSiO–TiN interface. It also reveals the presence of nitrogen at the silicate/substrate interface and of an oxidized layer between the TiN and poly-Si layer. Even without the size limitation, an ARXPS measurement of the same high-*k* stack would be extremely difficult, as the signal from the SiO_x interfacial layer would be mostly hidden by the Si signal from the silicate layer. However, the TEM/EELS approach also suffers from limitations when heavy elements are present in the stack, or when roughness is present simultaneously with interlayer diffusion [34].

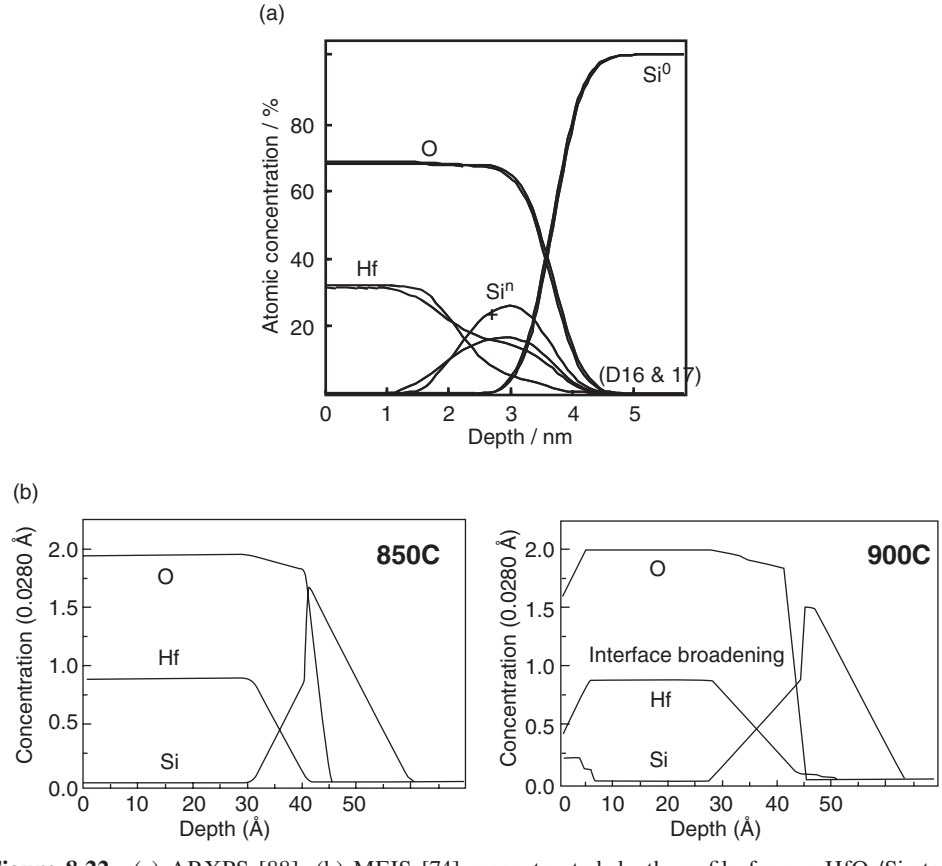

Figure 8.22 (a) ARXPS [88]; (b) MEIS [74] reconstructed depth profile from a HfO_2/Si stack before and after annealing (Reproduced with permission from Elsevier)

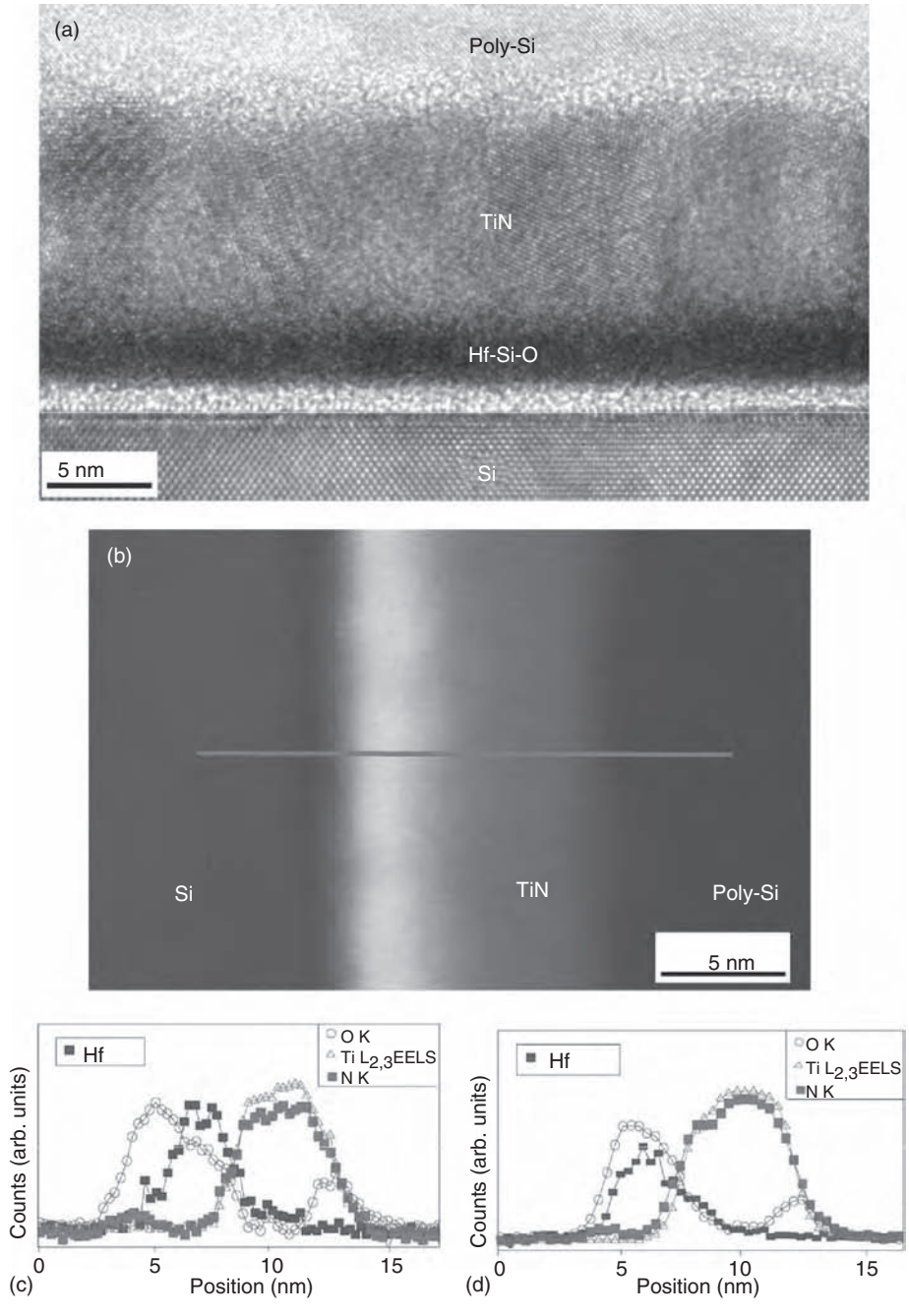

Figure 8.23 (a) Conventional HRTEM image of a MOCVD Hf–Si–O film capped with a TiN/poly-Si gate electrode stack; (b) HAADF image of the same stack. The bright layer is the Hf–Si–O. An interfacial oxide was observed between the Si substrate (left-hand side of image) and the high-*k* layer. The interface between Hf–Si–O and TiN shows significant roughness; (c, d) EELS and EDS chemical profiles with two different spot sizes, corresponding to (c) ~3 Å and (d) ~5 Å, respectively. Nitrogen is detected at the substrate interface and an oxygen-rich layer is present between the TiN and the poly-Si. Apparent spreading of Ti and N into the high-*k* layer is due to interfacial roughness [34] (Reproduced with permission from Elsevier)

8.7 BANDGAP AND BAND OFFSET

Analysis of bandgap and band offset is useful in order to optimize the high-*k* stacks for their electrical performances, for example leakage current. Band structure analysis can lead to the search of optimized stacks where 'natural' band alignment are unfavorable, such as in the $SrTiO_3$/Si system [15, 50]. A large number of systems were studied for their band alignment characteristics [16, 51–62].

A common technique to detect band alignment is photoemission. It has the advantage of simplicity and also provides both bandgap (from O 1s photolectron measurements) and band-offset (from valence band measurements) data. Further, it allows one to easily study the influence of processing on modifications of the bandgap and band-offset.

For ZrO_2 and Al_2O_3, Nohira *et al*. [57] showed that no dependence of the bandgap and band-offset value were observed as a function of film thickness. Bandgap values of 6.7 eV for Al_2O_3 and 5.4 eV for ZrO_2 were measured and are very close to reported bulk values, even for films as thin as 0.6–0.9 nm. A similar observation is made for the valence band-offsets with Si that were determined as 2.9 eV and 2.5 eV for Al_2O_3 and ZrO_2, respectively. More recently, Vitchev *et al*. [58] and Xie *et al*. [59] (Figure 8.24) showed similar results for HfO_2, and found a bandgap of 5.75 and a valence band-offset of 2.53 eV, respectively.

Next to HfO_2, hafnium aluminates and silicates are strong candidate for high-*k* gate dielectrics in low power application. Interestingly, a large difference of the bandgap and band-offset evolution between these two families is observed as a function of Hf content. Bandgaps and band-offsets of Hf silicates have been studied by photoemission as a function of the layer composition [56], and the results are presented in Figure 8.25. A stabilization of bandgap and band-offset values are observed for large Hf concentration (above ~0.75). Very similar results are obtained for zirconium silicates [63]. This is explained by the fact that the highest portion of the valence band is composed of nonbonding O 2p states, and the O atom coordination increases with increasing Hf content, which in turn leads to reduction of the valence band-offset. The change to a constant value for high Hf content is attributed to a discrete increase in O atom coordination due to the change of the bonding form dative to ionic [63].

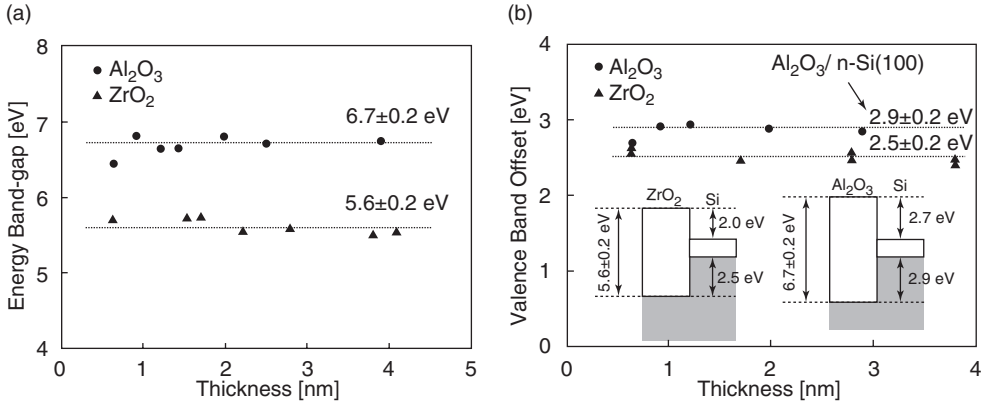

Figure 8.24 (a) Energy bandgap; (b) band-offset of ALCVD grown Al_2O_3 and ZrO_2 thin film as a function of the film thickness, as determined by XPS [57] (Reproduced with permission from Elsevier)

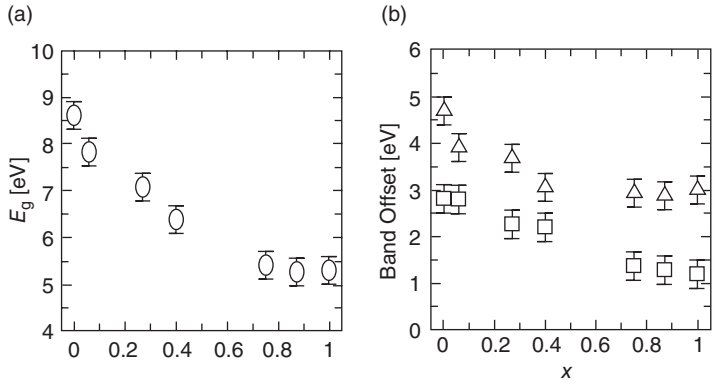

Figure 8.25 (a) Bandgap energy; (b) energy offsets for the conduction band (squares) and for the valence band (triangles) at the silicate/Si interface, as a function of the Hf content [56] (Reproduced with permission from the Institute of Pure and Applied Physics)

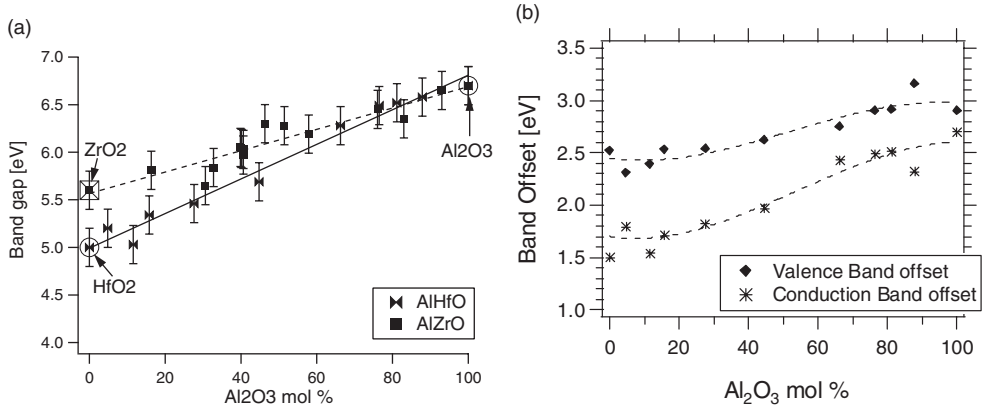

Figure 8.26 (a) Bandgap; (b) band-offset with Si for $Hf_{(1-x)}Al_xO$ as a function of the Al_2O_3 molar fraction, as determined by XPS from [62] (a) and [64] (b) (Reproduced with permission from Elsevier)

Figure 8.26 shows the changes in bandgap and band-offset with Si for Hf aluminates as a function of the Al_2O_3 molar content, as measured by XPS [64]. Similar measurements were performed by Yu *et al.* [54]. Both authors found a linear dependence of the bandgap value on sample composition; however, Petry [64] found some flattening of the band-offset value for low Al_2O_3 composition, while a linear variation was observed by Yu *et al.* The origin of this constant value for low Al_2O_3 concentration is assumed to be similar to that observed for the silicates. The fact that this flattening of the band-offset was not observed by Yu may be due to his more limited data set used at low Al_2O_3 concentration. The observation of a linear variation of the bandgap with composition is however not compatible with the constant value of the band-offsets. This suggests that the precision of the data is still

too limited to draw firm conclusion on the evolution of the band energies as a function of composition.

Photoemission can also be used to monitor the changes in the band alignment upon annealing. This is important, as full device processing will include different annealing schemes. For instance, Fulton *et al*. [51] studied the influence of annealing of ZrO_2 layers under vacuum, and the influence of interfacial layer thickness on the modification of the band alignment. They show that annealing the ZrO_2 film to 600°C produces a 2 eV shift of the ZrO_2/Si band alignment, making the band-offset favorable for device applications; this was attributed to the removal of excess oxygen in the as-gown film. However, when increasing the annealing temperature further, chemical reduction of the ZrO_2 is observed, leading to the formation of $ZrSi_2$. This reaction can be limited through the use of buffer layers between the ZrO_2 and the Si substrate, such as using Si_3N_4 instead of thin SiO_2.

Another study addressing the influence of processing on band alignment was made on ternary oxides by Petry *et al*. [62, 65], with N_2 annealing up to 1000°C. Figure 8.27 shows the evolution of the bandgaps and the valence band-offsets for annealing at different temperature, and for different composition (51.8, 69.6, 77.6, and 82.6 mol% of Al_2O_3) of 5-nm-thick layers of HfAlO oxide.

For all oxide compositions, the bandgap increases after annealing. The Al_2O_3 bandgap starts to increase from 800°C, which can be attributed to structural modifications, such as the crystallization of thick Al_2O_3 (around 800°C) [66]. The value determined in this study above 800°C annealing (7.3–7.6 eV) is between the amorphous (6.7 eV) and the γ-phase (8.7 eV) bandgap value, which is interpreted as due to a partial crystallization of the layer and/or to a lower density of the layer. The change in the bandgap of HfO_2 is less dramatic, but still significant (from 5.0 to 5.35 eV) and is also attributed to crystallographic structure changes. In the mixed oxide case, an increase at 800°C is also observed. For the 1 : 1 oxide, it correlates with phase segregation. As bandgap measurements from the energy loss spectra always measure the smallest available gap, it is surprising that the value observed is larger

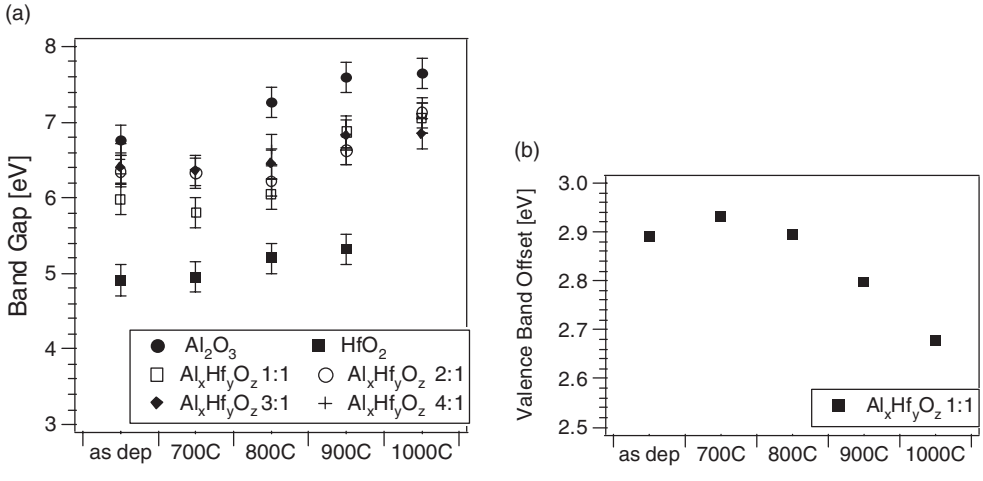

Figure 8.27 (a) Bandgap of HfAlO oxide with different composition as a function of the annealing temperature; (b) valence band offset for ALCVD HfAlO 1 : 1 as a function of the temperature [64]

than the HfO_2 value. It is is assumed that the stress generated by defects in the HfO_2 embedded in the Al_2O_3 prevent the electronic structure of these clusters matching that of the bulk HfO_2. An increase of the bandgap is also accompanied by a decrease of the valence band-offset. For AlZrO, on the contrary, no significant dependence upon annealing is seen for the bandgap or the valence band-offset.

Techniques others than photoemission can yield important information about the band structure. The bandgap, for instance, can also be determined from the onset of the rise of the absorption coefficient as obtained by ellipsometry, but requires measurement in the UV range. This is well illustrated for a number of high-*k* dielectrics ($LaAlO_3$, $GdScO_3$, $SmScO_3$, etc.) by Lim *et al*. [52]. They were able to accurately determine band gaps by combining measurements in the far UV and visible–near-UV. The optical results are usually in good agreement with photoemission results [83]. However, these measurements are inconvenient to apply to very thin films.

Another very important measurement technique is internal photoemission, that has the advantage of being applicable to metal/dielectric/silicon structures that mimic the real device structures; however, the specific set-up regarding materials and thickness used also have to be considered. Brewer *et al*. [55], determined the energy barrier in $Au/HfO_2/Si$ and $Au/Al_2O_3/Si$ structure using bias-dependent internal photoemission spectroscopy; band-offset values of 2.7 eV for HfO_2, and 3.3 eV for Al_2O_3, were determined.

Internal photoemission has also been applied to study the energy barrier between the metal Fermi level and the insulator conduction band for metallic nitride with SiO_2 an HfO_2 [67], which is not measurable with photoemission.

Unfortunately, although these techniques are very useful in looking at bandgap and band-offset, they lack the possibility for detailed study of the electronic structure. In order to identify the precise transition responsible for the electronic structure, a thorough spectroscopic study, including X-ray absorption, is necessary, as has been shown by Lucovski and co-authors [53], who studied the electronic structure of binary oxides and Hf or Zr silicates.

8.8 CRYSTALLOGRAPHY

Crystallographic information for high-*k* gate stacks as a function of processing is of prime importance. Indeed, an amorphous film is often preferred, as grain boundaries in the film could cause larger leakage or charge trapping. Among the numerous studies investigating these crystallographic aspects, two techniques largely dominate the literature data [30, 68–73]: TEM and XRD.

Next to identification of the crystalline phase, it is often important to determine the crystallization temperature, as this can influence the device integration scheme if an amorphous layer must be maintained. Figure 8.28 shows, for instance, that not only the material has to be considered, but also the precise stack must be analyzed; the layer thickness itself has an influence on the crystallization temperature.

Another important, and obvious, parameter for the crystallization temperature is the layer composition. Precise determination of the crystallization temperature as a function of composition has been carried out for HfAlO oxide [84]. In this case, the dielectric constant varies proportionally with the Hf content, and thus the largest Hf content for which an amorphous layer is preserved may be determined (see Figure 8.13).

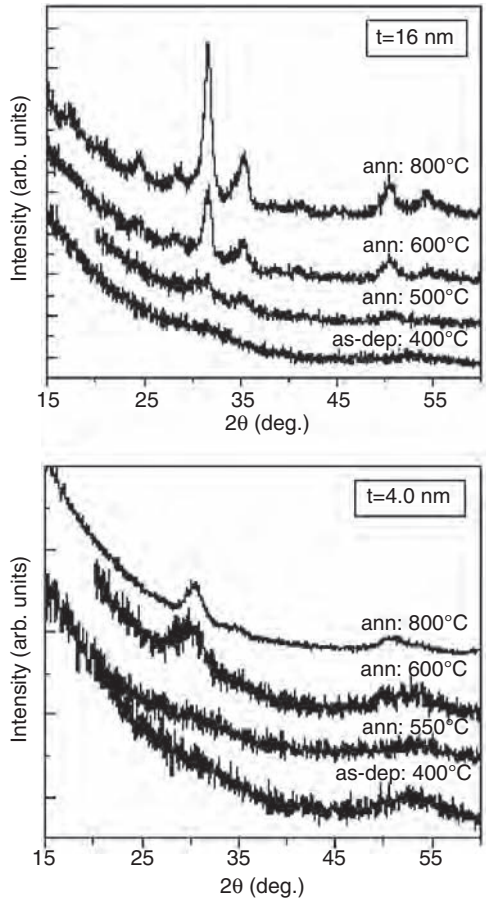

Figure 8.28 Change of XRD pattern for a 16- and 4-nm-thick MOCVD HfO_2 film after post-deposition annealing [30] (Reproduced with permission from Elsevier)

8.9 DEFECTS

Most of the knowledge about the electrical behaviour of high-*k* materials has been gained from measurement performed on macroscopic MOS capacitors or transistors using standard characterization methods at the device level. These tests, however, provide only spacially averaged information on the electrical properties of the materials, and do not address microscopic failure mechanisms. In order to understand the origins of failure/leakage, one has to microscopically investigate the defects in high-*k* layers. This is seldom done due to experimental difficulties. A few examples have been published where defects are investigated either indirectly or directly [64, 74–78].

Kaushik *et al*. [77] investigated defects in a Hf-based high-*k* material through a combined study using wet-etch defect delineation, electron microscopy, depth profiling and conventional electrical measurements. Figure 8.29 shows the results of an etch test visualized by SEM. It shows that annealing of the layers under nitrogen significantly reduces the number

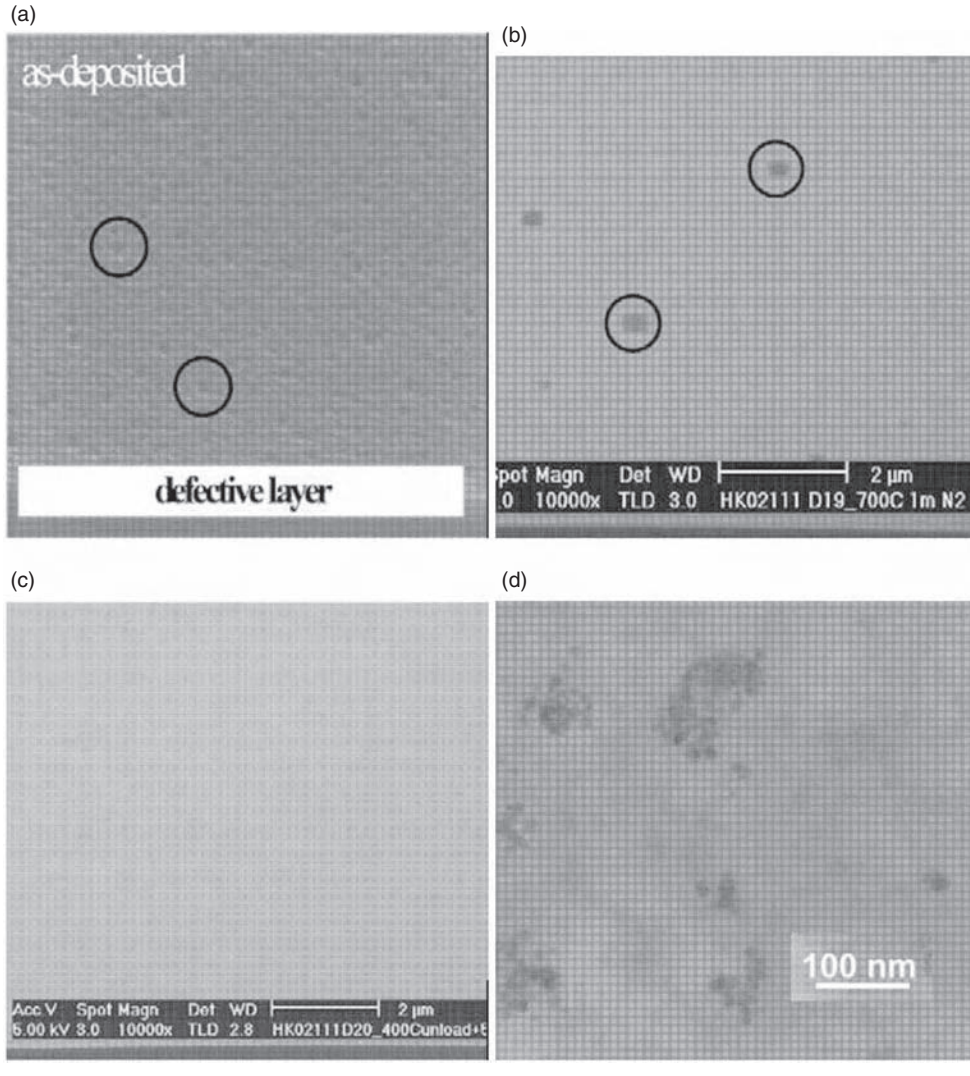

Figure 8.29 SEM images from HfO_2 layer grown on chemical oxide: (a) as deposited; (b) N_2 annealed; (c) O_2 annealed; (d) and plan-view TEM image of as deposited HfO_2 layer deposited on RTO surface [77] (Reproduced with permission from Elsevier)

of observable defects, and that oxygen annealing leads to a (SEM-observed) defect-free film. A good correlation was obtained between the presence of the defect and the failure of the layers. However, additional defects are present that lead to large leakage current, and are not visible on etched layers.

In order to understand the origin of these defects, a microscopic electrical characterization of the layers is necessary.

One of the techniques used for this study is CPD (contact potential difference) an AFM-based system [79, 80, 81], where correlations between topographical images and electrical

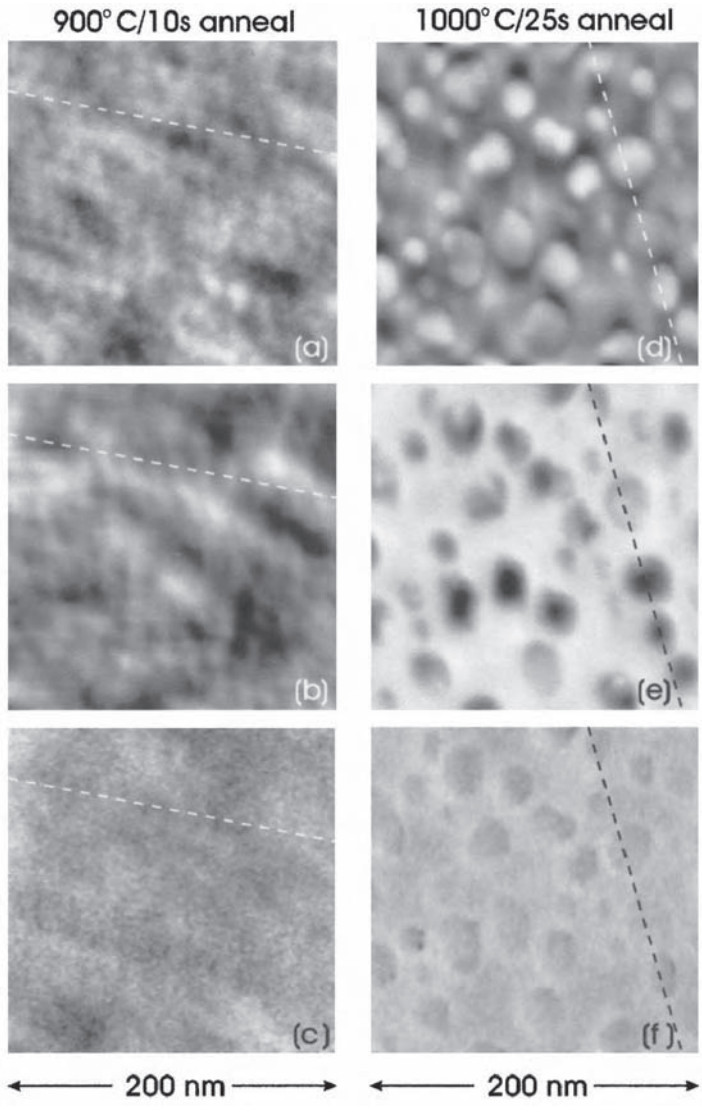

Figure 8.30 200 nm^2 topography (a, d), CPD (b, e) and differential capacitance (c, f) images for 2.2 nm $Hf_{0.78}Si_{0.22}O_2$ layer annealed for 10 s at 900°C (a–c) and for 25 s at 1000°C (d–f). Full-scale, black–white image contrast: (a) 0.624 nm, (0.077 nm rms roughness); (b) 0.21 V; (c) 9.1 nm (0.58 nm rms roughness); (d) 0.50 V [79] (Reproduced with permission from the American Institute of Physics)

images are investigated. A detailed analysis of the effect of annealing of HfO_2 and Hf silicates has been performed by this technique [79, 80]. Figure 8.30 shows an image obtained on a $Hf_{0.78}Si_{0.22}O_2$ sample after 900 and 1000°C annealing. Low roughness was measured for the as-grown and annealed films, and small fluctuations of the surface potential were observed, that did not change significantly upon annealing. However, correlation between the topographic and CPD images for the as-grown sample changed dramatically after

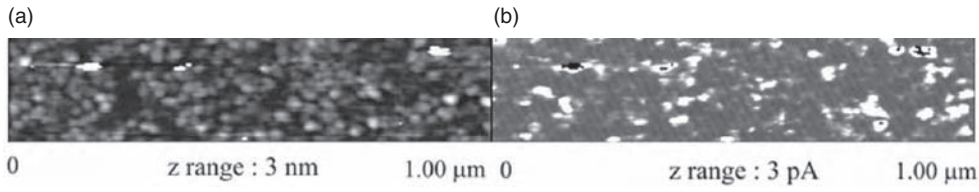

Figure 8.31 (a) Topographical; (b) current map of a 5.6 nm HfO_2 ALCVD layer deposited on a 0.4 nm chemical SiO_2 layer, annealed at 800°C under N_2. (Reprinted with permission from J. Petry, PhD thesis, Katholieke Universiteit Leuven, ISBN 90-5682-586-0)

crystallization, where the higher CPD value was associated with grain boundaries. However, detailed interpretation remains elusive.

Another microscopic technique that can be used to retrieve local electrical information is the C-AFM (conducting AFM) or TUNA [76, 78, 64]. In this technique, both a topographical and a current image can be obtained. Figure 8.31 shows the topographical and current maps of a HfO_2/SiO_2 stack annealed under nitrogen. Obviously, high leakage is observed on some spots, but these cannot be correlated to the grain boundaries. As most of the leakage current passes through these weak spots, it is important to understand their origin in order to improve the leakage characteristics of the actual devices. The origin of these weak spots could be grain boundaries, local decreases in thickness, local change in k values, local change in structure, the presence of charges, etc. A detailed study involving TEM and TOF-SIMS profiling, of an Al_2O_3 layer showed that the most likely source of the increased leakage in the weak spots was thinning of the interfacial layer. Besides current maps, C-AFM can also be used to retrieve local I–V characteristics and to perform some reliability measurements. On the above-mentioned stacks, shifts in the I–V curves show the creation of positive charges or the existence of a trap-assisted conduction mechanism.

8.10 CONCLUSION

We have shown that a large range of physical characterization techniques allows one to achieve precise characterization of ultra-thin high-k oxide stacks, including thickness, composition, defects and crystallography. However, for each of the characteristics to be analyzed, a multi-technique approach is preferable in order to obtain a reliable characterisation of the stack.

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9 Electrical Characterization of Advanced Gate Dielectrics

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9.1 INTRODUCTION

The key issue for the success of MOS-based technologies has always been the control of the interface between the silicon and the gate dielectric. From the very beginning of the MOS scaling era, SiO_2 has been the gate dielectric of choice because of its almost unique combination of properties that are beneficial for good MOSFET operation. Indeed, SiO_2 is the natural oxide of silicon, it can easily be grown thermally on a silicon wafer, it shows

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very reproducible growth with low defect density and uniform thickness, and contains minimal charges and traps. It forms also a good diffusion barrier against many common impurities, and shows no leakage currents under operating voltage (at least down to a certain thickness, see further), has a large breakdown field (>12 MV/cm) and long time-to-breakdown.

SiO_2 is a noncrystalline (amorphous) insulator with a very high energy bandgap of about 9 eV. It is thermally very stable and therefore insensitive to subsequent processing steps, which makes it highly suitable for process integration. But probably the main reason for the success of SiO_2 as gate dielectric in silicon-based technologies is because it forms a very high quality interface with the silicon surface, especially after annealing in H-containing ambients. The hydrogen passivates the silicon dangling bonds, and as a result the number of interface states can be reduced to very low densities, of the order of only $10^{10}/cm^2$, which is an absolute prerequisite for good MOSFET operation. All of these properties made SiO_2 into the most studied dielectric material, with a learning curve of more than 40 years now, and actually there is at this moment no clear candidate to replace it, although a lot of research is going on in this field.

But by the very aggresive scaling of the past 30–40 years, SiO_2 is now reaching its physical scaling limits. Figure 9.1 shows the evolution of channel length and SiO_2 thickness over the past 35 years. In today's technologies, effective oxide thicknesses of 1–1.5 nm are being used. As a result, gate leakage currents have been steadily increasing, certainly when the oxide thicknes crossed the boundary where direct tunneling becomes dominant over Fowler–Nordheim tunneling (below 4 nm). Figure 9.2 shows the evolution of gate leakage currents through SiO_2 dielectrics in the direct tunneling regime. It can be concluded that in this thickness range the leakage increases by one decade per 0.2 nm oxide thickness reduction! This gate leakage current is dominating the transistor off leakage currents today, which leads to strongly increasing standby power dissipation of the CMOS circuits compared to older CMOS process generations.

The increase in gate leakage current does not only affect the circuit operation. It also has a strong influence on the electrical characterization of the gate dielectrics. Nearly every electrical characterization methodology, developed in the past, has to be revised in order to take into account the increased leakage currents and scaled down oxide thickness. The measurement of a simple *C–V* characteristic for example, which is the standard technique

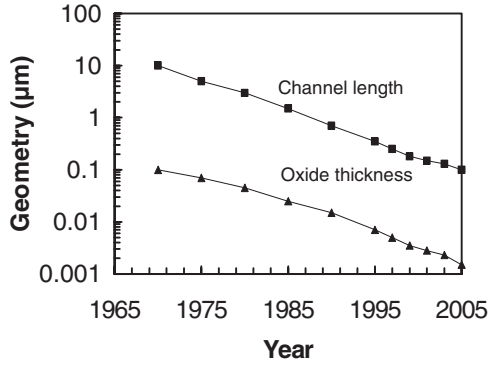


Figure 9.1 Evolution of channel length and oxide thickness as a function of time. Today effective oxide thickness of 1.5 nm have been reached

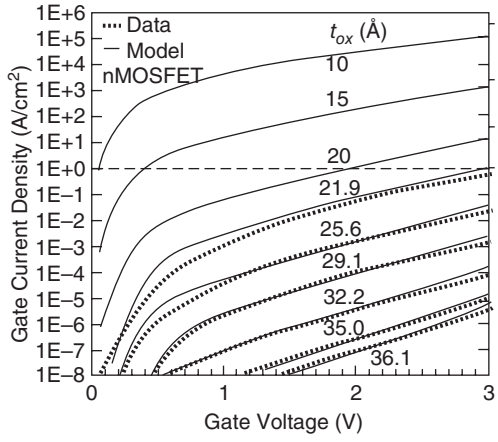


Figure 9.2 Impact of oxide thickness scaling on gate leakage currents [1] (Reproduced by permission of IEEE)

of every MOS electrical characterization methodology, has become much more complicated under influence of increasing capacitance density, increasing leakage currents, poly-depletion effects, and quantum effects in the inversion layer. As a result, the methodology cannot be applied any longer like before and needs to be adapted.

Moreover, in order to cope with the increasing standby power consumption, the search for a replacement of SiO_2 as the gate dielectric is at this moment in full progress. A new gate dielectric with a higher dielectric constant is urgently needed, where the physical thickness can be chosen higher to reach the same (or larger) capacitance per unit area, thereby reducing the gate leakage currents. Although some of the electrical properties of these high-k gate dielectrics are very similar to the case of SiO_2 dielectrics, some of them are quite different. One of the major differences is the presence of a thin interfacial layer (usually SiO_2 or a silicate). This leads to a number of new electrical phenomena and again requires adaptations to the electrical characterization methodology.

The purpose of this chapter is to give a broad overview of the implications of aggressive SiO_2 scaling and of the introduction of high-k gate materials on the electrical characterization of modern gate dielectrics. In the first part of the chapter, the impact of scaling of SiO_2-based gate dielectrics on the electrical characterization is discussed, covering the mechanisms of gate leakage currents, the measurement of C–V and of charge pumping characteristics under high gate leakage currents, noise measurement and models for scaled oxide thicknesses, and finally reliability measurements such as time-dependent dielectric breakdown (TDDB) and negative-bias-temperature instability (NBTI). It is important to mention that in the chapter it is assumed that the basics of the techniques are already known to the reader. These basics can be found in other textbooks, such as [2]. In this chapter the focus is on the changes when scaling down the oxide thickness.

In the second part, the electrical characterization of high-k dielectrics is discussed, covering the definition of effective oxide thickness (EOT) and capacitive effective thickness (CET), the extraction and importance of gate workfunction, the impact of defects in the high-k dielectrics on the V_t- instability of the MOSFET's and techniques to measure these defects under dynamic conditions, and again noise, TDDB and NBT characterization and models for high-k gate dielectrics.

9.2 IMPACT OF SCALING OF SiO_2-BASED GATE DIELECTRICS

9.2.1 Gate leakage current

Fowler–Nordheim and direct tunneling

In deep-submicrometer MOS transistors, the current flowing through the gate dielectric under normal operating conditions is considerable. This is caused by the combination of high electric field (~6 MV/cm) and low dielectric thickness (<4 nm). Under these circumstances, a significant quantum mechanical tunneling current is observed, even through a perfect dielectric.

The basic principle of tunneling is sketched in the band diagram of Figure 9.3. The potential barrier[1] for electrons between the gate and the gate dielectric has a height Φ_b around 3 eV, which at room temperature is so much higher than kT/q (25 meV) that electrons are not able to jump into the conduction band of the dielectric. (It is customary, although not strictly correct, to represent amorphous SiO_2 in band diagrams as a semiconductor with a large bandgap around 9 eV.) However, a potential barrier with finite width and finite barrier height can be passed by quantum mechanical tunneling.

Electrons can tunnel from gate to substrate when a negative gate bias is applied. Fowler and Nordheim derived an approximate expression for the current density through a triangular potential barrier in 1928 [3], which was later reformulated as [4]:

$$J_{FN} = AE_{OX}^2 e^{-B/E_{ox}} \tag{1}$$

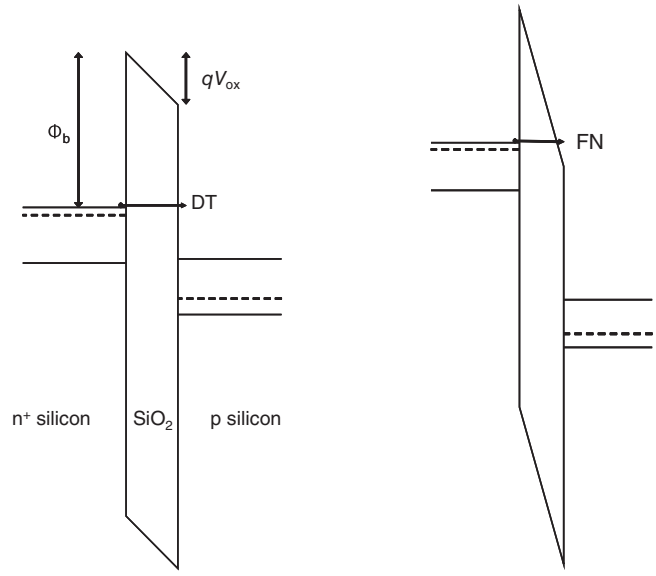


Figure 9.3 Energy band diagrams of an n^+ poly-Si/SiO2/p-Si structure under negative gate bias, illustrating direct tunneling (left) and Fowler–Nordheim tunneling (right) of electrons from the poly-Si gate electrode into the substrate

where

$$A = \frac{q^3}{16\pi^2 \hbar \Phi_b} \frac{m_e}{m^*} \qquad B = \frac{4\sqrt{2m^*}\Phi_b^{3/2}}{3q\hbar} \tag{2}$$

In these equations, E_{ox} is the electric field across the dielectric ($E_{ox} = V_{ox}/t_{ox}$), q the elementary charge, $\hbar$ the reduced Planck constant, m_e the electron rest mass, m^* the effective mass of electrons in the dielectric, and Φ_b the barrier height at the conductor/dielectric interface. One normally assumes $m^* \simeq 0.3$–$0.5\,m_e$ inside SiO_2, and $\Phi_b = 3.1$ eV between the conduction bands of Si and SiO_2. This equation qualitatively describes the conduction behavior of an SiO_2 layer at high field [5]. The potential barrier is however not perfectly trapezoidal. The barrier top is rounded off slightly [3], and fixed charge inside the dielectric affects the field.

The lack of precise knowledge of the material properties also makes it difficult to accurately predict the tunnel current. For instance, both Φ_b and m^* are not known with sufficient precision, and it is practically impossible to establish the depth of fixed charges in the dielectric. Finally, when measurement data are compared with tunnel equations, the determination of V_{ox} in the measurements is not straightforward (see, e.g., [6]).

At low fields, the potential barrier shape becomes trapezoidal (Figure 9.3, left) and the Fowler–Nordheim equation loses validity. Electrons will not tunnel into the conduction band of the dielectric, but directly into the substrate, hence the term *direct tunneling*. The mathematical complexity of direct tunneling prohibits the derivation of a simple expression such as Equation (1), and several approximations are used in practice. One commonly used approximation yields [2]

$$J_{DT} = A' E_{OX}^2 e^{-B'/E_{ox}} \tag{3}$$

with

$$A' = A\left(1 - \sqrt{\frac{\Phi_b - qV_{OX}}{\Phi_b}}\right)^{-2} \qquad B' = b\left[1 - \left(\frac{\Phi_b - qV_{OX}}{\Phi_b}\right)^{3/2}\right] \tag{4}$$

This formulation shows that direct tunneling and Fowler–Nordheim tunneling have a similar dependence on oxide electric field; however, A and B now are corrected with a weak dependence on V_{ox}. Direct tunneling is only significant in ultra-thin dielectric films (below 4 nm for SiO_2). The assumptions made for the derivation of Equation (3) do not hold too well. Therefore this equation has only limited value in predicting the direct tunnel current flowing in a MOS transistor, especially at low gate voltage, as discussed, e.g., in [6]. For an overview of direct tunneling equations, see [7] and references therein.

This discussion has focused on electrons tunneling from gate to substrate in an NMOS structure. Similar conduction mechanisms exist in PMOS; where hole tunneling from a p-type gate can occur under positive gate bias. Under particular circumstances, electron tunneling can also be observed from interface states or even the valence band; but normally the tunneling from the conduction band dominates. Hole tunneling is highly improbable compared with electron tunneling, due to the much higher potential barrier at the valence band. It is only significant in deep-submicrometer PMOS devices in inversion [8].

Gate leakage through MOS stack imperfections

Any real-life dielectric will contain imperfections leading to additional leakage currents. When a dielectric has been exposed to stress, for instance high-field stress or radiation, it exhibits a higher than normal leakage current. The excess leakage currents are classified according to their conduction behavior:

- Stress-induced leakage current, or SILC: stress causes chemical bonds in the dielectric to break, leading to traps in the bandgap. An additional tunnel current can then flow in the dielectric through an inelastic trap-assisted tunneling process [9–12]. SILC appears as low-field conduction and gradually becomes stronger with longer stress times.
- Soft breakdown: a sudden event where a weakly conductive path is formed between the gate electrode and the substrate. The conduction is noisy.
- Progressive breakdown: an event similar to soft breakdown, but with a conductive path that gradually becomes more conductive when further stressed.
- Hard breakdown: a catastrophic sudden event leading to a low-resistive conductive path between gate and substrate, normally causing device failure.

The three breakdown modes are discussed in Section 9.2.5. Besides the phenomena related to SiO_2 bulk imperfections, contributions to the tunneling current from interface states are also reported [13], [14].

Figure 9.4 shows the progressive stages of a dielectric under stress, becoming more and more conductive.

In a MOS transistor, the gate current flows into source, channel region and drain. The source and drain regions having a different doping level than the channel, the current through the dielectric is not always homogeneous. Whether a current flows towards the bulk

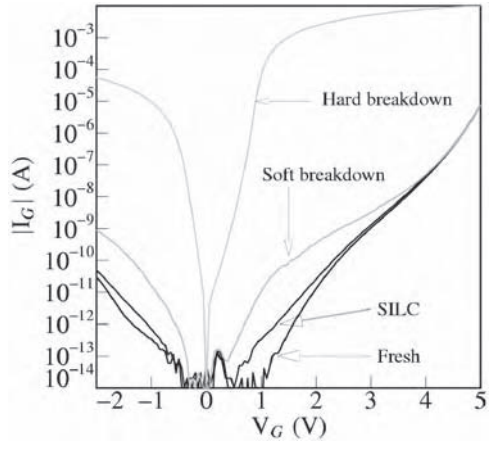


Figure 9.4 Gate leakage through a 4.0 nm SiO_2 gate dielectric, measured before stress ('fresh'), and after application of an excessive gate voltage for several minutes, showing SILC, soft breakdown and hard breakdown, consecutively

(well) contact further depends on the type of tunneling carrier and the applied bias. Overall, the distribution of the gate current over the three other MOS terminal nodes, source, drain and bulk, is therefore not straightforward. By precise modeling the distribution of the gate current flow over the various terminals can be explained, see, e.g., [15–17].

9.2.2 *C–V* measurements and interpretation

To extract the main MOS characteristics, the *C–V* measurement is one of the most commonly applied techniques. This measurement allows extracting gate dielectric thickness, flatband voltage, threshold voltage, substrate impurity profile, gate depletion and interface trap density. The classical *C–V* measurement approach, with the subsequent extraction of parameters, is described in [2]. However, with ongoing downscaling of the dielectric, the tunnel current through the dielectric becomes large, and the shape of the *C–V* curve changes. This calls for a modified measurement approach and analysis, as discussed in the following sections.

The reader is assumed to be familiar with traditional *C–V* measurements and their interpretation, as treated, e.g., in [18, 2]. In this section, it is first discussed how a good *C–V* measurement can be carried out on a leaky dielectric. This requires the right instrumentation, test structures, and analysis. Then, the features of a *C–V* curve of a deep-submicrometer MOS structure are discussed, and parameter extraction approaches are presented.

C–V measurement techniques

Two generic types of *C–V* measurements exist: the quasi-static and the high-frequency measurement. Both measurements quantify the *differential* capacitance, $C = \partial Q/\partial V$. In a quasi-static measurement, this is done with a slow, linear ramp of the voltage on the gate ($\mathrm{d}V/\mathrm{d}t$ = constant, typically 0.05 V/s). The current is measured, and capacitance is computed from $I_{QS}(V) = C(V)\ \mathrm{d}V/\mathrm{d}t$. ($I_{QS}$ is called the *displacement current*.) When gate leakage is present, the measured current will be $I_{QS} + I_G$, and $I_G >> I_{QS}$ for dielectrics thinner than 2–3 nm. Since both currents scale with the capacitor area, this technique thus becomes intrinsically inaccurate for thin dielectrics. Some leakage current correction can still be done (see, e.g., [19, 20]), but in practice quasi-static *C–V* measurements are difficult to be carried out on SiO_2 dielectrics below 3.5 nm.

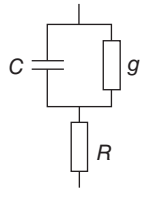
For deep-submicrometer MOS devices, the high-frequency *C–V* measurement is preferred. It is carried out using a capacitance meter or an LCR impedance meter. For this measurement, the instrument applies a DC bias to the device, and a small sinusoidal voltage signal is added with a typical amplitude of 10–50 mV. The system measures the AC current amplitude at the same frequency, as well as the phase shift between the voltage and current signals. Normally, the capacitor or transistor used for this measurement is connected as a two-terminal device, with the gate connected to the 'low' terminal and the substrate connected to the 'high' terminal of the measurement instrument (for stray signals reduction) [21]. A transistor (or so-called gated diode) is preferred over a capacitor, because the source and drain act as minority-carrier supplies, so that the inversion layer can build up fast enough to appear in the *C–V* curve. The source and drain terminals can be connected with the substrate.

Ideally, the phase difference measured between the applied ac voltage and the current is 90°; and the measured impedance relates to the capacitance as $|Z| = (\omega C)^{-1}$. In practice, the phase difference always deviates from 90°, and here, the art of C–V measurement starts [22]. Many guidelines have been formulated for distilling the proper capacitance value from a high-frequency C–V measurement, and a lot of research in this field is still going on at this moment [23]. In this section, one approach is presented, but the reader is referred to recent literature for other possible approaches, since the problem is not completely solved at this moment.

A wafer-level C–V measurement is conveniently carried out using two probe needles with top-side contacts for the test structure (a capacitor or a transistor). A good C–V measurement starts with the calibration of the measurement set-up. When the two probes are contacted to the same bond pad, the system ideally should measure zero impedance. Similarly, the impedance should be infinite when the probes are disconnected from the device. However, the inductance and capacitance of the cables, and the contact resistance cannot be neglected. By measuring the impedance in the short-circuited ('short') and disconnected ('open') states at various frequencies, these parasitic components can be quantified. Most measurement instruments allow for an automatic correction of cable parasitics, as is usually explained in their operating manuals.

The on-wafer test structure itself can also contain parasitic components. In classical high-frequency C–V tests, very large capacitors were used (>10 000 μm^2) in a square or round design. The parasitic components at the device edges can then readily be ignored. However, when leaky dielectrics are tested, large-area capacitors are inadequate. This can be understood from the following argumentation. A MOS capacitor (or transistor) connected as a two-terminal device can roughly be described by the three-component equivalent circuit shown in Figure 9.5, where C symbolizes the gate-semiconductor capacitance, g the conductance of the dielectric ($g = dI/dV$) and R the series resistance of the structure. The figure also gives equations for the impedance Z, the quality factor Q and the frequency f_{opt} where the quality factor reaches its maximum value Q_{opt}. High quality factor (above unity) allows using a simple equivalent circuit and an easy capacitance determination.

The admittance of the gate dielectric, $j\omega C + g$, tends to become more resistive when the gate leakage current increases. This makes an accurate measurement of C more difficult. Because C and g both scale with the capacitor area, only an increased measurement frequency (or ω) helps [24, 25]. For dielectrics with a direct tunneling leakage current density larger than 100 A/cm^2, a measurement frequency higher than 10 MHz is required to obtain



$$Z = \frac{1}{j\omega C + g} + R \tag{5}$$

$$Q \equiv -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega C}{g + R(\omega^2 C^2 + g^2)} \tag{6}$$

$$f_{opt} = \frac{1}{2\pi RC}\sqrt{gR(1 + gR)} \tag{7}$$

$$Q_{opt} = \frac{1}{2\sqrt{gR(1 + gR)}} \tag{8}$$

Figure 9.5 Three-element equivalent circuit approximation of a leaky MOS capacitor, with equations for its impedance Z, the related quality factor $Q(\omega)$, and the maximum achievable quality factor Q_{opt}, found at frequency f_{opt} [24] (Reproduced by permission of IEEE)

a quality factor well above unity. In turn, a higher frequency calls for the use of a smaller area capacitor, for two reasons: the first is that at higher frequencies, non-quasi-static effects will influence the response of a large device, as quantified, e.g., in [26]. Secondly, the external resistance R becomes more important when the measurement frequency increases. In accumulation, this resistance is dominated by the well resistance, which roughly decreases with the square root of the capacitor area [27]. In inversion, R is dominated by channel resistance and is, to first order, independent of area. Therefore, using Equation (6) in Figure 9.5, it is found that Q improves with decreasing area in both accumulation and inversion (especially above f_{opt}).

The external resistance R of the three-element equivalent circuit is composed of contributions from the gate resistance, the channel and source/drain resistance in inversion, and the well resistance in accumulation. The gate, channel and well resistance have a distributed nature and only when the test structure is properly designed, the three-element approximation holds well. For instance, when the channel length is $>>1\,\mu m$, a distributed network description is more accurate [28, 29], but not very practical. A good test structure allows for the application of a simple equivalent circuit and a simple capacitance extraction with few fit parameters. One approach that is gaining ground is to lay out multi-finger capacitors with a basic topography as sketched in Figure 9.6 (a) [30, 31]. To obtain a significant overall gate capacitance, several of these structures can be drawn in parallel.

One such structure does not suffice: 'open' and 'short' reference structures should be added, and moreover, several structures should be laid out with varying gate finger length and width. This allows extraction of the capacitance per unit area in a reliable way (minimizing the impact of gate edge contributions).

The presented measurement approach with two top-side contacts has the benefit of being simple to carry out and analyze; and that the influence of the wafer chuck is minimized. Including the chuck in the measurement patch can cause various problems, as reported, e.g., in [32, 33].

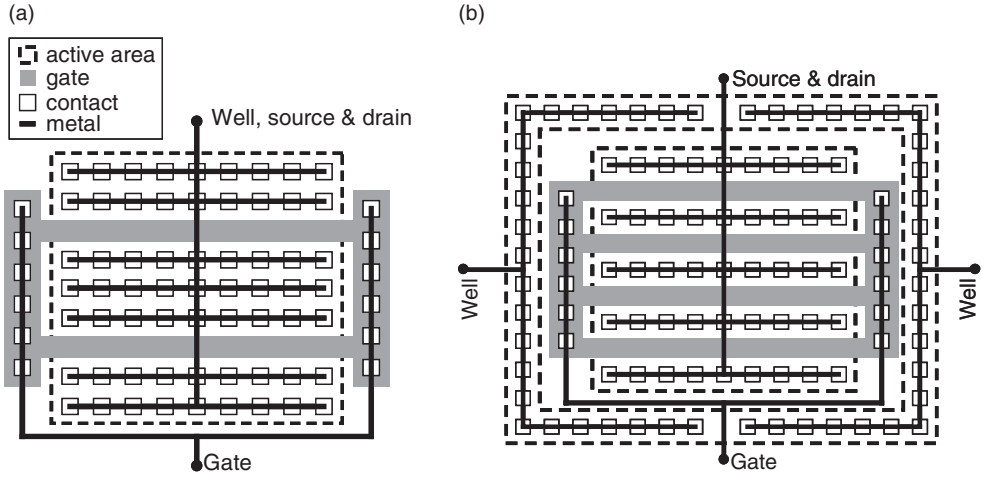


Figure 9.6 (a) Top view of the (conceptual) layout of multi-finger capacitors, suitable for high frequency C–V measurements. Left: two-terminal approach; the well contacts run in between the source/drain regions around each gate finger; (b) three-terminal layout where the well contact is separated from the source/drain contact

A drawback of the two-terminal structure is that the split-*C–V* technique [34] and charge pumping techniques cannot be applied; and that no back-bias can be administered (which is useful for channel impurity profiling). To this purpose, the well contact should be separate from the source/drain contact, as depicted in Figure 9.6 (b).

The *C–V* curve for devices with an ultra-thin dielectric

From a correctly obtained high-frequency *C–V* curve, several MOS parameters can be extracted: dielectric thickness, threshold and flatband voltage, channel doping concentration, and gate doping concentration. In Figure 9.7 it is illustrated how variations of some parameters affect the shape of the *C–V* curve. It is clear from this figure how the three parameters each impact the curve shape, and with a good fitting procedure, the parameters can be extracted from a measured curve.

Handbooks on *C–V* measurement and interpretation generally do not describe the peculiar features seen with an ultra-thin dielectric. These features do affect the *C–V* curve strongly and should be taken into account to extract accurate parameter values. The charge accumulated at each side of the gate dielectric is not concentrated in an infinitesimally narrow sheet at the dielectric edge, as normally assumed. Both in the gate and in the substrate, charge is not precisely localized at the interface. Instead, in silicon electrodes the charge *centroid* is positioned about a nanometer away from the Si–SiO_2 interface. This effect is seen as 0.2–0.3 nm in the equivalent oxide thickness, due to the higher permittivity of silicon compared with SiO_2. Moreover, this position depends on the applied electric field. Therefore, contrary to the thick-oxide situation described in most textbooks, the accumulation capacitance does not saturate to a certain constant value [40]. Instead, as seen in Figure 9.7, the capacitance keeps increasing with increasing accumulation voltage, until the point of dielectric breakdown. This effect must be considered both in the gate and in the substrate.

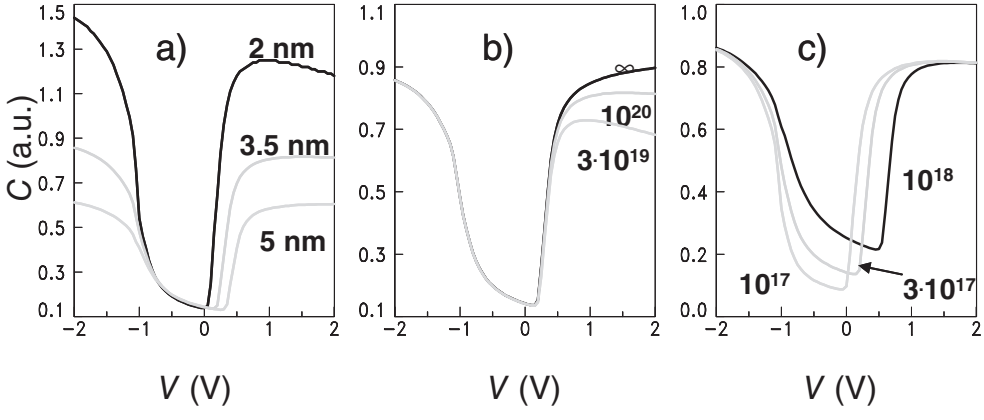


Figure 9.7 *C–V* curves as described with MOS Model 11, for *n*-type transistors in a standard 0.18 µm technology. In the figures, three parameters are varied: (a) the gate dielectric thickness; (b) the gate doping concentration (displayed in cm^{-3}); (c) the channel impurity concentration (in cm^{-3}). The curves were kindly provided by R. van Langevelde

Therefore it is impossible to speak of *the* accumulation capacitance and to compute t_{ox} from that value. More accurate methods exist even for thick dielectrics, see, e.g., [35].

In inversion, the quantization of the energy levels in the channel also becomes significant. Pals [36] and van Dort *et al.* [37] showed how quantization effects influence the onset of inversion, and the value of the threshold voltage. Again, the charge centroid will be positioned away from the interface. In CMOS technologies with implanted poly-Si gates, the gate electrode usually depletes in inversion [38, 39]. The inversion capacitance decreases with higher inversion bias through this effect (see Figure 9.7b).

The *C–V* curve of a deep-submicrometer MOS transistor is therefore not well described with the traditional equations. An analytic equation describing $C(V)$ does not exist [40]; the Poisson and Schrödinger equations have to be solved numerically to determine the *C–V* curve from theory. Several implementations are available, but do yield divergent results [41]. By optimizing the model parameters, such a Poisson–Schrödinger solver can find a *C–V* curve that overlaps with a measurement result. This so-called inverse modeling approach is accurate but far from convenient. A fitting procedure with a compact model description is more attractive to the process engineer. The open-source Hauser program [42] provides just that, and is presently the most widely used tool.

9.2.3 Charge pumping

Principle of the charge pumping technique

Whereas *C–V* measurements are the standard workhorse for the dielectric characterization at the capacitor level, it cannot be applied to very small area transistor devices. However, a good alternative technique suitable for small area devices is known to be the charge pumping technique.

The basic experimental set-up to perform charge pumping measurements, as introduced by Brugler and Jespers [43] is illustrated in Figure 9.8 for the case of an *n*-channel MOS

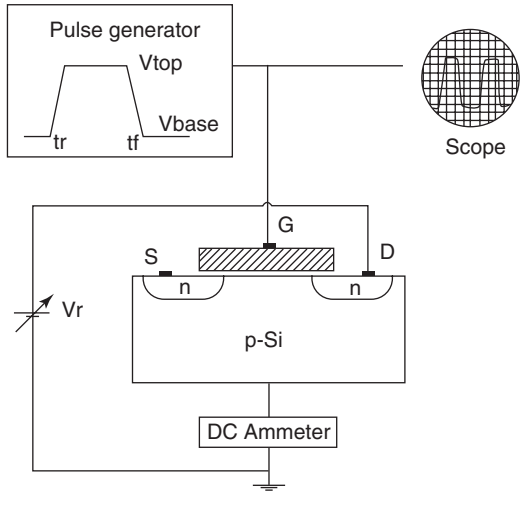


Figure 9.8 Basic set-up for charge pumping measurements [52] (Reproduced by permission of IEEE)

transistor. The gate of the MOSFET is connected to a pulse generator, a reverse bias is applied to the source and the drain diodes, while the substrate current is measured. When the gate is pulsed between inversion and accumulation conditions (from above the threshold voltage to below the flatband voltage), a charge pumping current can be measured at the substrate, which flows in the opposite direction of the normal drain and source to substrate leakage currents.

When the *n*-MOS transistor is pulsed into inversion, electrons will flow from the source and drain regions into the channel, where a fraction of them will be captured by the interface traps. When the gate pulse is driving the surface back into accumulation, the mobile electrons drift back to the source and drain, but the charges that are trapped at the interface traps will recombine with the majority-carriers coming from the substrate. This gives rise to a net flow of negative charge into the substrate, given by

$$Q_{\mathrm{cp}} = qA_{\mathrm{G}} \int_{E_{\mathrm{F,acc}}}^{E_{\mathrm{F,inv}}} D_{\mathrm{it}}(E)\mathrm{d}E \tag{9}$$

where q is the electron charge, A_{G} is the channel area of the transistor (cm^{-2}), $D_{\mathrm{it}}(E)$ is the interface trap density at energy level E ($\mathrm{cm}^{-2}\mathrm{eV}^{-1}$) and $E_{\mathrm{F,inv}}$ and $E_{\mathrm{F,acc}}$ are the Fermi level in inversion and accumulation, respectively. When applying repetitive pulses with frequency f, this charge Q_{cp} will give rise to a net DC current in the substrate, which can be written as:

$$I_{\mathrm{cp}} = fQ_{\mathrm{cp}} = fqA_{\mathrm{G}}\overline{D_{\mathrm{it}}}\Delta E \tag{10}$$

where $\overline{D_{\mathrm{it}}}$ is the mean interface trap density over the energy range $\Delta E = E_{\mathrm{F,inv}} - E_{\mathrm{F,acc}}$.

In this simple first-order theory, Brugler and Jespers assumed tacitly that the carriers that are trapped in the interface traps during the first half of the pulse period, remain trapped until they recombine with the opposite type of carriers during the second half of the pulse period. As a result, all interface traps between the Fermi levels in inversion and accumulation are participating to the charge pumping process. This is only true, however, for zero transition times between inversion and accumulation. In practice this switching between inversion and accumulation requires a finite time. During this time, part of the carriers trapped in the interface states can be released from the traps by thermal emission, and become free carriers which are also swept out of the channel. Only these traps that are not able to emit electrons to the conduction band during the falling gate pulse edge and holes to the valence band during the rising gate pulse edge, contribute to the charge pumping current. Both the capture of the carriers from the silicon bands into the traps and the thermal emission of the carriers from the traps towards the silicon bands are described by the so-called Shockley–Read–Hall (SRH) generation/recombination theory [44, 45].

Based on the SRH theory and the analysis of Simmons and Wei [46], it can be shown that the energy region that contributes to the CP-current is given by [47, 48]:

$$\Delta E = 2kT \ln\left(v_{\mathrm{th}} n_{\mathrm{i}} \sqrt{\sigma_p \sigma_n}\, \frac{|V_{\mathrm{FB}} - V_{\mathrm{T}}|}{\Delta V_{\mathrm{A}}} \sqrt{t_{\mathrm{f}} t_{\mathrm{r}}} \right) \tag{11}$$

with k the Boltzmann constant, T the temperature, v_{th} the thermal velocity of the carriers, n_{i} the intrinsic carrier concentration, σ_n and σ_p the capture cross-section of the traps for

electrons and holes, respectively, V_{FB} and V_T the flatband and threshold voltage of the MOSFET, ΔV_A the amplitude and t_f and t_r the fall and rise times, respectively, of the gate pulse. ΔE, as given by Equation (11) yields, in conjunction with Equation (10), a more correct expression for the CP-current equation. This expression has allowed to describe the CP-current for conditions when the pulse is switching the surface completely from strong accumulation to strong inversion, and when the fall and rise times are not too small. This was confirmed by numerical simulations of the CP-current in the time domain [49–51].

Heremans *et al.* [52] showed that by applying constant amplitude pulses with varying base levels, information can be obtained on the charge state of the interface. This is illustrated on Figure 9.9, which shows five regions of operation. By plotting the CP-current as a function of the base level voltage of the pulse (referred to as base level curve), a hat-shaped characteristic is obtained, where the rising edge of the curve occurs at V_T-ΔV_A, the falling edge at V_{FB}, and the saturation level is the CP-current as given by Equations (10) and (11). Any change of the edges is therefore indicative for trapped charges in the oxide, whereas the change of the maximum CP-current is a measure for the interface trap generation. It was also demonstrated that the rising and falling edges of the base-level curve contain information on the interface characteristics at the source and drain and at the field edges of the transistor [52]. This feature has been used to perform lateral profiling of the interface traps after degradation.

The use of base-level curves has allowed to investigate the degradation of the interface under various kinds of oxide stress, such as Fowler–Nordheim tunnel injection, substrate hot electron and hot hole injection and ionizing radiation. An example is shown in Figure 9.10, which shows the degradation of the CP-curves for a MOSFET that is stressed by uniform Fowler–Nordheim tunneling [52]. As can be observed, during the F-N–injection, the interface trap density is increasing, which is accompanied initially by a shift of the curves to lower base level voltages, followed later by a shift to higher voltages.

This integral version of the charge pumping technique has a sensitivity as low as $10^8\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, which is better than any other existing interface trap characterisation technique. It has even been demonstrated that CP can measure single interface traps in deep

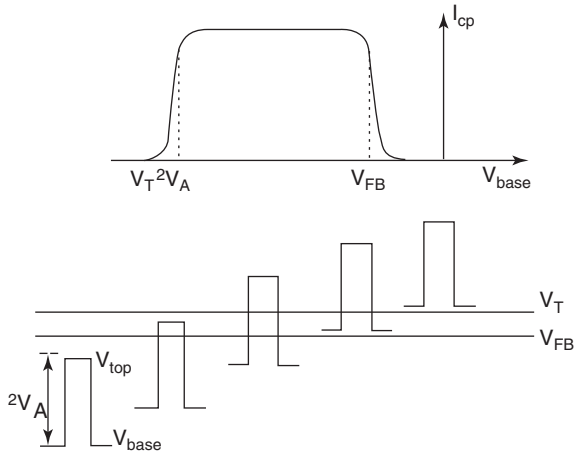


Figure 9.9 Principle of the base-level charge pumping technique [52] (Reproduced by permission of IEEE)

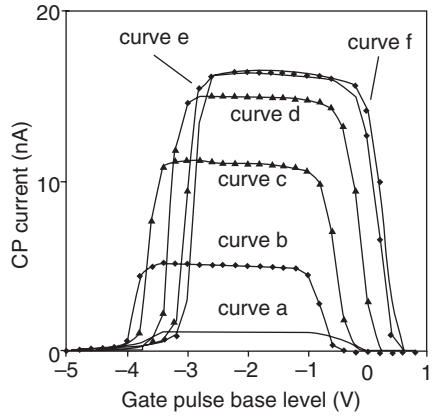


Figure 9.10 Degradation of CP-curves of a MOSFET stressed by Fowler–Nordheim tunneling [52] (Reproduced by permission of IEEE)

submicrometer transistors [53, 54]. This high sensitivity is primarily due to the fact that, in case of very low trap densities, one can increase the frequency in order to get a larger charge pumping signal, and thus a higher sensitivity. Besides for the study of MOSFET degradation, charge pumping has also been applied for energy profiling of interface state, for spatial profiling in case of nonuniform degradation and for SOI and DMOS devices. For more details on the basic principles and applications of the charge pumping technique we refer to [62] and [55] and the references therein.

Influence of gate leakage

Due to the scaling of the oxide thickness the increased gate leakage currents are interfering with the CP-measurement. Indeed, if tunneling occurs during the measurement the resulting CP-current measured at the substrate is the sum of the interface trap component and the gate leakage current due to direct tunneling of carriers through the gate oxide. As in the case of *C–V* measurements, also here the presence of this leakage current leads to important errors in the extracted interface trap parameters when its magnitude is in the same range than the CP-current. This effect was first reported by Masson and Autran [56] who also proposed two methods to correct experimental data from this parasitic leakage mechanism based on the exploitation of the static gate leakage current and low frequency CP measurements.

Figure 9.11 (a) shows the charge pumping characteristics measured at various frequencies for a NMOSFET with 1.8 nm gate oxide [56]. It is clearly seen that the tunneling current starts to dominate the CP current for lower frequencies (<100 kHz), which prevents the correct extraction of any relevant interface trap parameters. Masson corrected for the leakage current by averaging the DC measured tunneling current over one CP-period and subtracting it from the measured CP-current. Another method to correct for the leakage current is by measuring the substrate current for such low CP-frequencies that the interface trap component can be neglected. Figure 9.11 (b) shows the measured charge per cycle as

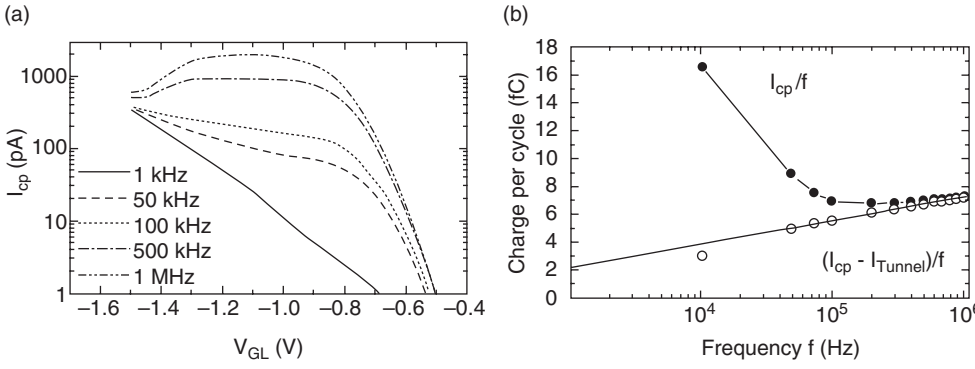


Figure 9.11 (a) Frequency dependence of charge pumping current versus gate pulse base level for an oxide of 1.8 nm thickness and gate pulse amplitude = 2 V; (b) charge per cycle as a function of frequency for as-measured and tunneling-corrected CP data [56] (Reproduced by permission of IEEE)

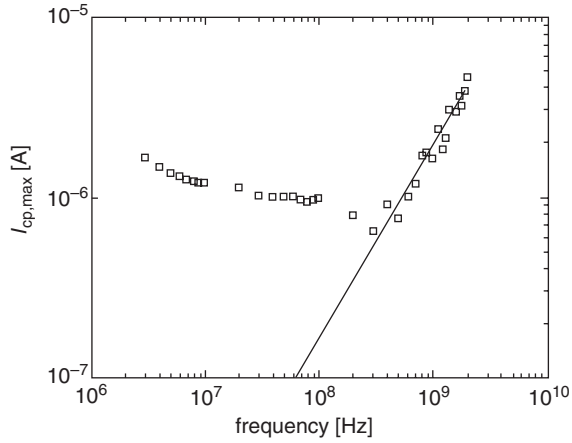


Figure 9.12 Maximum charge pumping current as a function of frequency. At low frequencies (below 300 MHz) the current is dominated by leakage current, but for higher frequencies the data can be fitted with the CP expression for sinusoidal gate waveforms [58] (Reproduced by permission of IEEE)

well as the corrected data as a function of the frequency. From the corrected data, the mean value of the interface state density can be evaluated using the classical expressions.

Another way to cope with the increased tunneling leakage current is to increase the frequency of the CP-signal. Sasse *et al.* showed that by using CP at RF frequencies up to 2 GHz the tunneling component can be overcome [57]. For this purpose they used special gated diode test structures optimized for two-port RF measurements in a ground–signal–ground configuration, and took special measures to measure accurately the applied gate voltage waveform under the RF measurement frequencies, taking into account the input impedance of the structure. The measurement approach was later refined [58]. Figure 9.12 shows the maximum measured CP-current as a function of frequency for a MOSFET with an oxide thickness of 1.4 nm. It can be clearly observed that below 300 MHz the CP-current

is completely overwhelmed by the gate leakage current, whereas above this frequency we observe the expected frequency dependence of the charge pumping data. The interface trap density can be extracted by using the CP-equation for sinusoidal waveforms:

$$\overline{D_{it}} = \frac{\log(e)}{2qkTA_G} \frac{d(I_{cp}/f)}{d(\log(f))} \tag{12}$$

For the data of Figure 9.12 an interface state density of $5 \times 10^{10}\,eV^{-1}\,cm^{-2}$ has been extracted.

Recently, an on-chip charge pumping method was proposed, where a full-pulse generator was designed on-chip, which can deliver pulses upto 500 MHz to the MOSFET [59]. By doing so the difficulties to apply the high-frequency pulses to the gate from an external pulse generator can be avoided.

A third approach to measure charge pumping in MOSFETs with ultra-thin oxides was proposed by Bauza [60]. He used charge pumping measurements with very small gate pulse amplitudes, which is based on earlier work by Wachnik *et al.* [61]. By choosing gate pulse amplitudes so low such that no emission can occur the interface trap density can be simply extracted by:

$$D_{it} = \frac{Q_{cp}}{qA\Delta E} \tag{13}$$

Contrary to the large-voltage-pulse approach, D_{it} in this case is independent of the trap capture cross-sections. If the biases between which the device is switched are between the device threshold and flatband voltages, no quantization of the inversion and accumulation layers occurs so that ΔE can be obtained in the conventional manner. In the large-voltage-swing approach, saturation of the traps with carriers is achieved by the large capture rates. In the small-voltage-swing mode, proposed by Bauza, saturation is obtained by increasing the time for capture, i.e., by decreasing the gate signal frequency. Therefore the interface trap density is obtained when $D_{it,}$ given by Equation (13), becomes independent of the pulse amplitude and frequency, when all the traps contribute to the CP-signal for the proposed small signal conditions (i.e without emission).

Figure 9.13 (a) shows measured charge pumping curves recorded at 100 kHz with various gate pulse amplitudes between 0.3 and 1 V, for a MOS device with an oxide thickness of 1.3 nm. The CP-current is easily measurable at pulse amplitudes between 0.3 and 0.4 V; at an amplitudes of 1 V the CP-curve edges begin to be influenced by the leakage current. In Figure 9.13 (b), the extracted trap densities, using Equation (13) are shown. As discussed above the extracted values saturate when the pulse amplitude increases and the frequency is reduced. Frequencies higher than 10 kHz are required to extract D_{it}. A value of about 1.3×10^{10} /eV cm^2 is found.

9.2.4 Noise characterization and modeling

The charge transport in the channel of a MOSFET is a stochastic process showing random fluctuations with time. Its power spectral density spectrum S_I typically shows a $1/f^{\gamma}$ spectrum at low frequencies (<1 MHz), with the frequency exponent γ close to 1. Fluctuations

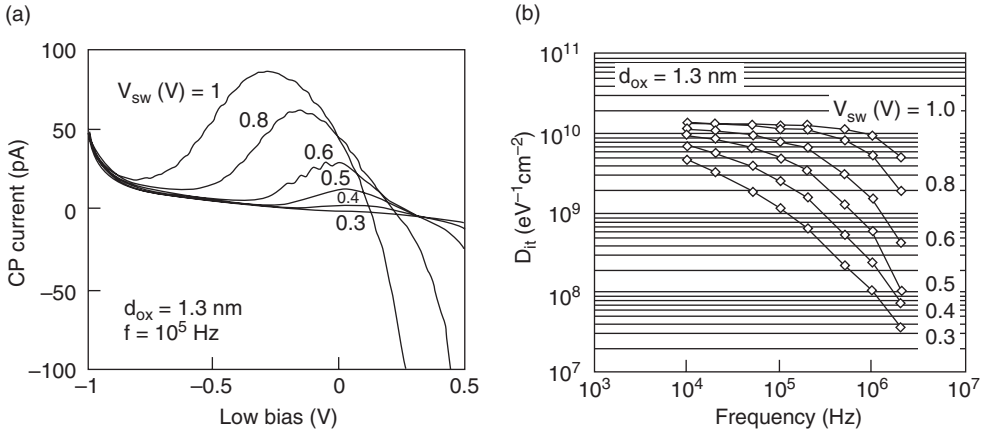


Figure 9.13 (a) CP-current as a function of pulse base level recorded at 100 kHz and various pulse amplitudes for a device 1 : 3 nm oxide thickness; (b) evolution of D_{it} given by Equation (5) for a MOSFET device with oxide thickness of 1.3 nm, as a function of the gate signal frequency for different values of the gate pulse amplitude [60] (Reproduced by permission of IEEE)

in the current can originate from fluctuations in the inversion layer mobility, in the density (number) of carriers or from both mechanisms correlated between themselves. Usually, it is assumed that the 1/*f* or flicker noise is generated by number fluctuations, coming from trapping and de-trapping of channel carriers by defect centers in the vicinity of the Si–SiO_2 interface—these centers are sometimes called border traps [62]. The 1/*f* noise spectrum is then explained by assuming in the first instance tunneling to traps at different distances z from the interface, thus resulting in a range of trapping time constants, given by:

$$\tau = \frac{1}{2\pi f} = \tau_0 \exp(\alpha_t z) \tag{14}$$

where the decay length α_t^{-1} of the electron wave function in SiO_2 is usually taken as $10^8\,cm^{-1}$ and τ_0, the time constant at the interface is 10^{-10} s [63]. The resulting input-referred noise spectral density in the ohmic regime is then given by [64, 65]:

$$S_{VG} = \frac{q^2 kTN_t}{WLC_{ox}^2 \alpha_t f} \tag{15}$$

whereby $S_{VG} = S_I/g_m^2$, with g_m the transconductance, q is the elementary charge, kT the thermal energy and C_{ox} the gate oxide capacitance density. As can be seen from Equation (15), the 1/*f* noise magnitude is directly proportional to the border trap density, i.e., to the gate oxide quality and is thus highly sensitive to dielectric processing details. Device scaling will impact the noise in two ways: lateral scaling of the transistor area WL enhances the noise accordingly, while a reduction of the gate oxide thickness t_{ox} produces a t_{ox}^2 dependence of S_{VG}. This type of reduction has been approximately found experimentally [66–68], as illustrated in Figure 9.14.

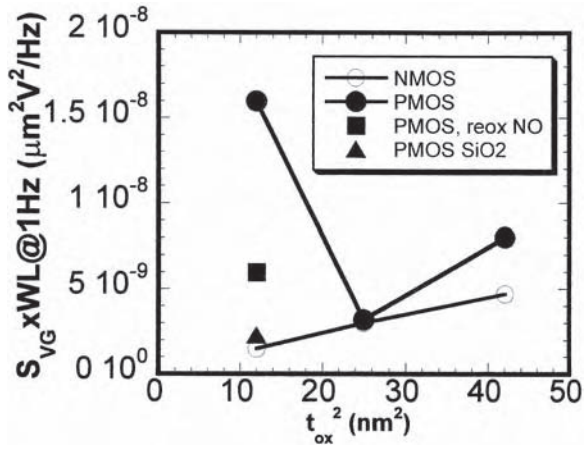


Figure 9.14 Normalized voltage noise spectral density as a function of the oxide thickness for three CMOS generations: 0.35, 0.25 and 0.18 μm. V_{GS} = 1 V, V_{DS} = 0.1 V. For the 0.18 μm technology NO-annealed oxides are considered as standard. After Da Rold *et al.* from [66] (Copyright (2001), with permission from Elsevier)

Before discussing further the impact of SiO_2 scaling on noise, it should be remarked that lateral scaling not only increases the noise magnitude according to $1/WL$ but gives rise to two other phenomena. One is that reducing the area to the submicrometer range significantly enhances the device-to-device spread in the noise magnitude [69]. This is closely related to a second phenomenon, namely, that the noise spectrum changes its character from a $1/f$-like into a Lorentzian one, typical for a generation–recombination (GR) type of spectrum, with a flat amplitude at low frequencies and a $1/f^2$ roll-off at higher f. At the same time, so-called random telegraph signals (RTS) show up in the time domain, which in their simplest form are switching of the current between two discrete levels. It has been demonstrated that such a behavior can be explained by considering the charging and discharging of a single oxide trap [70]. Therefore, it is strongly believed that RTS forms a basic component of the $1/f$ noise in large-area transistors, where more traps simultaneously contribute to the number fluctuations. More detailed overviews regarding the low-frequency noise in MOSFETs can be found in [71, 72]. It is also evident from Equation (15) that $1/f$ noise can be used to evaluate the trap density and profiles in MOSFETs [73] and, therefore, can be considered as a useful characterization tool. The difference with charge pumping is that all traps within a certain frequency range (typically 1–100 kHz) contribute to the spectrum simultaneously.

From a viewpoint of noise measurement, in the first instance, no modifications of a basic set-up is required to address thin gate oxide components. An important feature is the use of batteries to bias the device and the low-noise amplifier. The amplified noise signal is fed to a dynamical signal analyzer, that takes its Fourier transform. Usually, a second input is available, enabling the measurement of the correlation between the drain and gate current noise. A recent overview of low-noise measurement techniques can be found in [74]. Currently, commercial systems are available to perform (semi-)automatic, on-wafer low-frequency noise measurements (e.g., BTA 9812B Noise Analyzer from Cadence). With respect to RTS analysis, one can use a digital oscilloscope to capture the time traces of the

current jumps and dedicated software for the data handling. An example of an automated system for RTS can be found in [75].

Regarding the impact of SiO_2 scaling, Figure 9.14 illustrates immediately the role of the process technology used. For several reasons it turns out to be advantageous to implement a certain percentage of nitrogen in thin gate oxide. However, this is known to introduce additional traps, which may enhance significantly the $1/f$ noise, depending on the nitrogen concentration profile. For optimal noise performance, it is necessary to place the peak nitrogen concentration close to the gate electrode and away from the $Si–SiO_2$ interface [71–73, 76].

Reducing the physical gate oxide thickness enhances the vertical electric field in the silicon substrate and this, in turn, impacts on the band splitting in the two-dimensional inversion layer. As a consequence, inversion-layer quantization effects become important in thin gate oxide devices, whereby the effective (electrical) gate oxide thickness t_{oxe} becomes significantly larger than the physical one t_{ox} [77]. This also implies that the capacitance density in Equation (15) should be regarded as the effective one, based on t_{oxe}, including polysilicon depletion and inversion-layer quantization effects. Neglecting this can lead to a serious overestimation of trap densities in the gate oxide, based on Equation (15) [77].

Scaling t_{ox} brings about another effect, illustrated in Figure 9.15, where S_{VG} for a thick (30 nm) and a thin (1.5 nm) oxide $WL = 10 \times 1\,\mu m^2$ n-MOSFET is compared. While the thick oxide transistor shows a roughly gate voltage (V_{GS})-independent input-referred noise spectral density, a strong increase is observed for the thin oxide counterpart. Equation (15) does not exhibit a gate voltage dependence and is strictly speaking valid only for the weak-to-moderate inversion regime, i.e., for a gate voltage overdrive around 0 V [78]. A gate voltage dependence of S_{VG} can be explained by several effects. In the so-called correlated

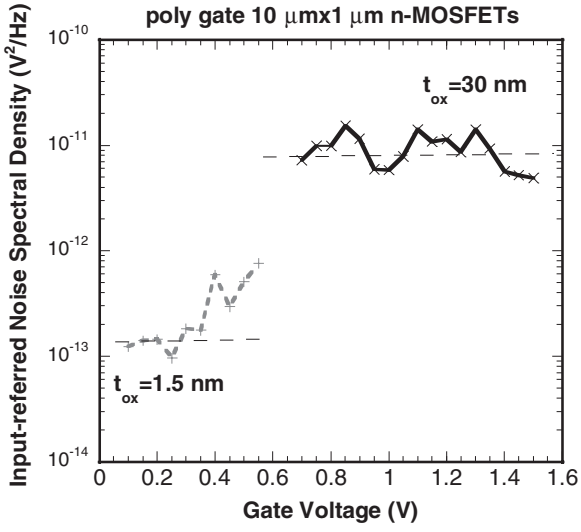


Figure 9.15 Input-referred noise spectral density for $10 \times 1\,\mu m^2$ n-MOSFETs with poly-silicon gate and $t_{ox} = 30$ nm (SiO_2) or 1.5 nm (SiON). $V_{DS} = 0.05$ V and $f = 25$ Hz

mobility fluctuations model [78, 79], charge trapping in the oxide also induces additional scattering and, hence, fluctuations in the mobility that produce a quadratic V_{GS} dependence, given by:

$$S_{VG} = S_{Vfb}[1 \pm \alpha_{sc}\mu_0 C_{oxe}(V_{GS} - V_T)]^2 \tag{16}$$

with V_T the threshold voltage, S_{Vfb} the flat-band voltage spectral density (i.e., at low V_{GS}), μ_0 the low-field mobility and α_{sc} a scattering parameter, in the range of 10^4 Vs/C cm^2. The plus or minus sign depends on the nature of the trap (attractive or repulsive).

Equation (15) predicts a quadratic V_{GS} dependence (or a linear dependence of $\sqrt{S_{VG}}$) which is typically found for thicker gate oxides. However, Figure 9.15 shows a much stronger dependence of S_{VG} on V_{GS}. It has been argued that oxide trap density profiles increasing with energy [80] or quantization effects [77] can explain this behavior. However, a factor which definitively comes into play for ultra-thin gate oxide transistors is the noise in the gate current [81–83]. The strong V_{GS} dependence then naturally follows from the strong increase of I_G with gate voltage. Another remarkable consequence is that the area scaling of the noise of Equation (15) is no longer obeyed: a turn-around behavior has been demonstrated, whereby the large-area devices become more noisy than the short-channel transistors at high V_{GS}, since I_G increases proportionally with WL [81]. A detailed modelling of the correlation between gate and channel fluctuations has been developed by Lee *et al.* [82, 83] and provides a good platform for the low- and high-frequency noise simulation in modern devices. The fundamental origin of the gate current fluctuations on the channel noise can be understood as follows: while in thick gate oxides, channel carriers only communicate with traps in the oxide at a typical tunneling distance of 1–2 nm, they can also escape to the gate electrode for thin oxides, thereby contributing to the number fluctuations in both the gate and drain current. In other words, these processes are connected or correlated.

The gate current across a thin oxide not only raises the 1/*f* noise of the channel, but gives rise to new low-frequency noise mechanisms, which are particularly important for floating-body-operated silicon-on-insulator (SOI) transistors [84–86]. An example is given in Figure 9.16 for a $10 \times 1\,\mu m^2$ partially depleted (PD) SOI *n*-MOSFET. A clear peak in the noise spectral density at 10 Hz occurs, starting around $V_{GS} = 1.1$ V. At the same time, the spectrum changes its character from 1/*f*-like to Lorentzian at low frequencies [84–86]. It has been shown that this noise peak is associated with the so-called linear kink effect (LKE) [86] in the drain current I_D or transconductance, which is created by majority carriers that are injected in the floating body by electron valence band (EVB) tunneling. The injected holes raise the body potential of the film, thereby lowering V_T and increasing the drain current. Along the same lines, the LKE noise overshoot has been modeled, assuming that it corresponds to the shot noise of the source-body and gate-body junctions that is filtered by the RC impedance of the parallel junctions [87, 88]. Meanwhile, such type of noise overshoot has been found in fully depleted SOI transistors as well, when the back-gate is in accumulation [89]. It has also been reported that EVB tunneling may give rise to a new type of RTS mechanism in bulk MOSFETs, whereby electrons and holes recombine through interface traps [90]. The introduction of thicker layers of a high-*k* dielectric may suppress these specific ultra-thin gate noise mechanisms, as long as the thickness and barrier heights are high enough to eliminate the injection of majority carriers in the underlying silicon substrate/floating body.

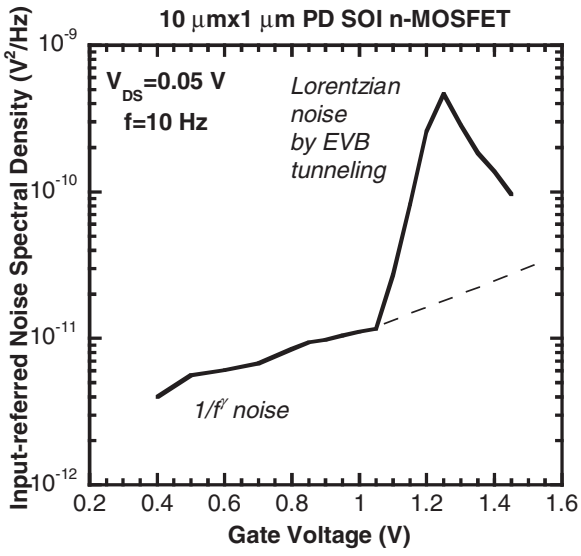


Figure 9.16 Input-referred noise spectral density at $f = 10\,\text{Hz}$ and in linear operation ($V_{DS} = 0.05\,\text{V}$) for a $10 \times 1\,\mu\text{m}$ PD SOI *n*-MOSFET

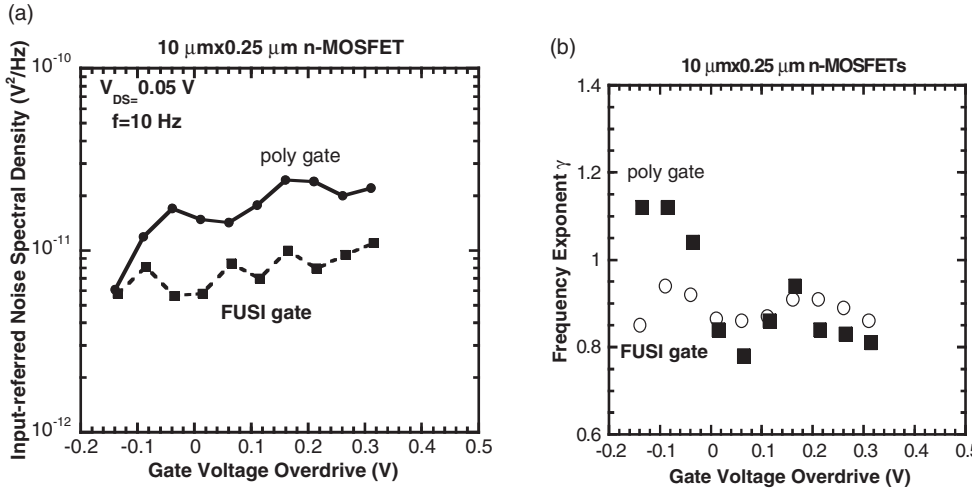


Figure 9.17 (a) Input-referred noise spectral density versus gate voltage overdrive for a $10 \times 0.25\,\mu\text{m}$ *n*-MOSFET with a 1.5 nm SiON gate dielectric and a polycrystalline silicon (poly) or a fully (nickel-) silicided (FUSI) gate electrode; (b) corresponding frequency exponent of the LF noise spectra

A final factor that should be taken into account for ultra-thin SiO_2 is the proximity of the gate electrode to the channel, within direct tunneling distance. It has already been noted in the past that, depending on the gate oxidation technology, excess noise can occur at low frequencies—the so-called $1/f^{1.7}$ noise [91]. This extra noise component has been ascribed to the existence of a trap profile connected with the gate electrode, i.e., with a concentration increasing closer to the gate. An example is also given in Figure 9.17 (a) for a 1.5 nm SiON

transistor with a polysilicon gate. The frequency exponent in Figure 9.17 (b) is higher than 1 for low V_{GS} and this is indicative of a density of traps that increases with distance from the Si–SiO_2 interface. According to Equation 9.14, a higher time constant corresponds with a larger z and a smaller frequency. Replacing the polysilicon gate material by a fully silicided (FUSI) gate leads to a pronounced reduction in the $1/f$ noise spectral density, as can be verified in Figure 9.17 (a) [92]. At the same time, the frequency exponent becomes more or less independent on V_{GS} and smaller than 1, i.e., with a trap density profile increasing towards the Si–SiO_2 interface. This points either to the removal of the oxide traps close to the gate or to a screening of the impact of these traps by the higher electron density at the gate–SiO_2 interface in the metallic FUSI gate. This could be related to a change in the work function (Fermi level position) of the gate electrode.

Summarizing the foregoing, it is clear that scaling the gate oxide thickness has a tremendous impact on the low-frequency noise of MOSFETs, leading to a significant increase of the $1/f$ noise or to the occurrence of new excess noise mechanisms. Both technological and fundamental factors contribute to this noise degradation with scaling and their role should be well understood in order to optimize the noise performance of deep submicrometer transistors. At the same time, it has become clear that the traditional engineering models for LF noise, successful in the past decade and based on the correlated mobility fluctuations theory are no longer capable of capturing all features of the noise behavior. A first step towards a better noise modeling includes the impact of the gate current of thin oxide devices. The next step is to include the impact of the gate–oxide interface.

9.2.5 Time-dependent dielectric breakdown

In Section 9.2.1, the different stages of leakage current increase after continuous electric stress have already been introduced: Stress-induced leakage current (SILC), soft and hard breakdown. This section focuses on the various aspects of dielectric breakdown in very thin (<5 nm) gate dielectrics that are used in advanced CMOS technologies. The phenomenon of soft breakdown is described in more detail: its appearance, the detection issues and statistical properties. An overview is presented of the recent developments in voltage acceleration and corresponding lifetime prediction methods. Finally, the so-called progressive breakdown, which is the most commonly observed breakdown mode in very thin gate dielectrics at low voltage, is discussed.

Soft breakdown

Dielectric breakdown is caused by the formation of a conductive path that connects the electrodes. In thick dielectrics stressed at high voltage, the creation of this path is followed immediately by the propagation of thermal damage leading to a low-ohmic connection between gate and substrate. This is the hard breakdown that results in device failure. However, it has been known for several years that ultra-thin oxides can have ‘anomalous’ failure [93], characterized by the creation of a more resistive breakdown path: soft breakdown (SBD). Many synonymes are used in literature for soft breakdown: quasi, early, non-destructive, electric breakdown or B-mode SILC [94–110].

Soft breakdown can be defined as an oxide breakdown without the lateral propagation of the breakdown spot due to thermal damage [96]. It is generally accepted that soft and hard breakdown originate from the same precursor [104, 111], show the same stress current dependence [106] and can be described by the same Weibull statistics [111, 112].

In Figure 9.18, a typical example is shown of the gate current vs gate voltage immediately after soft breakdown. A sudden current rise compared to SILC is observed, but the SBD is less destructive when compared with the hard breakdown. It has been shown that the gate current after soft breakdown is a unique curve as a function of the gate voltage independent of area, proving that soft breakdown is indeed a localized effect [100]. This conclusion is confirmed by emission microscopy experiments [101]. However, for very small areas, a lower, unstable current is measured [100]. This might be explained by the difference in energy available for discharging at the moment of breakdown.

Typically, when the applied voltage is plotted as a function of time during a constant voltage stress, SBD is indicated by a jump of the current (or equivalently a small decrease of the voltage during constant current stress). This jump is weaker than the hard-breakdown, and can be hard to indentify when large-area capacitors are tested. Soft breakdown also induces a sudden increase of the gate current noise, which has been studied as a SBD detection monitor [99, 113].

In typical large-area test structures, the small voltage or current jumps indicating soft breakdown become very difficult to detect with automated measurement systems. Therefore, other breakdown detection methods have been proposed. The most interesting one is using the sudden increase of the noise in the gate current as detection monitor [99, 113].

This noise has been studied carefully [100, 102, 103, 106, 114, 115]. At low gate voltage, two-level and multilevel random telegraph signals are observed with current amplitudes that are depending on the applied gate voltage. An example is shown in Figure 9.19. It has been

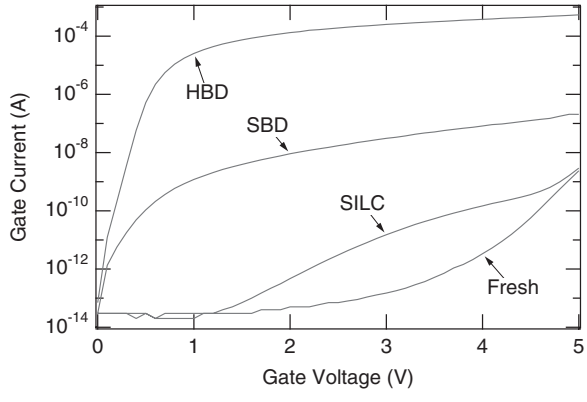


Figure 9.18 I_G–V_G curves for a capacitor with oxide thickness 4.5 nm. A comparison is made between the current in the fresh device, after stress (SILC), after soft breakdown and after hard breakdown (from [100])

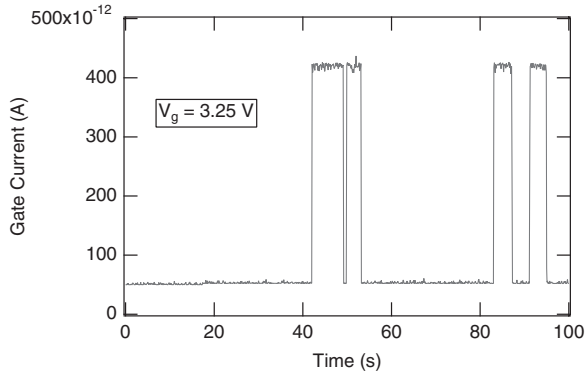


Figure 9.19 Example of two-level random telegraph signal in the gate current of a capacitor after soft breakdown [100] (Reproduced with permission of IEEE)

demonstrated that the current–voltage characteristics of the ON and OFF state are shifted over a constant voltage interval [100]. This observation can be explained by electron capture-emission-induced local field fluctuations in the breakdown path [100, 102]. With this model, the area of the soft breakdown spot is estimated to be $2 \times 10^{-13}\,\mathrm{cm}^2$ [100].

The current conduction mechanism through soft-broken spot in the oxide has been modeled in several ways, and the correct physical picture is still not completely clear. Models based on variable range hopping of carriers [97, 116], point contact conduction [117, 118], energy funnels [98], resonant tunneling through strategically placed traps [119, 120], direct tunneling through a thinned oxide region [95, 121] and electrode-controlled conduction [115] have been proposed.

SBD adds leakage current to the gate current, but no significant variations in MOSFET I_D–V_G characteristics can be observed and therefore, for some applications, SBD does not necessarily imply device failure [99, 122]. However, it has been demonstrated that for transistors with very small channel length, soft breakdown no longer occurs. Instead hard breakdown is immediately observed [104, 105]. Since the reliability of small-geometry devices has to be guaranteed, this means breakdown might still be a reliability limiting process.

Statistical modeling of breakdown

Already in the beginning of the 1990s, Suñé and co-authors [123] presented a 'weakest link' breakdown model [124, 125]. In this model, a capacitor is divided into a large number of small cells. It is assumed that during oxide stressing neutral electron traps are generated at random positions on the capacitor area. The number of traps in each cell is counted, and at the moment that the number of traps in one cell reaches a critical value, breakdown occurs by definition. The point is that in that critical cell the number of traps is sufficiently large to create a conductive path from anode to cathode via these traps.

A disadvantage to the model of [123] is its two-dimensional nature. In more recent work a three-dimensional weakest link model has been proposed that can accurately describe the

intrinsic breakdown distribution. This model is based on the principles of percolation theory [126]. The use of the percolation concept for modeling of oxide breakdown has been suggested in [127] and has been thoroughly elaborated in [128–131]. The percolation model for breakdown exists in two versions: (1) the 'sphere' model, where each generated defect in the oxide is characterized by a sphere with radius 0.9 nm; and (2) the 'cube' model, where each defect is represented by a cube with size 1.3 nm in a three-dimensional frame. Both models are implementations of the same concept and provide, therefore, similar results. As an example, the 'sphere' model of [128] is schematically illustrated in Figure 9.20.

It is assumed that electron traps are generated inside the oxide at random positions in space. Around these traps a sphere is defined with a fixed radius r, which is the only parameter of the model (Figure 9.20a). If the spheres of two neighboring traps overlap, conduction between these traps becomes possible by definition. Also, the two interfaces are modelled as an infinite set of traps (Figure 9.20b).

This mechanism of trap generation continues until a conducting path is created from one interface to the other, defining the breakdown condition (Figure 9.20c). In a computer simulation, the total electron trap density needed to trigger breakdown $D_{\mathrm{ot,crit}}$ can now be

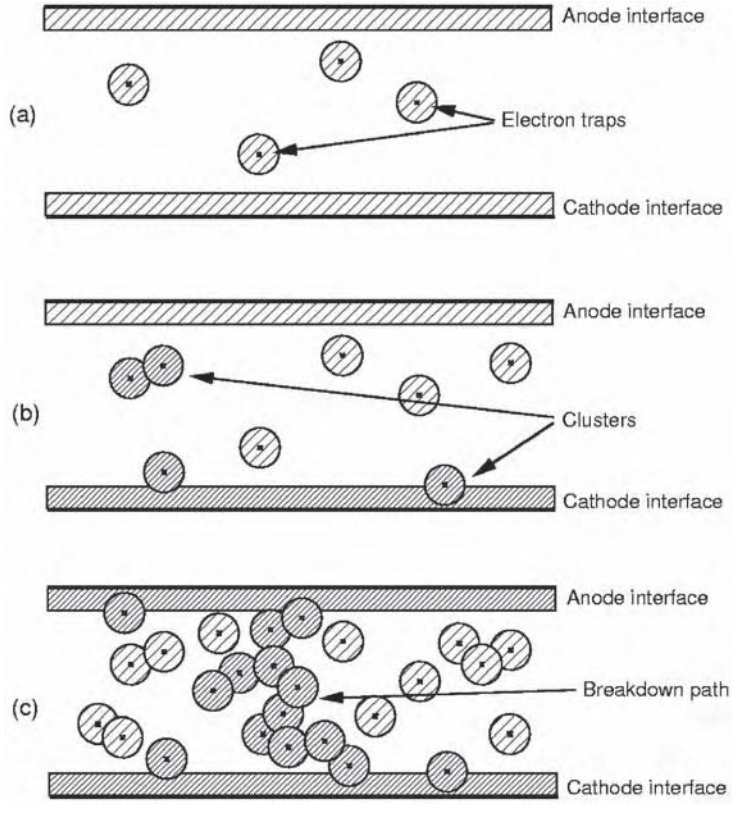


Figure 9.20 The percolation model for oxide breakdown explained step by step. As the density of neutral electron traps increases, conductive clusters of traps are formed, ultimately leading to the creation of a conductive breakdown path from anode to cathode [111] (Reproduced with permission of IEEE)

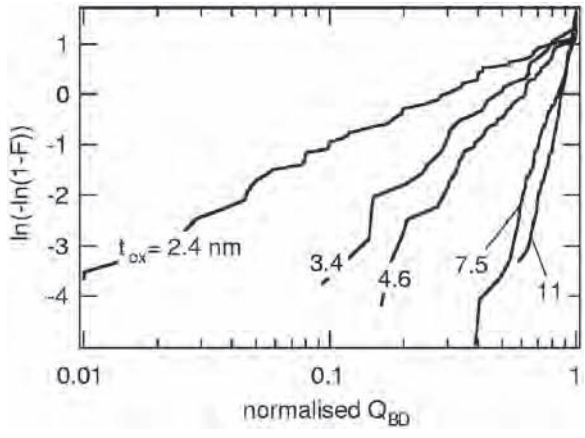


Figure 9.21 Normalized Q_{BD} distributions for different oxide thicknesses. The decrease of the Weibull slope with oxide thickness is clearly observed experimentally [129] (Reproduced with permission of IEEE)

calculated. It is found that the simulated $D_{ot,crit}$ distribution can be fitted with a Weibull expression [130]. This distribution can be easily associated with the time-to-breakdown or charge-to-breakdown distribution [129].

The percolation model for breakdown is able to explain quantitatively two important experimental observations: (i) as the oxide thickness decreases, the density of oxide traps needed to trigger breakdown decreases [128, 129, 132]; and (ii) as the oxide thickness decreases, the Weibull slope of the breakdown distribution decreases, i.e., a larger spread on the breakdown values is observed [128, 129, 131, 133]. The latter effect is illustrated in Figure 9.21.

An important consequence of the decreasing Weibull slope for thinner oxides, is the strongly increased area dependence of the time-to-breakdown or charge-to-breakdown [129, 133]. Indeed, based on the random character of the breakdown position, it has been shown that the for the scale factors η_1 and η_2 of two Weibull distributions (either t_{BD} or Q_{BD} distributions) of capacitors with identical oxide thickness, but area A_1 and A_2 respectively, the following relationship holds [134, 135]:

$$\frac{\eta_1}{\eta_2} = \left(\frac{A_2}{A_1}\right)^{\left(\frac{1}{\beta}\right)} \tag{17}$$

As β decreases, the area dependence becomes stronger. This is illustrated in Figure 9.22. It can be concluded that for thick oxides (t_{ox} > 10 nm), the intrinsic Q_{BD} value is, with acceptable approximation constant, in the range of capacitor areas commonly available for experimental purposes, but for thin oxides the Q_{BD} can no longer be considered area independent. This has important implications when the Q_{BD} value is used as a the figure of merit for the oxidation process, as is commonly done in an industrial environment. It is meaningless to specify a Q_{BD} value without specifying the area, and it is also mandatory to specify the area when Q_{BD} values of different oxide thicknesses are compared.

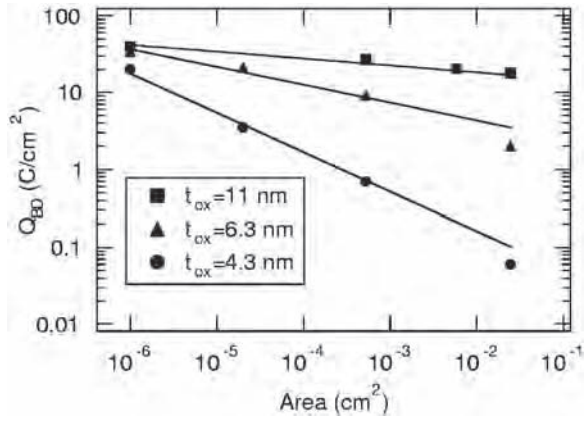


Figure 9.22 The 63% value of Q_{BD} as a function of the area of the test capacitor for different oxide thicknesses (gate injection). As the oxide thickness decreases, a strong area dependence is observed [129] (Reproduced with permission of IEEE)

Breakdown acceleration models

The time-to-breakdown is collected at high stress voltage and in order to predict the oxide reliability at operating conditions, it is important to choose the correct field or voltage extrapolation law. There has been a continuous evolution in the development of the voltage dependence of time-to-breakdown. Some research groups claim that, based on the anode injection model, the logarithm of time-to-breakdown scales with the inverse of the oxide field E_{ox}, whereas others find better results using an E_{ox} dependence. More recently, it was shown that the oxide voltage rather than the field controls the time-to-breakdown in ultra-thin layers where ballistic transport of electrons through the oxide occurs. The most recent publications show experimental evidence that time-to-breakdown scales as a power law with the gate voltage, and theoretical models have been proposed to explain this dependence. This section presents a brief overview of the various field and voltage extrapolation methods, but the reader should be aware of the still ongoing developments in this area of reliability analysis.

According to the anode hole injection model [136–138], the field dependence of α, which is the probability of creating a hole which can tunnel back into the oxide, can be described as:

$$\alpha = \alpha_0 \exp\left(\frac{-H}{E_{OX}}\right) \qquad \text{and} \qquad Q_{BD} = Q_0 \exp\left(\frac{H}{E_{OX}}\right) \tag{18}$$

with α_0 and H constants (for a fixed oxide thickness) and $Q_0 = Q_{p,crit}/\alpha_0$. With this equation, the time-to-breakdown becomes:

$$t_{BD} = \frac{Q_{BD}}{J_{FN}} \simeq \frac{Q_{BD}}{A^*} \exp\left(\frac{B^*}{E_{OX}}\right) = \frac{Q_0}{A^*} \exp\left(\frac{B^* + H}{E_{OX}}\right) = \tau_0 \exp\left(\frac{G}{E_{OX}}\right) \tag{19}$$

with τ_0 a constant. Reported values for $G = B^* + H$ vary from 290 to 350 MV/cm, depending on oxide thickness and stress type (CVS or CCS). Equation (19) expresses the so-called 1/E model, because the logarithm of t_{BD} depends linearly on the reciprocal oxide field.

The E model, on the other hand, predicts a linear relationship between the logarithm of the time-to-breakdown and the oxide field [139–141]:

$$t_{BD} = t_0 \exp(-\gamma E_{OX}) \tag{20}$$

with t_0 and γ constants. This model has been used long before there existed any physical argumentation to support it. In the literature of the past years publications trying to prove the correctness of either the E or the $1/E$ model can be found [125, 142–145].

All models that provide the E model with a physical base assume that a direct correlation exists between the electric field and the oxide degradation, i.e., all of these models ignore the role of the injected electrons as an intermediate step for generating oxide traps. More recent experiments clearly demonstrate that the oxide degradation process is fluence-driven [146, 147].

Furthermore, detailed simulations of anode hole injection including minority-carrier ionization [148, 149], no longer link a $1/E$ model directly with the anode hole injection concept. Instead, a mixed model with approximate $1/E$ dependence at high voltage and E dependence at low voltage is found. Other groups have proposed similar 'unified' E–$1/E$ models [150–153].

The E-model vs $1/E$ model discussion mainly concerns oxides thicker than 5 nm, where the injection of electrons is dominated by nonballistic F–N injection. The injected electrons enter the conduction band of the silicon dioxide and interact with the SiO_2. The oxide field mainly determines the electron energy at the anode and consequently the oxide degradation. Since there exists a unique relationship between the F–N current density and oxide field, the charge-to-breakdown should be measured using constant current stress.

For ultra-thin oxides (<5 nm) however, the injected electrons travel ballistically through the oxide without interacting with the SiO_2 lattice. This can be either by F–N tunneling above 3.5 V, typically in oxides with thickness between 5 and 3.5 nm, or by direct tunnelling below 3.5 V, typically in oxides with thickness below 3.5 nm. The electron energy at the anode is determined by the voltage difference between the cathode and the anode, which corresponds to the applied gate voltage [146, 149, 154]. As a consequence of this, the charge-to-breakdown should be measured using constant voltage stress [154]. This means also that for an ultra-thin oxide the gate voltage determines the breakdown, and the constant current stress methodology needs to be replaced by constant-voltage stress evaluations [154, 155].

Based on extensive experimental data on very thin oxides, it was shown [156] that the t_{BD} and the oxide voltage are correlated through a power law:

$$t_{BD} = t_0 V_G^n \tag{21}$$

with n of the order of 40–45. This dependence is more and more accepted as the correct way to extrapolate time-to-breakdown for very thin oxide layers stressed at low voltage in the direct tunneling regime. Physical models that support the power law model are still being developed.

Progressive breakdown

One of the most important complications in the analysis of dielectric breakdown in very thin oxide layers used in advanced CMOS technologies is the so-called progressive breakdown [157–163]. While in the 'classical' approach, the breakdown is considered to occur at a well-defined moment in time, the time-to-breakdown, this simple concept no longer holds for ultra-thin dielectrics stressed at low voltage. Only the formation of the conductive path between the electrodes happens at a well-determined moment in time and the voltage extrapolation models of the previous section refer to the how the occurrence of this event scales with stress voltage.

After the formation of a conductive path (this is 'soft breakdown'), the leakage current increase is very small and therefore the device will in most cases continue to work normally. The conductive path will slowly wear out and after some time result in a complete breakdown that also corresponds with operational device and circuit failure. With this progressive wear-out phase, gate oxide failure can no longer be characterized by a single breakdown distribution. Instead, concepts such as the 'first time-to-breakdown' and the 'final breakdown' are needed to comprehensively describe the complete breakdown process [161].

In summary, we can state that nowadays three phases are identified in the oxide degradation and breakdown process, as schematically illustrated in Figure 9.23. In the first phase electron traps are created in the dielectric. This continues until a percolation path is created at a random place on the device area. The percolation path will act as a conducting filament connecting the electrodes and its formation is therefore observable as a sudden small increase of the leakage current. In thick (typically $t_{ox} > 5\,\text{nm}$) SiO_2 layers and at 'high' stress voltage (typically $V_G > 6\,\text{V}$), the creation of the percolation path immediately results in hard oxide failure and therefore ends the degradation process. All published work on oxide degradation mechanisms and voltage acceleration models refer to the first phase in Figure 9.23, ending with a breakdown at the moment the percolation path is created.

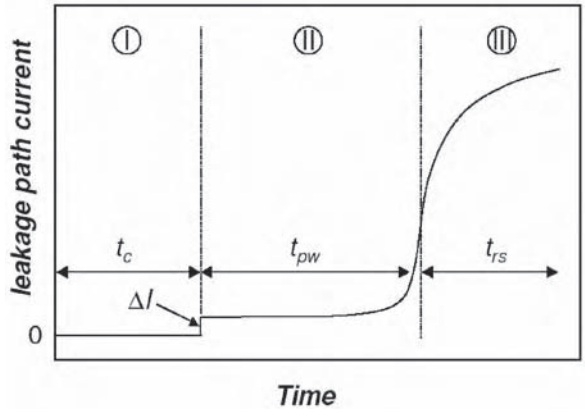


Figure 9.23 The time evolution of the current I in a leakage path. The time-to-creation of a leakage path t_c is controlled by the percolation process (part I). When the path is created at $t = t_c$, its leakage is ΔI. From that moment on the path progressively wears out (part II). Time t_{pw} represents the time from t_c to a significant current increase. Eventually, the leakage current will become limited by a series resistance and will start leveling off (part III) [162] (Reproduced with permission from IEEE)

In very thin SiO_2 and SiON layers and at low voltage, the formation of the percolation path does, however, not correspond to immediate oxide failure. Instead, the percolation path needs some wear-out time (phases II and III in Figure 9.23) until the leakage current has increased sufficiently to cause device failure. In this wear-out phase two parts can be distinguished: first a phase with increased gate current noise, but on average a relatively stable current level (phase II in Figure 9.23) and second, a current runaway that is limited by the gate resistance (phase III in Figure 9.23). In the thickness range 1–3 nm, phase II is characterized by a discrete number of current levels and is therefore sometimes named digital soft breakdown, while phase III is sometimes referred to as analog breakdown [106, 159].

Progressive breakdown is of crucial importance to guarantee the reliability of dielectrics in advanced CMOS circuits because it allows to relax the reliability specifications. If soft breakdown were to correspond to device failure, the oxide thickness scaling would have stopped because of reliability considerations. The extra margin that becomes available due to the slow wear-out of a soft breakdown is needed to meet the reliability specifications in ultra-thin layers.

9.2.6 Negative-bias temperature instability

When a *p*MOSFET is stressed under inversion condition (i.e., negative gate bias), at elevated temperature (above 100°C), the threshold voltage V_{th} of the device shifts towards more negative values, while the drain current and transconductance of the device decrease. This device degradation phenomenon is called negative-bias temperature instability (NBTI) and is presently considered as one of the most serious reliability concerns for ultra-thin nitrided oxides layers [164].

Measurement procedure

The conventional method used to characterize NBTI consists in measuring the I_D–V_G characteristics of the device periodically during the electrical stress, performed under constant negative gate voltage at temperatures ranging between 100 and 150°C. The (stress) time-dependence of the threshold voltage is extracted from these measurements, and the device lifetime is extrapolated, assuming that device failure occurs when a given shift in V_{th} is reached. Typical failure criterions are 10% or 30 mV shift in V_{th}.

However, as will be discussed in more detail below, a substantial recovery in V_{th} is observed when the electrical stress is interrupted [165, 166], as illustrated in Figure 9.24. Consequently, the conventional stress-sense method has been modified in order to reduce the recovery effect as much as possible.

This new characterization method consists in applying a pulsed-like stress on the gate of the transistor, as shown in Figure 9.25 [167–169]. The transistor is stressed under NBT conditions at $V_{G,stress}$, and the drain current I_D is measured when the gate bias is switched to $V_{G,sense}$. The delay in switching between $V_{G,stress}$ and $V_{G,sense}$ is minimized, in order to reduce the V_{th} recovery effect. The evolution of the drain current is then recorded during the electrical stress. The $I_D(t)$ trace is next converted to a $V_{th}(t)$ trace, by interpolating the I_D–V_G characteristics of the device (recorded before the NBT stress is applied).

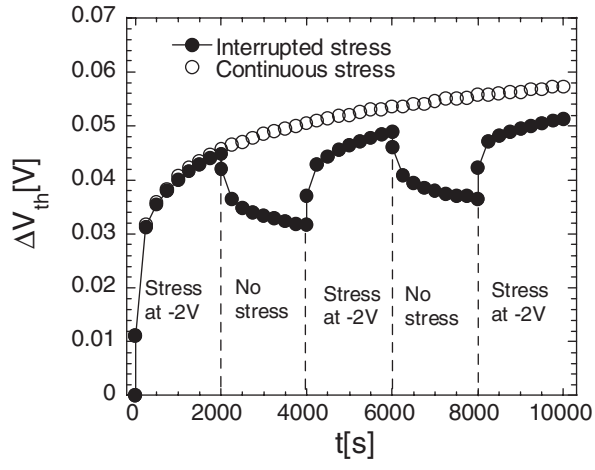


Figure 9.24 Illustration of the V_{th} recovery effect observed when the NBT stress is interrupted (solid symbols). The open symbols correspond to continuous stress of the device (Reprinted from [250], Copyright (2005) with permission from Elsevier)

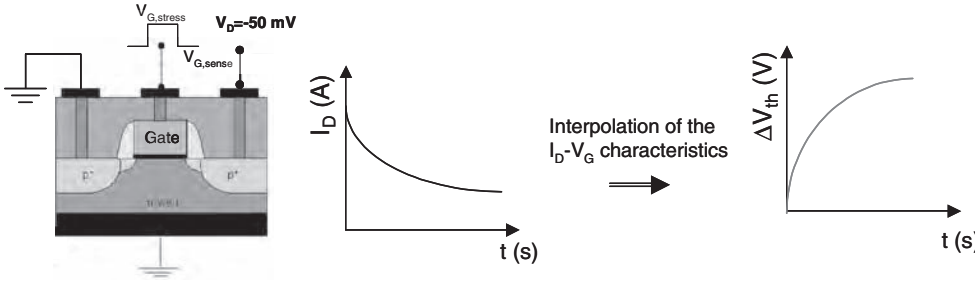


Figure 9.25 Illustration of the pulsed V_G stress method used to characterize NBTI. This method allows one to minimize the V_{th} recovery effect

Models

The shift in the threshold voltage during negative-bias temperature stress can be phenomenologically described by the expression

$$\Delta V_{th} = CE_{ox}^{m} \exp\left(\frac{-E_a}{k_B T}\right) t^{\alpha} \tag{22}$$

where E_{ox} is the electric field across the SiO_2 layer, m~3–4, E_a~0.1–0.2 eV is an apparent activation energy and α~0.2–0.3 is the characteristic power-law time exponent of NBTI. The most popular model that allows one to explain the characteristic time and temperature dependence of ΔV_{th} is the so-called reaction-diffusion model [170–173]. Holes attracted at the (100)Si/SiO_2 interface are supposed to depassivate silicon trivalent dangling bonds at this interface, namely P_{b0} centers, previously passivated by hydrogen during the forming

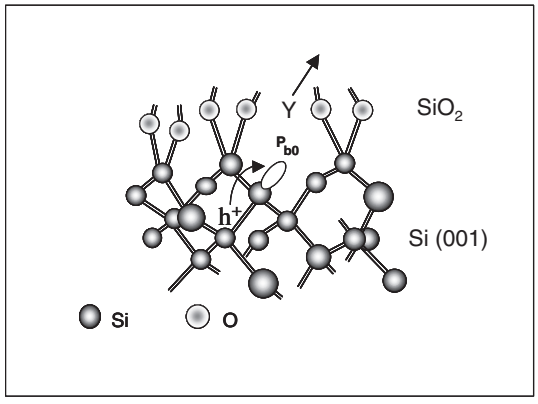


Figure 9.26 Schematic illustration of the generation of P_{b0} centers at the (100)Si/SiO_2 interface during NBT stress. Y represents a hydrogen species liberated during the dissociation of the $P_{b0}H$ centers. The characteristic temperature and time dependence of ΔV_{th} is predicted correctly by the model, assuming the diffusion of a neutral hydrogen species as the rate-limiting step for the generation of P_{b0} centers

gas anneal of the device. This results in the generation of positively charged interface states, responsible for the V_{th} shifts, as well as the liberation of hydrogen species (H^+, H^0, H_2, etc.), as illustrated in Figure 9.26. A key assumption of this model is that the rate-limiting step for the generation of P_{b0} centers is the diffusion of the hydrogen species away from the Si/SiO_2 interface.

This model predicts that V_{th} shifts should increase with time like a power law, with an exponent 0.25 if diffusion of a neutral hydrogen species is considered, and that V_{th} shifts should follow an Arrhenius temperature dependence, with an apparent activation energy ~0.2 eV [171]. This model has been recently adapted to account for the dispersive transport of H^0 or H^+ away from the Si/SiO_2 interface [174–176], which allowed one to consistently explain the time, temperature and field dependence of the P_{b0} generation, together with the polarity effect observed on device degradation, namely the much reduced device degradation observed under positive-bias temperature stress [177, 178].

An alternative explanation for NBTI is the trapping of holes injected from the channel of the transistor during the electrical stress [169, 179, 180]. This hole trapping mechanism results in the build-up of positive charges in the gate dielectric, leading to V_{th} shifts.

Impact of nitridation of the gate dielectric layer

The presence of nitrogen near the Si/SiO_2 interface leads to enhanced device degradation under NBT stress [181–183]. The extrapolated device lifetime, based on 10% shift of the drive current is shown in Figure 9.27 as a function of the stress voltage, for *p*MOSFETs with 2 nm SiO_2 and SiON layers [183]. Device lifetime is strongly reduced when the N content in the gate dielectric layer increases.

A possible interpretation of the role of nitrogen on NBTI considers that holes injected from the channel during electrical stress can be trapped at nitrogen-related defects, possibly

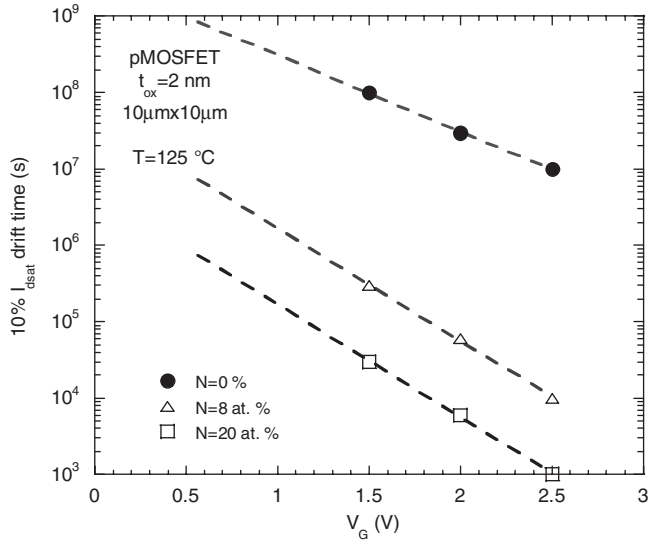


Figure 9.27 Extrapolated lifetime of *p*MOSFETs with different N content in the gate dielectric layer, as a function of the gate bias [183] (Reproduced with permission of AIP)

N vacancies, leading to the generation of bulk positive charges [180, 183]. Another recent model [184, 185] suggests that the presence of N near the interface decreases the activation energy for the depassivation of $P_{b0}H$ centers, leading to enhanced NBTI. Finally, it has been also suggested that the incorporation of nitrogen could change the properties of hydrogen transport in the oxide [186].

Recovery effects

As mentioned previously, partial recovery of the device characteristics is observed when NBT stress is interrupted. As can be seen in Figure 9.28, recovery of V_{th} at $V_G = 0\,V$ spans many decades in time, suggesting a *dispersion* in the characteristic time of the NBTI mechanism. The logarithmic shape of the recovery also illustrates the requirement of minimizing the measurement of V_{th}, as discussed above.

It has been shown that NBTI recovery is enhanced when the gate voltage is switched positive after NBT stress, as also illustrated in Figure 9.28. The temperature dependence of NBTI recovery is not well understood. Observed temperature dependences range from weak [168] to a reduced recovery at a higher temperature (so-called lock-in effect) [167].

The interpretation of the recovery effect is still much debated. One possible mechanism consists in the re-passivation of dangling bonds by hydrogen species coming back to the Si/SiO_2 interface when the stress is interrupted [172, 173]. This is the so-called generalized reaction-diffusion model, which was shown recently to be consistent with several experimental observations. Note that the effect of positive gate bias on recovery (see Figure 9.28), within this interpretation, would suggest the migration of a positively charged hydrogen species, possibly H^+.

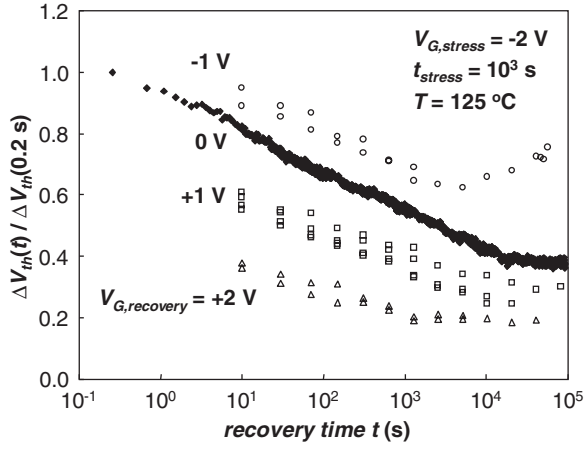


Figure 9.28 The recovery of ΔV_{TH} at $V_G = 0$ V follows the log(t) dependence for more than five decades. The data are normalized to the first point measured. The recovery is accelerated by application of positive V_G [168] (Reproduced with permission of IEEE)

The alternative model suggests that recovery is solely related to the detrapping or neutralization of holes [165, 169, 180]. In this model, a large fraction of defects produced during NBT stress is assumed to be holes trapped at defects located in the gate dielectric layer. Once the NBT stress is interrupted, holes can be detrapped or neutralized, possibly via a thermally assisted process. The effect of positive gate bias on recovery also naturally follows from this interpretation, assuming an electric-field-assisted detrapping/neutralization mechanism.

9.3 CHARACTERIZATION OF HIGH-*k* DIELECTRICS AND METAL GATES

9.3.1 Effective oxide thickness: EOT vs CET

One of the most important benchmarks to qualify a high-k gate stack is the effective oxide thickness (EOT). The EOT is inversely proportional to the maximum capacitance in accumulation and depends on several factors:

$$\mathrm{EOT} = t_{\mathrm{SiO_2}} + t_{\mathrm{high-}k}\frac{k_{\mathrm{SiO_2}}}{k_{\mathrm{high-}k}} \tag{23}$$

where $t_{\mathrm{SiO_2}}$ is the physical thickness of the eventual interfacial SiO_2 layer ($k_{\mathrm{SiO_2}} = 3.9$) and $t_{\mathrm{high\text{-}}k}$ is the physical thickness of the high-k layer with dielectric constant $k_{\mathrm{high\text{-}}k}$. To achieve the lowest EOT (i.e., highest capacitance) the $k_{\mathrm{high\text{-}}k}$ has to be high together with a thin $t_{\mathrm{SiO_2}}$. The EOT is usually determined from the fitting of the experimental C–V trace [187–190]. For a given set of samples with identical characteristics (processing conditions, gate material, post-deposition annealing, etc.) and different $t_{\mathrm{high\text{-}}k}$, the $t_{\mathrm{SiO_2}}$ and $k_{\mathrm{high\text{-}}k}$ can be determined

by plotting the EOT vs $t_{\text{high-}k}$ and assuming a linear relationship as in Equation (23). (This is usually accomplished using a transmission electron microscope profile of the stack.)

From a MOSFET operation standpoint, however, the total charge in inversion is more important then the effective oxide thickness. The capacitive equivalent thickness (CET) is a measure of the charge in the inversion channel and is proportional to the charge present in the MOSFET channel at inversion. For a given bias, the MOSFET drive current is proportional to the channel mobility *and* the total charge at inversion.

For a given electric field in the silicon layer (large enough), the charge measured in accumulation is larger than in inversion (i.e., CET < EOT). This is due to two effects: charge distribution in the channel and gate electrode depletion. With respect to the accumulation case, the channel electrons energy distribution is quantized (similar to a two-dimensional gas [191]). As already discussed in Section 9.2.2 on average the inversion electrons are roughly 1 nm away from the interface between the Si and the dielectric, thus effectively increasing the CET. The overall effect on the CET is ~0.4 nm. In other words, if a CET of 1 nm is required for future CMOS technologies, the combination of high-k and t_{SiO_2} has to be chosen such that EOT ~ 6Å. To further limit the CET scaling, when a semiconductor electrode is used (i.e., degenerately doped poly-Si) the source of carriers is limited by the electrode effective doping density. Due to electrostatic effects, the charge in the channel has to be screened by the same amount of charge (different sign) in the gate electrode. In conventional poly-Si technology the available minority carrier density is limited by the doping level and dopant solubility in the poly-Si [192]. In inversion conditions the poly-Si depletes to screen the charge at inversion. This depletion layer adds up to the CET. For a given doping level and impurity activation, the poly-Si depletion contribution to CET increases as the EOT is reduced.

9.3.2 Gate workfunction

Importance of V_t and V_{fb} control in high-k dielectrics

Another very important parameter for high-k/metal gate stack is the workfunction of the gate. When high-k was first put into devices with poly-Si gates [193], several important problems were observed. First of all the control of the flatband voltage V_{FB}, and threshold voltage V_{th} of the devices was problematic and, furthermore, the CET was much higher than expected. Figure 9.29 nicely illustrates the problem. The presence of a monolayer[5] of HfO_2 in close contact to poly-Si already changes the V_{FB} and V_{th}, with respect to the ideal SiO_2/poly-Si reference system. The ΔV_{FB} is asymmetrical: (a) $\Delta V_{FB} > 0$ for n^+-poly-Si; and (b) $\Delta V_{FB} < 0$ for p^+-poly-Si. Several models were proposed to explain these effects. These can be broadly grouped in two categories: poly-Si dopant effects [194] and interreaction between the high-k and the poly-Si [195–197]. (Note that a monolayer of HfO_2 is defined as the number of HfO_2 atoms necessary to cover the SiO_2 surface (by roughly 3Å). For more details on the deposition see [196] and references therein.)

Hobbs *et al.* [195] proposed that the interaction of Hf atoms with the poly-Si layer was creating a large density of defects in the Si bandgap, able to 'pin' the Fermi level, effectively changing the gate electrode workfunction, hence, the V_{FB}. The asymmetric V_{FB} shift observed in n^+ and p^+ gates could then be explained by the distribution of defects across the bandgap of the poly-Si layer, as also predicted by density functional theory (DFT) calculations [195,

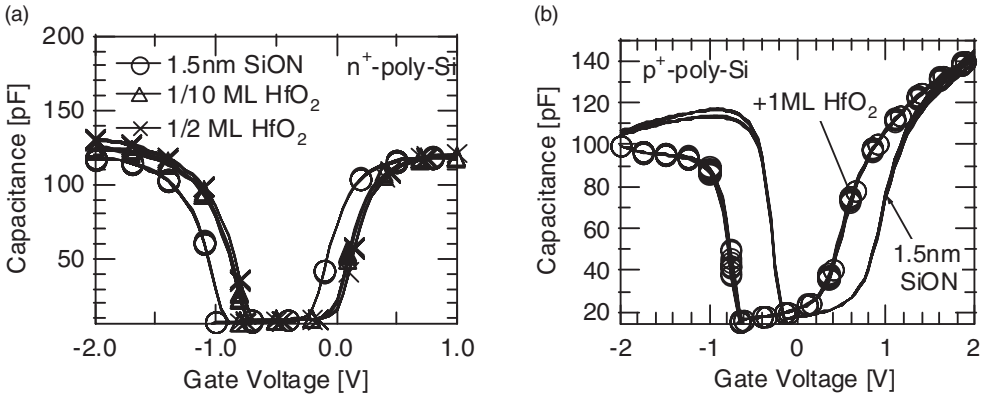


Figure 9.29 Split capacitance–voltage characteristics of $SiO_2/HfO_2/n^+$poly-Si devices, with different HfO_2 surface coverages. The deposition of 1 cycle (5 cycles) of HfO_2 on top of SiO_2 covers about 10% (50%) of the surface (island growth); (b) same as in (a) for $SiO_2/HfO_2/p^+$poly-Si devices [196, 203] (Reproduced with permission of AIP)

196]. More recently, it has been shown that a similar flatband voltage shift is observed for undoped poly-Si layer [196, 197] as well as fully silicided gates [197].

Conversely, it was argued that the V_{FB} and V_{th} shifts could be related to the presence of fixed charges in the high-k layer. In [198], the V_{th} shifts were mainly attributed to the penetration of dopants into the dielectric layer during the poly-Si activation process. The asymmetry of the V_{fb} shifts was then explained by the type of atoms used for the poly-Si doping (e.g., arsenic and boron for n^+ and p^+ gates, respectively). The larger V_{fb} shift was ascribed to preferential boron incorporation into the high-k film.

It is important to note that in both models the larger-than-expected poly-Si depletion measured in high-k samples can be readily explained taking into account the screening effect. The poly-Si carriers effectively screen any charge present into the high-k. Thus the poly-Si depletes more (thus a higher CET) due to this effect.

How can we distinguish whether the observed effects originate from charge incorporation into the dielectric layer or a change in the band alignment at the gate electrode side? This is not possible using only the capacitance–voltage (C–V) measurements as an experimental technique. Furthermore any C–V-based technique is an indirect measurement of the band alignment and any local change in barrier height is averaged out. Similarly to what has been done for the Schottky barrier height literature [199, 200], in the following paragraphs other techniques will be demonstrated to measure directly the band alignment at the gate/dielectric interface.

Internal photoemission

The internal photoemission (IPE) is a technique which allows one to measure directly the barrier height for electron and hole injection over Si/dielectric interfaces [201]. The ultraviolet radiation is used to excite electron–hole pairs in the poly-Si. Under negative gate bias (see inset in Figure 9.30), electron injection over the barrier can occur, provided the photon

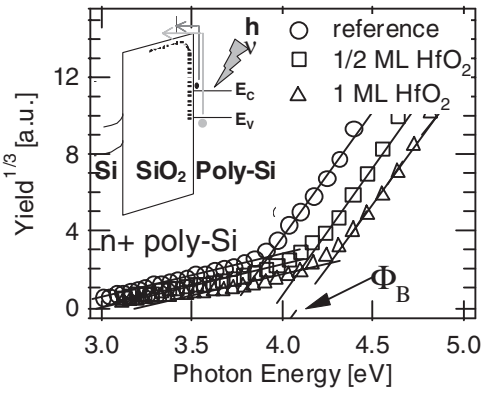


Figure 9.30 The cube root of the photon yield, $Y^{1/3}$, versus photon energy hν for the $SiO_2/HfO_2/n^+$poly-Si structure. The barrier height for electron injection from the Si valence band can be extracted from the linear extrapolation of the data. Inset: schematic energy band diagram of the structure under gate electron injection [196, 203] (Reproduced with permission of AIP)

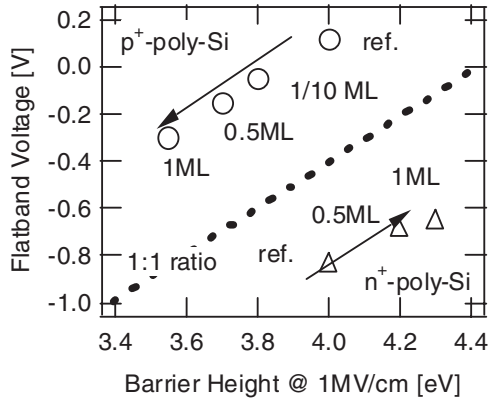


Figure 9.31 Flatband voltage of SiO_2/HfO_2/poly-Si structures, extracted from *C–V* characteristics, as a function of the HfO_2/poly-Si barrier height, extracted from IPE [196, 203] (Reproduced with permission of AIP)

energy is high enough. Using the model developed by Powell [202], the quantum yield *Y*, i.e., the ratio between the measured photoelectron current and the incident photon flux, is usually plotted in the $Y^{1/3}$–photon energy (hν) coordinates. The barrier height for electron injection from the Si valence band Φ_B can be extracted from the linear extrapolation of the $Y^{1/3}$–photon energy plot, as shown in Figure 9.30. It appears clearly that the presence of HfO_2 traces induces *an increase* in Φ_B by up to ~200 mV with n^+-poly Si gates. As the HfO_2 surface coverage increases, Φ_B increases for n^+-poly-Si gates and decreases for p^+-poly-Si gates, as shown in Figure 9.31. A one-to-one correlation between Φ_B change and V_{FB} shift is also clearly observed from this figure. A more detailed analysis [203] of the IPE results reveals the *discrete* nature of these charges located near or at the interface.

Measurement of the band alignment using valence band electron tunneling

The IPE is a rather straightforward technique to extract the band alignment together with the bandgap energy. However its usability is limited to rather thick stacks. (At low field the measured photocurrent close to threshold is in the order of few pA. If the dark current is very large, as in the case of thin leaky oxides, the experimental determination of the IPE yield is rather difficult.) For thin stacks another technique to determine the band alignment between the Si-substrate and the poly-Si gate is applicable to *n*MOSFET: the valence band electron tunneling [204] (VBET). The essential idea of the VBET is shown in Figure 9.32 and 9.33. Figure 9.32 shows the band diagram for the carrier separation in inversion. In Figure 9.33 the carrier separation in a reference SiON/poly-Si system is compared with the SiON/five cycles HfO_2/poly-Si (a system where we already know that the band alignment is different, see Figures 9.30 and 9.31). For a given gate bias, the gate current J_G is a quantity

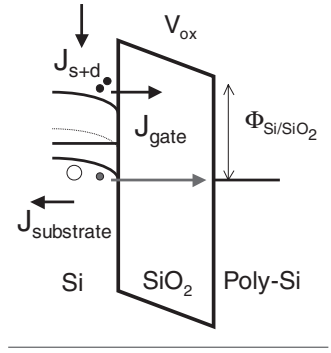


Figure 9.32 Band diagram for gate and substrate injection. Electron tunneling from the inversion layer can occur when the inversion layer forms. As soon as empty states are available at the gate side, VBET can occur. When defects at the gate/dielectric interface are present (i.e., higher effective *WF*, cf Figure 9.31), an earlier onset of VBET occurs (Reproduced with permission of AIP)

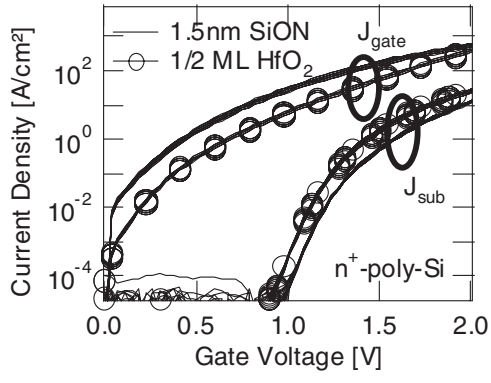


Figure 9.33 Carrier separation measurements of Si/SiON and Si/SiON/HfO_2 (5 cycles) devices with n^+-poly-Si gates, showing the contribution of the gate J_G and substrate J_{SUB} currents flowing through the gate stack [204] (Reproduced with permission of AIP)

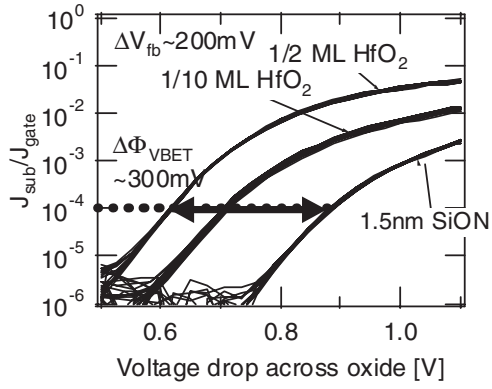


Figure 9.34 Ratio between the substrate and gate current (J_{SUB}/J_G) vs the voltage drop across the oxide V_{ox} of SiON and SiON/HfO_2 stacks. After 5 cycles HfO_2 deposition, the onset of valence band electron tunneling occurs ~300 mV earlier with respect to reference SiON [204] (Reproduced with permission of AIP)

proportional to the transmission (tunneling) probability as well as the inversion charge. One observes from Figure 9.33 that J_G of the SiON + half-monolayer HfO_2 stack is shifted to a more positive gate bias compared with the reference SiON layer, consistently with the increase in V_{FB}~200 mV observed from *C–V* measurements, cf Figure 9.31. An opposite trend is observed for the substrate current J_{SUB}, a quantity related to the tunneling of electrons from the Si substrate valence band to the poly-Si conduction band, so called valence band electron tunneling (VBET) [204, 205]. The onset of this current is observed when empty states in the poly-Si conduction band are available, and hence is related to the barrier height at the poly-Si gate side [204]: an earlier onset of VBET current should be observed when the barrier height at the poly-Si gate side is increased. This trend is indeed observed in Figure 9.33, when comparing a SiON reference layer with a SiON layer covered with five cycles of HfO_2.

The ratio J_{SUB}/J_G is plotted in Figure 9.34 as a function of the voltage drop across the gate oxide layer V_{ox}, for a SiON reference layer, and layers covered with 1/10 and ½-monolayer of HfO_2. The earlier onset of VBET is clearly observed in the layers partly covered with HfO_2, consistently with the increase of the n^+-poly-Si/HfO_2 barrier height observed from the IPE experiments (cf Figure 9.31). In addition, the shift of the VBET onset observed for the half-monolayer HfO_2 (~300 mV) quantitatively agrees with the 0.3 eV increase of the barrier height observed in Figure 9.31.

This approach can be demonstrated for SiON with metal gates and HfSiON/poly-Si, provided that the dominant leakage mechanism is by direct tunneling (see [205]).

9.3.3 Interface and bulk defect characterization

Most of the techniques available for classical SiO_2-based dielectrics to measure the interface states can, of course, be applied to high-*k* dielectrics. But due to some specific properties, some dedicated measurement methodologies have been introduced recently.

Early in the development of high-*k* gate stacks it was found that they suffer from a rather large DC hysteresis and threshold voltage instability effects [206]. Indeed, it was found

that, when combined with a poly-Si gate, the dielectric stack exhibits a defect band of bulk traps that can very efficiently trap electrons. This causes hysteresis in the *C–V* curves and transistor characteristics. Furthermore, the charge trapping also affects the extraction of important transistor parameters such as transconductance and threshold voltage. Various measurement methods to study these bulk defects and V_t instabilities have been proposed. The traps can be measured by pulsed *I–V* measurement or by charge pumping, as will be explained in the following subsections.

Pulsed *I–V* measurements

In order to study the details of the charging kinetics, fast voltage transients are mandatory. In these measurements the drain current I_D is recorded in the μs to ms time range [206, 207]. Several experimental techniques have been proposed to study these effects [208, 209]. In all these cases the MOSFET is connected as an amplifier and the input and ouput characteristics recorded as a function of time down to ns [209].

The I_D–V_G characteristics measured are presented in Figure 9.35. Note that the uptraces coincide because complete discharge has been reached at negative voltage. The open symbols show a 'quasi-DC' measured trace, illustrating how in this case the charge trapping is already occurring during the voltage ramp. The V_{th} shifts measured with fast pulses are significantly larger than with 'quasi-DC' techniques, as can be seen in the inset of Figure 9.35. This is caused by the large transient discharging during the down-trace for the case of DC, which does not occur for fast pulsing. In nonoptimized stacks, a hysteresis of more than 1 V under pulsed conditions can be observed! In a recent paper [209] it has been shown that the trapping during the uptrace becomes less and less efficient as the pulse width is reduced for the Hf-based stacks.

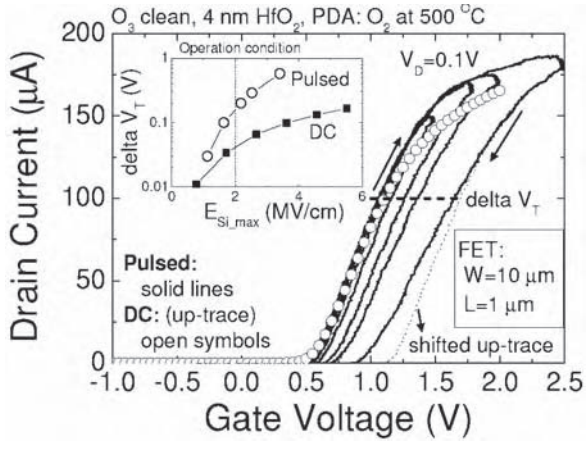


Figure 9.35 I_D–V_G traces measured a fast voltage ramp. The open symbols show an up-trace measured by conventional quasi DC technique. Significantly more threshold voltage shift is measured with a fast pulse technique, demonstrating the fast charge trapping in these layers. The inset shows the V_T shift as a function of the maximum Si field for both measurement techniques [206] (Reproduced with permission of IEEE)

Charge pumping

Charge pumping has been proven to be a suitable technique to measure the charge trapping in SiO_2/high-k stacks [210]. Different from measurements in SiO_2 layers, where the only interface states are sensed, charge pumping on high-k layers can also sense traps at the SiO_2/high-k interface or even inside the high-k. Conventional CP measurements [211], as explained in earlier sections, where the base level of the gate pulse is swept from accumulation to inversion (see Figure 9.36), provide poor control over the charge exchange. The use of the amplitude sweep, on the other hand, with a sufficiently negative gate bias results in complete detrapping throughout the entire sweep range. Electrons emitted from the high-k layer to the substrate will recombine with majority-carriers and contribute to the substrate current, such that the oxide charge can be measured. In SiO_2/HfO_2 stacks, as expected and consistent with the pulsed I_D–V_G results, the measured charge per cycle rapidly increases with gate bias and charging time, as shown in Figure 9.37.

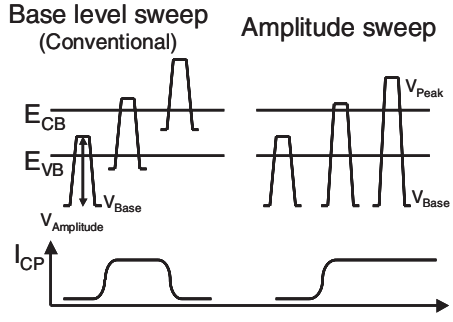


Figure 9.36 Schematic of charge pumping using the conventional base level and the amplitude sweep. Only an amplitude sweep with sufficiently negative base voltage guarantees complete discharging of the stack during the complete measurement (from [210])

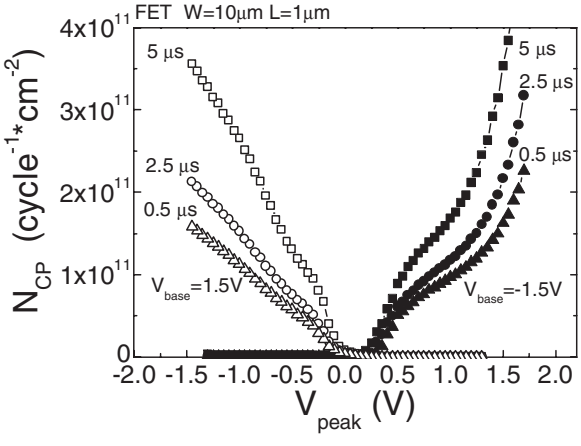


Figure 9.37 The pumped charge per cycle is plotted as a function of the gate pulse amplitude for a fixed pulse base level (solid symbols) or for fixed top level (open symbols). Different frequencies corresponding to different charging times are shown [210] (Reproduced with permission of IEEE)

If pulses with identical duty cycle (=0.5) are used, the charging time is inversely proportional to the frequency. By varying the CP frequency we can therefore sense different fractions of the trap density. At high frequency, corresponding to short charging time, only Si/SiO_2 interface traps and HfO_2 traps very close to the SiO_2/HfO_2 interface are pumped, but at lower frequency, corresponding to long charging time, traps deeper in the stack can also respond to the signal. Therefore, if the trap density sensed at high frequency is subtracted from the trap density measured at low frequency, a fraction of the bulk trap density only is obtained [212]. With this method, the generation of traps in the high-k can be monitored as a function of the stress time, and this analysis provides insight into the physical mechanisms of degradation of high-k stacks. Charge pumping is preferred over V_T-hysteresis because the change of the substrate current can be measured far more accurately than the increase of the hysteresis.

Note that CP does not measure the total trapped charge in the dielectric, but only the recombined charge in the substrate. Especially in short-channel devices a significant part of the charge is collected by the source and drain junctions of the transistor. If this effect is taken into account, good numerical agreement between pulsed I_D–V_G measurements and CP is obtained [213].

Quantitative models that relate the charge pumping parameters, frequency and amplitude, with the physical, parameters trap energy level and position in the stack, are still under development.

Defect band model

Most of the results presented in the following focus on polycrystalline HfO_2 deposited by ALD. Several other deposition techniques (MOCVD, PVD), chemical precursors, post-deposition annealing were also used for similar studies. Marginal differences were found between them, suggesting that the instability observed is a property of the dielectric considered rather than due to chemical impurities. A report by Gusev *et al.* [214] suggests that the use of the metal gate can alleviate some of these problems. Other high-k materials (i.e., HfSiON) seem more stable than pure HfO_2 [215].

The results for HfO_2 can be easily explained if we postulate the presence of a defect band located above the Si conduction band [216] (see the band diagram in Figure 9.38). The defects in this band can be very efficiently charged when a positive gate voltage V_G is applied. Electrons tunnel through the interface layer directly into the traps, or into the HfO_2 conduction band with subsequent trapping, as illustrated in Figure 9.38(c). The traps in the defect band are discharged at zero bias or, more efficiently, at negative gate bias, as illustrated in Figure 9.38(a). With this simple picture, one can readily understand most of the electrical instabilities observed in the capacitor and transistor characteristics, as will be demonstrated in the following paragraphs.

The interfacial SiO_2 layer strongly influences the charge trapping by controlling the electron injection (into the traps). The influence of the interfacial layer on the bulk trapping in HfO_2 can be decoupled using a 'thick' 9 nm SiO_2 layer [217, 218]. Detailed charge trapping studies were carried out, varying the injection condition and the lattice temperature, and it was concluded that only the electron fluence controls the trapping, while the detrapping is controlled by oxide electric field in combination with the lattice temperature.

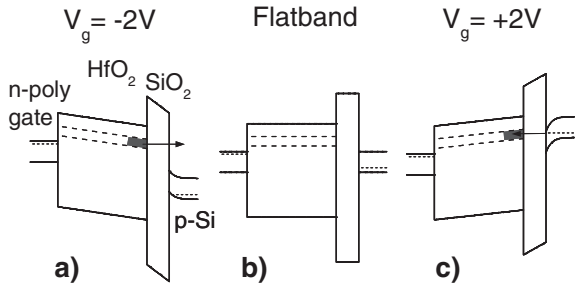


Figure 9.38 Schematic energy band diagram of a SiO_2/HfO_2/poly-Si gate stack containing a defect band in the HfO_2 layer at flatband condition (b), for negative (a), and for positive gate bias (c), the defects located near the SiO_2 interfacial layer move rapidly with respect to the Fermi level in the Si substrate [216] (Reproduced with permission of IEEE)

For a given amount of injected charge, N_{inj}, the apparent trapping probability

$$\overline{P(N_{inj})} = \bar{x}P(N_{inj}) \tag{24}$$

is proportional to the trapping probability P, and the charge centroid $\bar{x}$, as measured from the gate electrode. The apparent trapping probability, $\bar{P}$, is defined as

$$\overline{P(N_{inj})} = \Delta N_{tr}/\Delta N_{inj} \tag{25}$$

where ΔN_{tr} is the amount of trapped charge determined from the drain current decrease at stress condition (alternatively, the flatband voltage shift in a capacitor can also be used), and ΔN_{inj} is the amount of injected carriers determined from the gate leakage current.

The measured apparent trapping probability $\bar{P}$ is shown in Figure 9.39(a). Independent of the SiO_2 thickness, a large trapping probability, $\overline{P(N_{inj})} \simeq 0.3$ is measured for $N_{inj} < 10^{12}\,cm^{-2}$, and $\bar{P}$ decays with N_{inj}^{-1} at larger fluence. The fact that the value of $\bar{P}$ appears to be saturated at 0.2–0.3 can be explained by the charge location, $\bar{x}$, according to Equation (24). If we assume that the charge is located in the bulk of the HfO_2, a charge centroid of $\bar{x} \sim 0.3$ is estimated, suggesting that all the injected charge gets trapped initially, $P \simeq 1$, providing a simple explanation for the saturation of $\bar{P}$.

Furthermore, since $\bar{P}$ is independent of the gate voltage, the trapped charge can simply be calculated by integrating $\bar{P}$ over the injected charge. As expected, this approach works well, as illustrated by the examples in Figure 9.39(b), where the trapped charge measured by the pulse technique is compared for the two samples with different interfacial layer thickness as a function of the gate voltage and using a constant charging time of $\Delta t = 100\,\mu s$. The solid lines show the predicted trapped charge based on the trapping probability measured in thick films, as shown in Figure 9.39(b), and the estimated injected charge, $N_{inj} = \Delta t j$, where j is the measured gate current. The trapping probability is integrated over the injected charge at each voltage condition. Charge trapping can be reasonably well predicted by this simple empirical approach. The interfacial SiO_2 controls the supply of electrons that can flow to the gate, and thus the amount of charge trapped at each voltage condition.

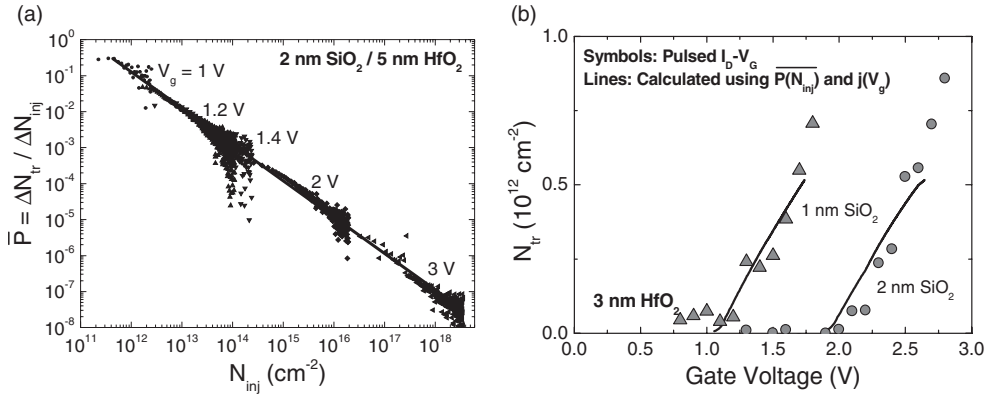


Figure 9.39 (a) Apparent trapping probability $\bar{P}$ as a function of electron fluence N_{inj} for several gate biases. Note that at low N_{inj}, $\overline{P(N_{inj})} \simeq 0.3$. If we assume that the charge is located in the bulk of the HfO_2, a charge centroid of $\bar{x} \sim 0.3$ is estimated, suggesting that all the injected charge gets trapped initially, in other words $P \simeq 1$ Reprinted from [217] Copyright (2003) with permission of Elsevier; (b) comparison of the measured trapped charge with the calculated trapped charge, using the apparent trapping probability of Figure 9.39(a) and gate current data, in a 3 nm HfO_2 layer with 1- and 2-nm-thick interfacial layers, respectively

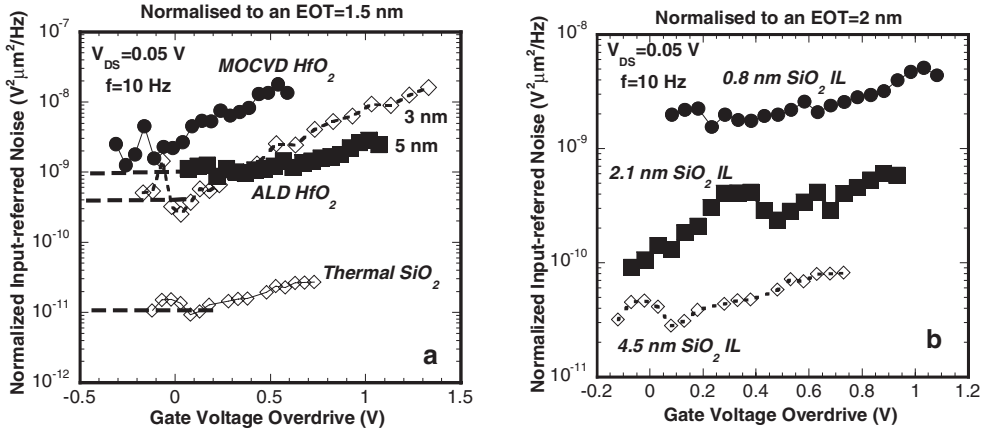


Figure 9.40 (a) Normalized input-referred voltage noise spectral density versus gate voltage overdrive for the two types of *n*MOSFETs with 1.5 (MOCVD) and 1.5 and 2 nm EOT HfO_2 (ALD) gate dielectric, compared with a standard thermal oxide reference device with an EOT of 5.5 nm. The noise has been normalized to an EOT of 1.5 nm; (b) normalized input-referred voltage noise spectral density versus gate voltage overdrive for ALD *n*MOSFETs with different interfacial layer thickness. Normalization has been done to an EOT of 2 nm. $f = 10$ Hz and $V_{DS} = 0.05$ V [227] (Reproduced by permission of ECS – The Electrochemical Society)

9.3.4 Noise characterization and modeling

As the low-frequency noise of a MOSFET is proportional with the gate oxide density, one may anticipate a strong impact of the high-*k* deposition technique on the noise magnitude, which is illustrated in Figure 9.40(a), comparing the input-referred spectral density at 10 Hz

for *n*MOSFETs with MOCVD and ALD HfO_2 gate dielectric. In this case, the MOCVD devices have the highest 1/*f* noise, suggesting a higher defectiveness of the film [219]. One can also derive from Figure 9.40(a) that the S_{VG} normalized for the device area, i.e., multiplied by *WL*, is significantly larger for the high-*k* transistors compared with an SiO_2 reference device. This has been consistently reported in the literature [219–229] and is directly related to the poor(er) quality of the deposited films. Employing Equation (15), with the appropriated tunneling parameter α_t reveals trap densities which are typically one decade higher than in SiO_2, i.e., in the range 10^{18}–$10^{19}\,cm^{-3}\,eV^{-1}$.

In the case of HfO_2 gate dielectrics, it has been shown that the 1/*f* noise increase can be well explained by a similar model that was developed for the corresponding V_T instability [230], assuming one or more energy bands of defects in the high-*k* layer, as explained in the previous section [221]. This was supported by the observation of resonance peaks in the $1/f^{\gamma}$ noise magnitude in function of the gate voltage [227]. It was furthermore demonstrated that the 1/*f* noise is correlated with other device parameters, like the low-field mobility [222, 228]: devices with high noise correspond to a low mobility and vice versa. This can be explained by considering the scattering through charged traps in the dielectric. The corresponding reduction in inverse low-field mobility can be expressed as $\Delta(1/\mu_0) = \beta q N_t \alpha_{sc}$ [228], with β a proportionality constant. It was also observed that the scattering coefficient of traps in HfO_2 is a factor of ~2 smaller than in SiO_2 [219, 221], which is thought to be related to the higher average dielectric constant of the Si–IL–HfO_2 stack [231].

Regarding the impact of EOT scaling on the 1/*f* noise, it has been demonstrated that not only the thickness of the high-*k* layer itself is of importance, but also the thickness of the interfacial layer [221]. This is illustrated in Figure 9.40(a) and (b). It has been found that the noise increases with HfO_2 layer thickness, for identical IL. This is correlated with a similar thickness dependence of the low-field mobility and flatband voltage [232], indicating an increasing N_t for thicker layers. This could be related to a transition from amorphous to polycrystalline structure when depositing thicker films [233]. The impact of the interfacial layer (IL) thickness can be understood by considering that the more defective high-*k* layer is brought closer to the interface with silicon, so that they can have a stronger impact on carrier trapping and scattering. It has been shown that for a thermal SiO_2 thickness of 4.5 nm, deposition of a 5 nm HfO_2 layer has marginal impact, opening perspectives for a dual-gate oxide approach [228]. However, other studies point out that in-diffusion of Hf may lead to an increase of the 1/*f* noise spectral density in an underlying thermal SiO_2 [223].

At the moment, HfO_2 and related high-*k* materials ($Hf_xSi_{1-x}O$, silicates and HfSiON) are the leading high-*k* materials for 45 nm and below CMOS development. Given the difference in trap density and noise between pure HfO_2 and SiO_2, one would expect some impact of the fraction *x* of Hf on the properties of silicates. A strong, one decade increase in noise for $x = 50\%$ compared with 0 or 30% has been reported [225]. However, the results of Figure 9.41 show a very smooth dependence on *x* for the 1/*f* noise in TaN metal gate *n*MOSFETs, with MOCVD HfSiON gate dielectric. A similar conclusion was reached for poly-Si/HfSiON gate stacks [229]. It should also be noted that the normalized noise in Figure 9.41, for an area of $1\,\mu m^2$ and $f = 1$ Hz is significantly above the noise specification for the 45 nm analog node put forward by the ITRS roadmap [234].

Figure 9.41 illustrates another important factor in the scaling/implementation of high-*k* gate dielectrics in connection with metal gates. Similar to the case of thin SiO_2, shown in Figure 9.17(a), the noise is sensitive to the details of the metal gate processing. In the case of Figure 9.41, PVD TaN results in a lower 1/*f* noise spectral density than ALD TaN. The

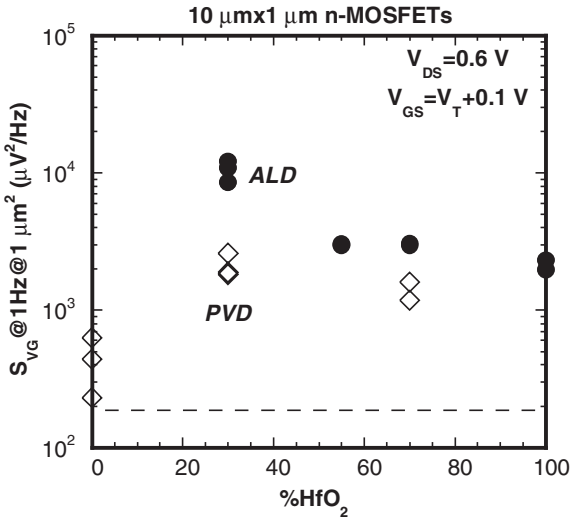


Figure 9.41 Summary of the input-referred noise at $f = 1\,\text{Hz}$ and $A = 1\,\mu\text{m}^2$ for the wafers with ALD and PVD TaN. The dashed line indicates the $200\,\mu\text{V}^2/\text{Hz}$ spec at 1 Hz and $1\,\mu\text{m}^2$. $V_{DS} = 0.6\,\text{V}$ and $V_{GS} = V_T + 0.1\,\text{V}$. Different data points correspond to different devices on the wafer

most probable reason is that ALD TaN gives rise to a nitrogen-rich gate material. Penetration of the nitrogen into the high-k layer may result in a higher trap density and, hence, in more noise.

A further illustration of the importance of the gate–dielectric interface on the noise performance is illustrated in Figure 9.42, corresponding to the trap density profiles derived from the $1/f^{\gamma}$ spectra, based on Equations (14, 15) and obtained on two identical devices, except for the deposition of two monolayers of HfO_2 (=20 ALD cycles). The presence of these monolayers drastically increases the $1/f$ noise, which is believed to originate from an increase in the trap density, close to the polysilicon gate-SiON interface. As such, it could be a direct evidence of the so-called Fermi level pinning mechanism [235], which relies on the formation of Hf-Si bonds at the gate interface. As a result, a high density of trap states are formed, which pin the Fermi level and shift the flatband voltage of the poly-gate transistors. According to the profiles of Figure 9.42, the trap density is enhanced not only near the gate electrode, but also deeper in the SiON layer, probably due to in-diffusion of Hf.

9.3.5 Time-dependent dielectric breakdown

All experimental evidence reported in literature so far indicates that the physical degradation mechanisms in high-k stacks are very similar to the ones in SiO_2. The major complication comes from the asymmetry in the dielectric that results in a strong polarity dependence of degradation and breakdown characteristics as shown in Figure 9.43 [212]. With positive stress voltage, the trap density at the SiO_2/substrate interface is hardly affected, but the trap density in the bulk of the HfO_2 rises. For negative stress voltage, the opposite is observed.

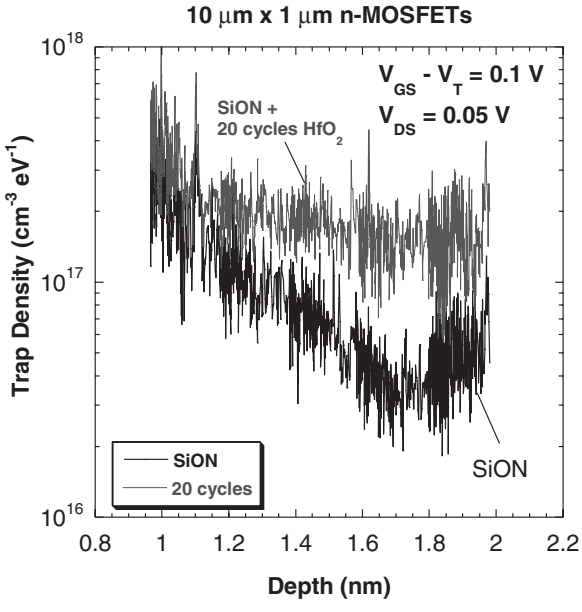


Figure 9.42 Qualitative trap density profiles derived from a $V_{GS} - V_T = 0.1$ V spectrum, for two $10 \times 1\,\mu$m *n*MOSFETs with 1.5 nm SiON gate dielectric and polysilicon gate. One transistor received 20 cycles of HfO_2, resulting in a higher effective trap density close to the gate-dielectric interface

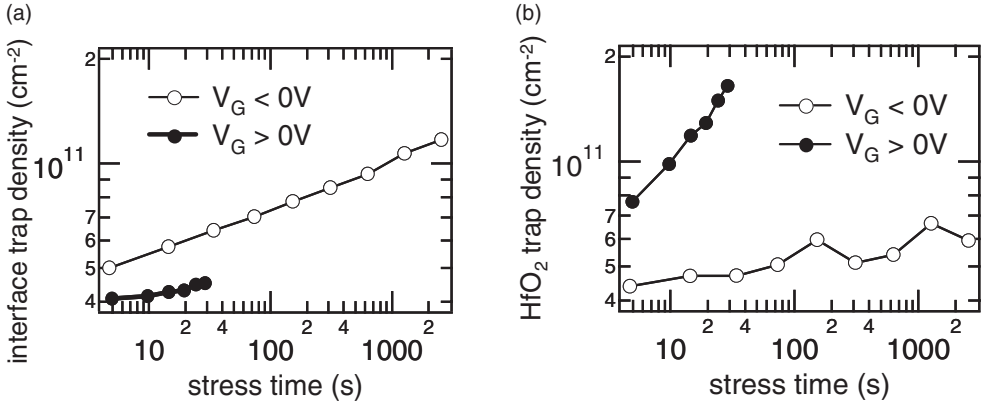


Figure 9.43 The increase of the bulk HfO_2 trap density (a), extracted from the difference of a high- and low-frequency CP current, and the Si/SiO2 interface trap density (b), extracted from high-frequency CP, vs time during positive and negative gate voltage stress. Breakdown occurs after 30 s for $V_G > 0$ V, while it does not occur even after 2500 s for $V_G < 0$ V. For $V_G > 0$ V, the N_{it} increase is very small and substantially lower than what can be generated for $V_G < 0$ V. For the bulk HfO_2 trap density the opposite trend is recorded. Note that the bulk HfO_2 trap density is only a fraction of the total trap density in the HfO_2. With different CP conditions, in particular higher pulse amplitude or lower frequency, more traps can be sensed [212] (Reproduced with permission of IEEE)

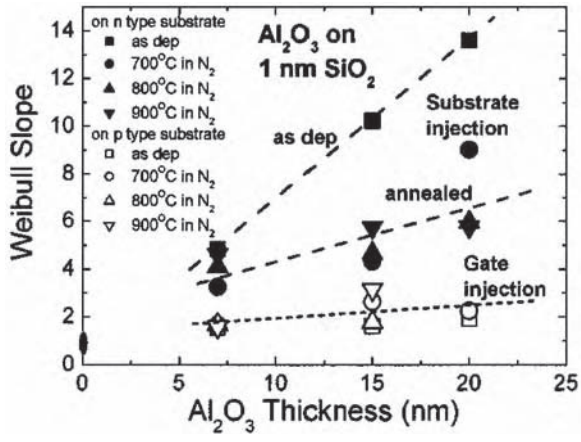


Figure 9.44 Weibull slope vs Al_2O_3 thickness in an SiO_2/Al_2O_3 stack with interface layer thickness 1.5 nm. For gate injection a shallow slope is obtained irrespective of Al_2O_3 thickness and annealing condition. For substrate injection the Weibull slope increases with the Al_2O_3 thickness, but the effect is reduced in annealed samples compared with as-deposited layers [236] (Reproduced with permission of IEEE)

The data in Figure 9.43 have been obtained with charge pumping, but the large interface trap generation with negative gate polarity has been confirmed also on SiO_2/Al_2O_3 by *C–V* measurements [236] and is related to the high energy of the electrons entering the substrate [149].

Because the creation of traps in a SiO_2/high-*k* stack is polarity dependent, we also expect this dependence to be reflected in the dielectric time-to-breakdown. In some stacks this is obvious from the statistical properties of the Weibull time-to-breakdown distribution. On SiO_2/Al_2O_3 stacks with different Al_2O_3 thickness for example, polarity-dependent Weibull slopes are observed, as shown in Figure 9.44 [236]. For negative gate stress, a low Weibull slope is observed, independent of the high-*k* thickness [237], while for positive gate stress the Weibull slope increases with high-*k* thickness and can be as high as 13 for a 20 nm layer.

A low Weibull slope independent of the high-*k* thickness suggests that the interface layer controls the breakdown of the entire stack and this picture is consistent with the high interface trap creation in Figure 9.43. The degradation of the interfacial layer can trigger the breakdown of the complete stack. On the other hand, an increasing Weibull slope with high-*k* thickness suggests that the high-*k* layer is controling the dielectric breakdown and the Weibull slope simply reflects the number of traps needed to construct the breakdown path through the high-*k* layer as predicted by the percolation model [129].

Using the properties of the t_{BD} distribution in this way is, however, an indirect approach. A low Weibull slope could also be explained in other ways, for example by extrinsic breakdown in process-induced weak spots or along grain boundaries. A more direct evidence for interface-layer-controlled breakdown in the case of negative stress polarity is obtained by plotting the time-to-breakdown vs electron energy at the anode for a sample set with a variety of thickness combinations, as shown in Figure 9.45 [237]. These data, taken on SiO_2/ZrO_2 stacks, can be grouped in three sets, corresponding to three interface layer

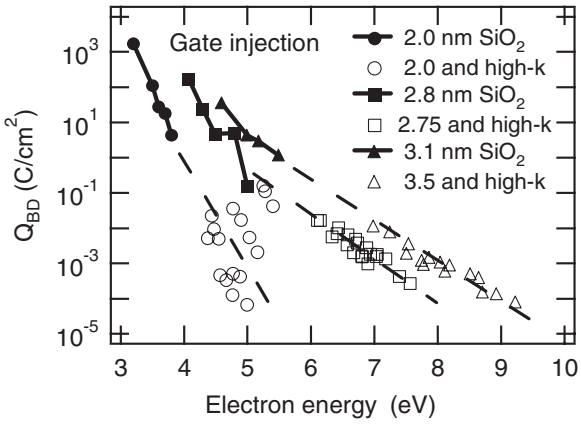


Figure 9.45 Q_{BD} for gate injection vs electron energy at the anode for a set of SiO_2/ZrO_2 stacks with three SiO_2 thicknesses (2, 2.75 and 3.5 nm) and four ZrO_2 thicknesses (8, 12, 16 and 20 nm). Data on pure SiO_2 have been added for comparison. For similar interfacial layer thickness, the data line up very well, confirming that the interfacial SiO_2 determines the breakdown of the whole gate stack. The electron energy was calculated assuming full energy relaxation in the high-*k* and direct tunneling through SiO_2 [237] (Reproduced with permission of IEEE)

thicknesses, and no dependence on the high-*k* layer thickness is noticed. The result of Figure 9.45 is, however, obtained on very thick stacks and it is not guaranteed that at low voltage in scaled stacks interface-controlled breakdown still occurs.

For positive stress polarity, the situation is quite different. In SiO_2/HfO_2 stacks, it has been shown that, independent of the stress condition, the breakdown for positive gate voltage occurs when the HfO_2 trap density reaches a critical value [212]. This was also observed in pure SiO_2 layers and it suggests that the HfO_2 layer controls the breakdown of the entire stack and that percolation theory can be applied. Furthermore, the stress-induced leakage current (SILC) increases linearly with the generated HfO_2 defects [238], similar as in pure SiO_2 layers [239].

In sub-nanometer EOT layers stressed at low voltage, the concepts of soft breakdown and progressive wear-out are also maintained [240]. With a metal gate, the analog breakdown cannot be resolved and instead, hard breakdown is observed [241, 242]. This suggests that the current increase during the analog breakdown depends on resistance of the gate and in low-resistive metal gates it is so fast that the breakdown appears again as hard breakdown, even at low stress voltage.

The digital soft breakdown still remains and needs to be taken into consideration in order to correctly predict the lifetime of the high-*k* stack at low voltage. Especially at low gate voltage, multiple soft breakdowns can be observed before hard breakdown, resulting in a large current increase as illustrated in Figure 9.46. The current increase partly eliminates the advantage of the leakage current reduction that was achieved when replacing SiO_2 by high-*k* and might be a reliability issue as such. This leakage current increase may be an even more limiting reliability issue than the hard breakdown and therefore both effects need to be considered by circuit designers.

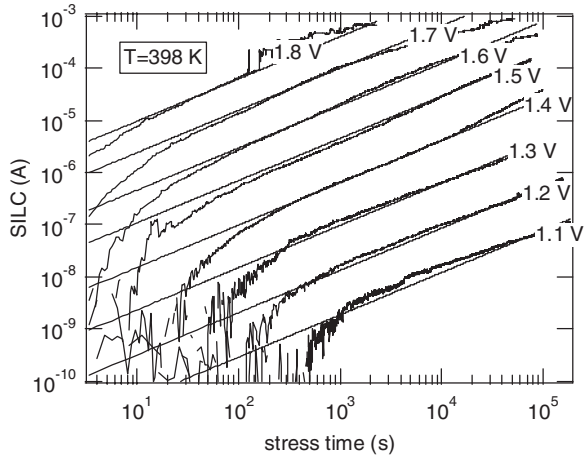


Figure 9.46 The leakage current increase in a 0.9 nm EOT SiO_2/HfO_2 stack is caused by multiple soft breakdowns. The leakage current increase can eliminate a considerable part of the leakage current decrease that was achieved when replacing SiON by a high-k stack of the same EOT [240] (Reproduced with permission of IEEE)

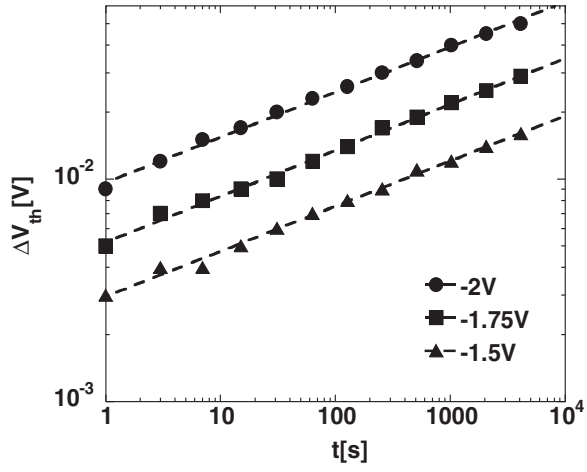


Figure 9.47 V_{th} shift as a function of time of a SiO_x/HfSiON/TaN gate stack, stressed under NBT stress at 125°C at different gate biases. Dashed lines are power-law fits to the data

9.3.6 Negative-bias temperature instability

As in SiO_2- and SiON-based devices, shifts in the threshold voltage of high-*k*-based transistors are observed during negative bias temperature stress, and it has been recently reported that NBTI could be a potential reliability issue in these devices [243–248].

The V_{th} shift of a SiO_x/HfSiON/TaN *p*MOSFET is shown in Figure 9.47 as a function of (stress) time [249]. The characteristic power-law time dependence of ΔV_{th} is clearly observed, with a power-law time exponent ~0.2.

The contribution of interface states N_{it} to the V_{th} shift was estimated from charge pumping measurements at 3 MHz, as shown in Figure 9.48(a); at such a high frequency,

only the fast states located at the Si/dielectric interface are supposed to respond when the device is switched between accumulation and inversion. The fraction of fast states to the total effective density of defects, $N_{\text{eff}} = (\Delta V_{\text{th}} C_{\text{ox}})/q$, is shown in Figure 9.48(b) as a function of the stress voltage [250]. The contribution of N_{it} ranges between about 40 and 20%, depending on the gate bias. Consequently, a substantial fraction of the V_{th} shift can be attributed to the generation of slow states N_{ot}, which are most likely bulk defects located in the SiO_x/HfSiON gate stack [250, 251].

The typical time and temperature dependences of the fast and slow state generation during the NBT stress are shown in Figure 9.49. The fast state density increases with time

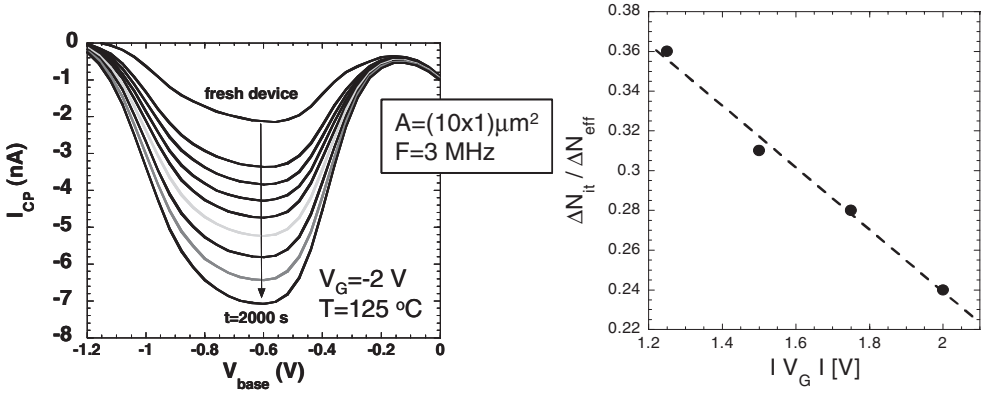


Figure 9.48 (a) Charge pumping current vs basal level of SiO_x/HfSiON/TaN pMOSFETs, recorded periodically during NBT stress at −2 V and 125°C; (b) ratio between fast interface states and total effective density of defects as a function of stress voltage (Reprinted from [250] Copyright (2005) with permission from Elsevier)

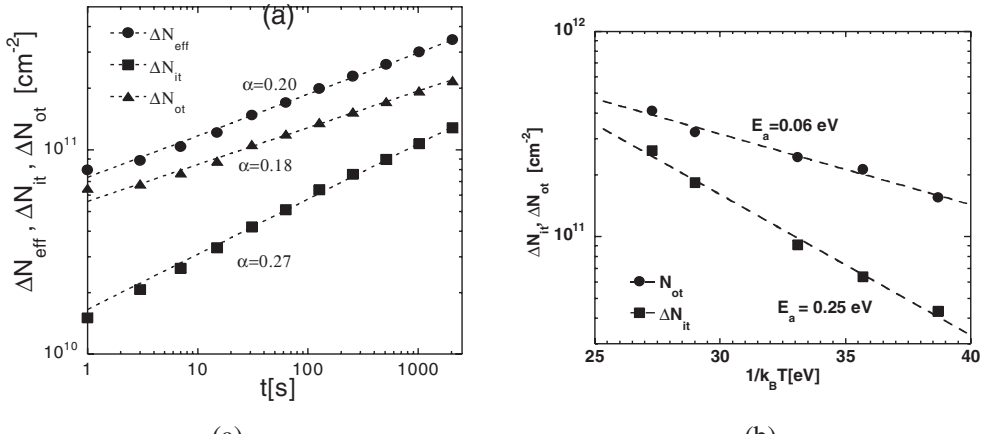


Figure 9.49 (a) Time dependence (Reprinted from [250] Copyright (2005) with permission from Elsevier); (b) inverse temperature dependence of the fast and slow interface states generated during NBT stress of a SiO_x/HfSiON/TaN gate stack

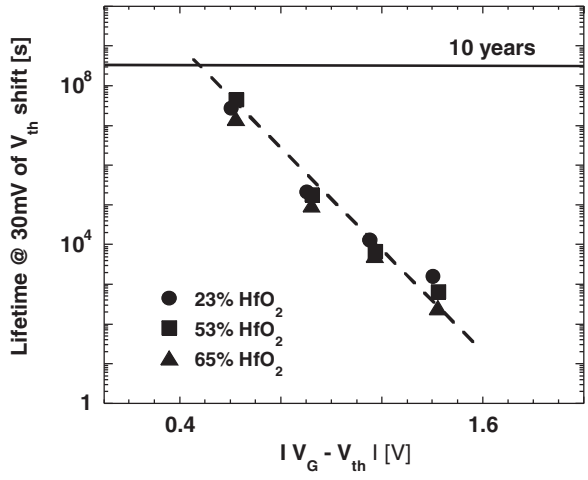


Figure 9.50 Extrapolated lifetime of SiO_x/HfSiON/TaN-based *p*MOSFETs as a function of gate overdrive, for gate stacks with different Hf content. Temperature was fixed at 125°C

like a power-law with an exponent ~0.25 and are thermally activated, with an apparent activation energy of about 0.25 eV. This time and temperature dependence is typical for the generation of P_{b0} centers, as predicted by the reaction-diffusion model (cf discussion of NBTI). On the other hand, the slow state density generation rate is characterized by a reduced power-law time exponent ($\alpha \sim 0.16$–0.18) and is almost independent of temperature. This suggests that the mechanism of slow state generation is most likely different from the fast interface states. A possible explanation for the slow state generation is the trapping of holes injected from the Si substrate inversion layer during the electrical stress, resulting in the generation of positively charged defects in the gate dielectric stack [251].

Finally, the extrapolated lifetime of HfSiON/TaN-based MOSFETs is shown in Figure 9.50 as a function of the gate overdrive, for devices with different Hf content [251]. The extrapolated gate overdrive, corresponding to 10 yr lifetime, is found to be about 0.4 V, irrespective of the Hf content. NBTI thus appears as a potential severe reliability issue in these devices.

9.4 CONCLUSIONS

In this chapter we have discussed the problems that occur in the electrical characterization of ultra-thin gate dielectrics when the conventional oxide thicknesses are scaled down to their ultimate limits on the one hand, and on the other hand when, in order to cope with this problem, high-*k* dielectrics are introduced in the gate stack. In the first part of the chapter, the impact of scaling of SiO_2-based gate dielectrics on the electrical characterization was discussed, covering the mechanisms of gate leakage currents, the measurement of *C*–*V* and of charge pumping characteristics under high gate leakage currents, noise measurement and models for scaled oxide thicknesses, and finally reliability measurements such as time-dependent dielectric breakdown (TDDB) and negative-bias temperature instability

(NBTI). It was shown that in each of these cases, the scaling of the oxide thickness has a tremendous impact on the conventional characterization of the gate dielectrics, and a lot of research has been done in the last few years to cope with this problem. The results of this research have been summarized in this part of the chapter.

In the second part, the electrical characterization of high-k dielectrics is discussed, covering the definition of effective oxide thickness (EOT) and capacitive effective thickness (CET), the extraction and importance of gate workfunction, the impact of defects in the high-k dielectrics on the V_t instability of the MOSFETs and techniques to measure these defects under dynamic conditions, and again noise, TDDB and NBT characterization and models for high-k gate dielectrics. Again it is demonstrated that the introduction of high-k gate materials has important consequences on the electrical characterization of the high-k gate stacks. The knowledge from conventional oxides cannot always simply be extrapolated, but the specific properties, such as the presence of the interfacial layer and the properties of the metal gate, have to be taken into account.

This chapter has aimed to give the reader an overview of the recent findings and the new insights in the electrical characterization of such advanced gate dielectrics.

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10 Integration Issues of High-*k* Gate Dielectrics

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10.1 INTRODUCTION

In order to improve the electrical performance of CMOS devices, scaling the MOSFET dimensions is essential. The scaling of MOSFET requires not only the miniaturization of gate length, but also scaling of the *p*/*n* junction depth in the source and drain region, gate dielectric thickness, and sidewall thickness. From a requirement of performance improvement for MOSFET at a rate of more than 15%/year, the MOSFET dimensions have been aggressively scaled since the mid-1990s. As a result, the gate dielectric thickness will approach 1 nm for most scaled devices in the near future. At these thicknesses, conventional gate dielectric materials such as SiO_2 or SiON exhibit severe gate leakage current problems via direct tunneling phenomena. This leakage current is not tolerable, especially for chips for low power applications. The ratio of gate leakage current to total leakage current within a chip increases and power dissipation by gate leakage current is no longer negligible.

Therefore, the implementation of an alternative gate dielectric material with high dielectric constant (high-*k*) is required. By using high-*k* material, the equivalent oxide

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thickness (EOT) is decreased, due to its higher dielectric constant than the conventional SiO_2 gate dielectric, while the leakage current is greatly reduced due to its greater physical thickness. In general, the gate leakage current for high-*k* gate dielectrics decreases by three to four orders of magnitude compared with a conventional SiO_2 gate dielectric with same EOT.

When one integrates high-*k* gate dielectrics into conventional planar CMOS, one has to consider several technological issues. The main issues are as follows; details of each issue will be described in the following sections.

1. Thermal stability of high-*k* gate stack. In a conventional CMOS fabrication process, the dopants introduced into the source and drain region must be electrically activated in order to lower the parasitic resistance. Therefore, high-temperature activation annealing at more than 1000°C is performed after the gate stack fabrication; thus, thermal stability of the high-*k* film is one of the key issues. Crystallization or phase separation may occur for some high-*k* materials. Such phenomena result in inhomogeneity of the high-*k* film, and may increase leakage current through grain boundaries. It is much preferred to retain the amorphous phase after high-temperature annealing, if possible.

2. Interfacial characteristics with silicon substrate. Maintaining good electrical characteristics while reducing EOT is an essential issue for the use of high-*k* gate dielectrics. The high-*k* gate dielectric stack usually consists of bilayers; the high-*k* dielectric film, and the interfacial SiO_2/SiON layer. The interfacial layer between high-*k* gate dielectrics and silicon substrate plays a vital role in avoiding degradation of carrier mobility (this is directly related to the current drivability of MOSFET) and reliability (breakdown and threshold voltage shift). There is often a tradeoff relationship between interfacial layer thickness and electrical characteristics. Therefore, careful attention must be paid to the thickness of the interfacial layer.

3. Gate material selection: Poly-Si gate vs metal gate. The threshold voltage controllability of conventional poly-Si gated MOSFETs is closely related to Fermi level pinning phenomena. Especially for PMOS transistors with poly-Si gate, the threshold voltage is fixed at a relatively high value due to Fermi level pinning, creating a serious problem for practical application. Some methods of modifying the poly-Si gate/high-*k* gate interface have been proposed, but they are not fully effective. In order to eliminate Fermi level pinning effects, the introduction of metal gates with appropriate workfunctions is required. Metal gate technology will also be effective in eliminating gate depletion effects, and boron penetration observed with conventional poly-Si gate MOSFETs.

Regarding high-*k* material selection, many materials have been proposed so far, such as Ta_2O_5, Al_2O_3, ZrO_2, HfO_2, HfSiO, HfAlO, HfSiON, and HfAlON. Among these materials, Hf-based materials have been regarded as the most promising candidates for CMOS device application [1–4]. This is mainly due to their high thermal stability during the CMOS fabrication process, especially when silicon and/or nitrogen are incorporated into the HfO_2. Good electrical characteristics, such as high carrier mobility and high drain current, have thus far been obtained. Therefore, discussion here will focus on HfSiO and HfSiON high-*k* materials.

10.2 THERMAL STABILITY IMPROVEMENT BY NITROGEN INCORPORATION

Nitrogen incorporation into HfSiO is effective in increasing its thermal stability. Figure 10.1 shows X-ray diffraction analysis results for HfSiON films with different nitrogen contents, after 1000°C annealing [3]. By increasing the nitrogen content, the crystalline HfO_2 peak disappears, and the film's amorphous structure is retained. TEM microphotographs with and without nitridation of HfSiO are shown in Figure 10.2 [4]. It is clearly observed that crystallization and phase separation were observed without nitridation. The amorphous

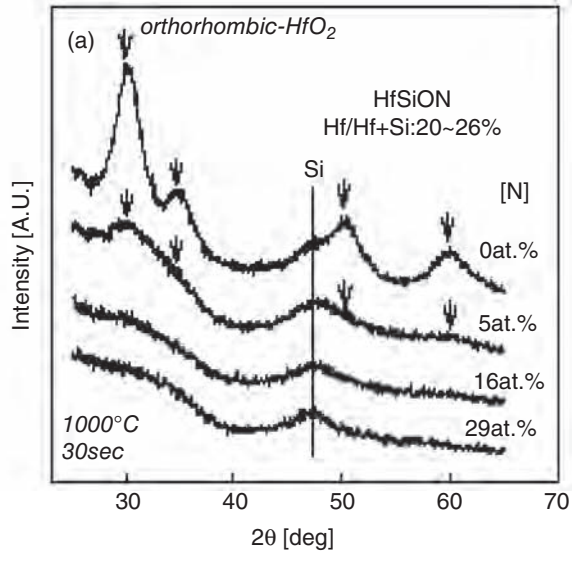

Figure 10.1 X-ray diffraction analysis of nitrided HfSiO films [3]. (Copyright (2002) IEEE)

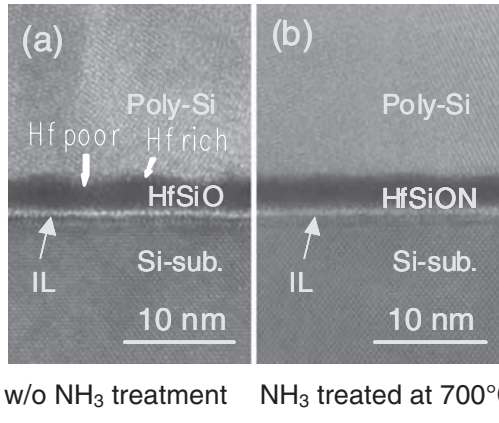

Figure 10.2 TEM microphotographs with and without nitridation of HfSiO [4]. (Reproduced by permission of the Japan Society of Applied Physics)

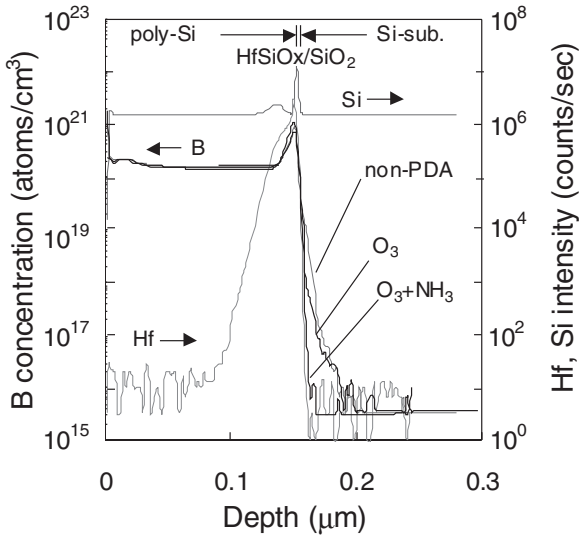

Figure 10.3 SIMS profile of B, Hf, and Si in HfSiON film after 1050°C annealing [4]. (Reproduced by permission of the Japan Society of Applied Physics)

structure of the as-deposited HfSiO film was retained after nitridation, demonstrating high thermal stability. During the nitridation, a substitution reaction from Si–O to Si–N bonds may occur [5]. Thus, the suppression of crystallization by nitrogen incorporation may be due to the formation of a thermally stable Si–N network in the HfSiON film.

Another benefit of nitrogen incorporation is the suppression of boron penetration from poly-Si gate in PMOSFETs. Boron penetration brings about threshold voltage fluctuations. Figure 10.3 show the backside SIMS profile of B, Hf and Si after 1050°C annealing [4]. Both an O_3 post-deposition anneal (PDA) and NH_3 nitridation were performed. After that, boron penetration was negligibly small compared with the case of no treatment, or only the O_3 anneal.

10.3 INTERFACIAL CHARACTERISTICS BETWEEN HIGH-*k* AND SILICON SUBSTRATE

The fabrication process of the thin interfacial layer and its quality are very important issues for achieving good electrical characteristics. A typical high-*k* gate dielectric stack is a bilayer, consisting of the high-*k* film and the interfacial layer, as shown in Figure 10.4. Possible factors affecting carrier scattering and therefore mobility are shown in Figure 10.5 [6]. Among them are charge, phonon scattering and roughness in both the interfacial layer and high-*k* layer, and also the interfaces between the high-*k* and poly-Si electrode layers. Because the effect of charge and phonon scattering in high-*k* films is dominant in many cases, and carrier mobility in channel region depends on the distance from the scattering source in high-*k* film, there is a tradeoff relationship between the interfacial layer thickness and carrier mobility [7]. This tradeoff relationship makes EOT reduction difficult, when trying to maintain a high carrier mobility.

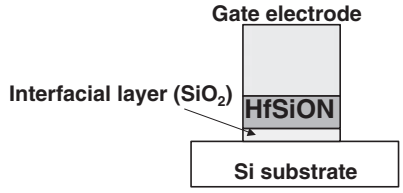

Figure 10.4 Typical high-*k* (HfSiON) gate stack structure which consists of HfSiON and interfacial layers

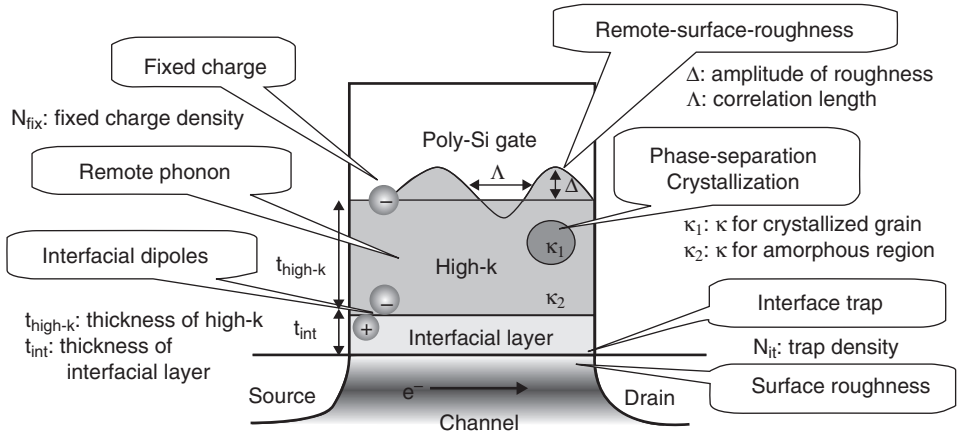

Figure 10.5 Possible carrier scattering factors in a high-*k* gate stack that affect mobility [6]. (Copyright (2003) IEEE)

The nitrogen profile in the interfacial layer also affects the electrical characteristics of high-*k* MOSFETs [8]. Nitrogen is introduced into the interfacial layer through the HfSiO nitridation.

In a SiON interfacial layer, nitrogen profile control is critical for achieving high-performance CMOS. Figures 10.6 and 10.7 show two different interfacial layer nitrogen profiles [9]. The first (Figure 10.6) is formed by N_2O re-oxidation of a SiN layer, and the second (Figure 10.7) is formed by NO re-oxidation of a SiN layer. It is noted that the nitrogen profile, especially at the interface between SiON and the Si substrate, are different. The nitrogen concentration at the interface is lower for the NO re-oxidation method. These differences clearly affect the electrical characteristics, as shown in Figure 10.8, in which the electron mobility dependence on electric field for HfAlO/SiON high-*k* dielectric stacks is compared. As can be seen in these figures, the carrier mobility has a clear dependence on interfacial layer nitrogen profiles. In Figure 10.9, electron mobility, EOT, and MOSFET on-current I_{on} are shown for different interfacial thicknesses [10]. It can be clearly seen that the electron mobility is higher for thicker interfacial layers. Thus a higher I_{on} will be obtained for thicker interfacial layers, showing the tradeoff between EOT reduction and carrier mobility. Therefore, it is necessary to carefully design the interfacial layer fabrication process by considering the balance between desired EOT and electrical characteristics.

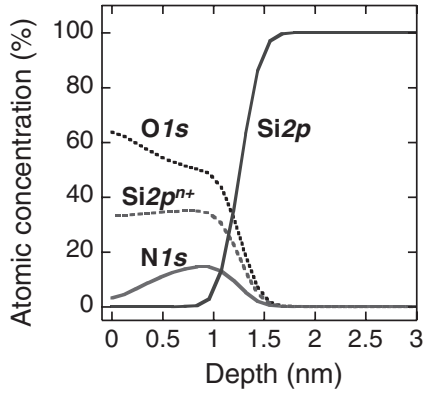

Figure 10.6 Atomic concentration of SiON interfacial layer formed by N_2O re-oxidation of SiN layer [9]. (Reproduced by permission of the Japan Society of Applied Physics)

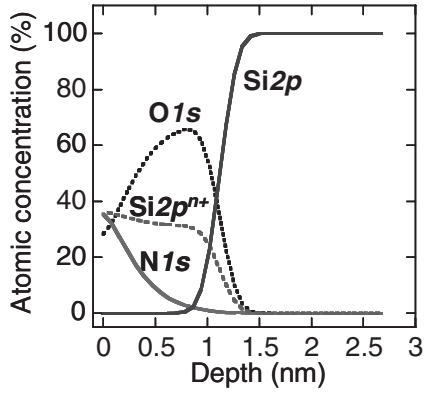

Figure 10.7 Atomic concentration of SiON interfacial layer formed by NO re-oxidation of SiN layer [9]. (Reproduced by permission of the Japan Society of Applied Physics)

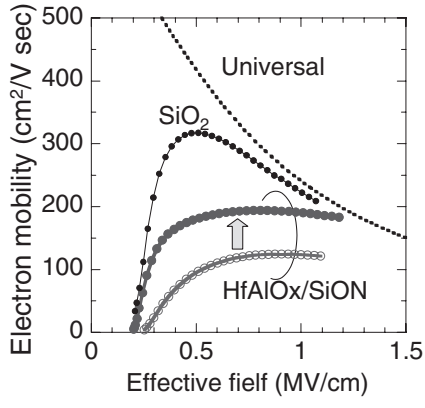

Figure 10.8 Difference in electron mobility for different nitrogen profile SiON interfacial layers for HfAlO/SiON gate stack [9]. (Reproduced by permission of the Japan Society of Applied Physics)

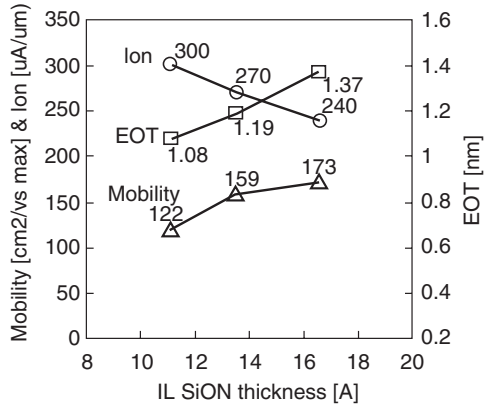

Figure 10.9 Electron mobility, EOT, and on-current of MOSFET I_{on} as a function of interfacial layer thickness [10]. (Reproduced by permission of the Japan Society of Applied Physics)

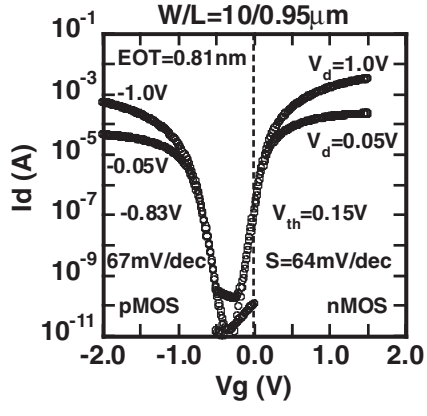

Figure 10.10 Drain current I_d vs gate voltage V_g characteristics of HfSiON MOSFETs with poly-Si gate [12]. (Reproduced by permission of Japanese Journal of Applied Physics)

10.4 GATE MATERIAL SELECTION: POLY-Si GATE VS METAL GATE

Threshold voltage controllability of poly-Si-gated high-*k* MOSFETs is limited by Fermi level pinning effects [11]. Figure 10.10 shows drain current I_d vs gate voltage V_g characteristics of HfSiON MOSFETs with a poly-Si gate [12]. The threshold voltage V_{th} of *p*MOSFET is larger than that of *n*MOSFET, due to Fermi level pinning. There are two possible models for Fermi level pinning. One is dipole formation at the poly-Si/high-*k* interface due to Hf–Si bond creation [11]. Due to the interface dipole, the Fermi level position is pinned just below the poly-Si conduction band edge,as shown in Figure 10.11. Another possible model is based on the formation of oxygen vacancies in Hf-based high-*k* dielectrics, with subsequent electron transfer to the poly-Si gate, schematically illustrated in Figure 10.12 [13].

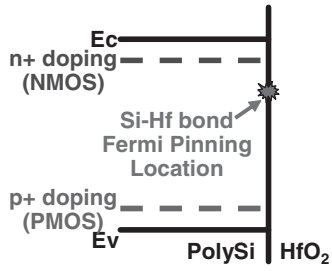

Figure 10.11 Fermi level pinning position due to Hf–Si bond creation at poly-Si gate electrode and Hf-based high-*k* film [11]. (Reproduced by permission of the Japan Society of Applied Physics)

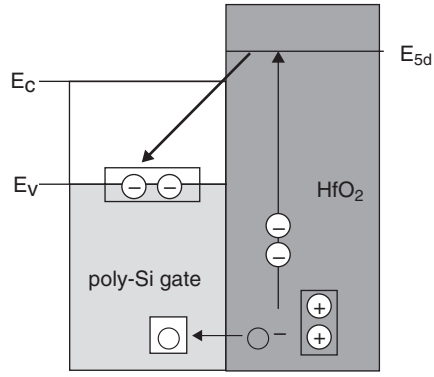

Figure 10.12 Model for Fermi level pinning by oxygen vacancies in Hf-based high-*k* dielectrics, and subsequent electron transfer into poly-Si gate [13]. (Copyright (2004) IEEE)

In spite of the fact that Fermi level pinning is believed to be fundamental to the poly-Si/metal oxide interface, and results in V_{th} shifts, some effort has been undertaken to improve V_{th} controllability. One approach is to modify the poly-Si/high-*k* interface by capping the top surface of the high-*k* layer [14–16]. Figure 10.13 shows the structure of a SiN-capped HfSiON gate stack. The SiN layer was deposited by cyclic CVD, and the resultant EOT increase was 0.2 nm. By using SiN capping, Fermi level pinning is partially relaxed, as shown in Figure 10.14. The flatband voltage V_{fb} difference between *p*-type and *n*-type poly-Si gate was increased by the SiN/HfSiON structure. However, the V_{fb} difference is still small compared with the poly-Si/SiO_2 structure, and SiN capping alone is not effective in eliminating the Fermi level pinning. Capping, in addition to counter-doping into the channel region, has been confirmed effective in reducing the V_{th} in poly-Si gate HfSiON MOSFETs, as can be seen in Figure 10.15. Almost symmetrical V_{th} values have been obtained for *n*MOSFET and *p*MOSFET.

In order to completely eliminate Fermi level pinning, the introduction of metal gate technology is necessary. Recently, there has been much research to find suitable metal gate electrode materials. The elimination of boron penetration and gate depletion is another important benefit of metal gate technology. The material selection of metal gates having comparable workfunction to conventional poly-Si is the most significant issue. Figure 10.16

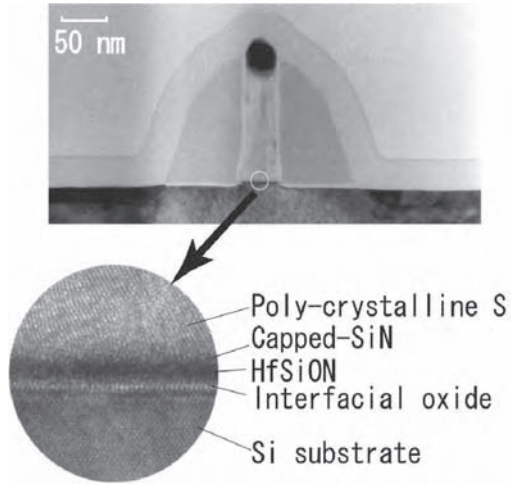

Figure 10.13 TEM cross-sectional photograph of SiN-capped HfSiON and poly-Si gate stack [15]. (Copyright (2004) IEEE)

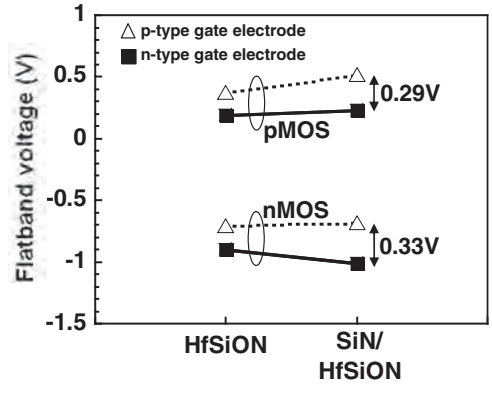

Figure 10.14 Suppression of Fermi level pinning in SiN-capped HfSiON [15]. (Copyright (2004) IEEE)

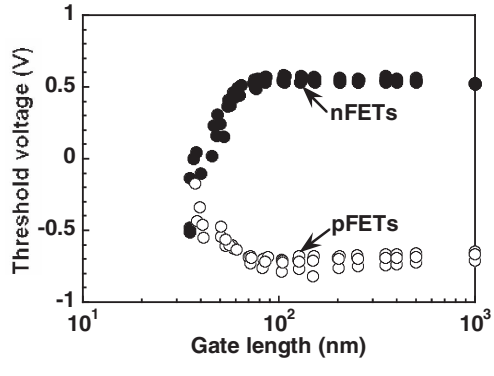

Figure 10.15 V_{th} lowering characteristics with SiN-capping and counter-doping, for poly-Si gate HfSiON MOSFETs [15]. (Copyright (2004) IEEE)

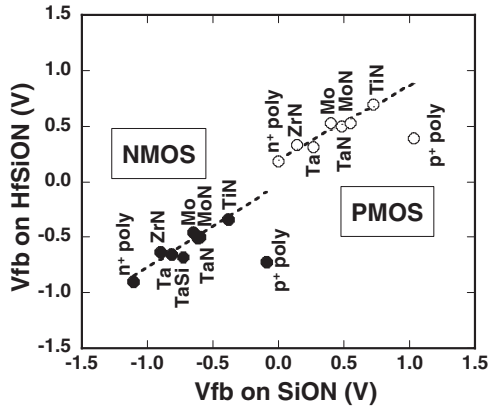

Figure 10.16 Relationship between V_{fb} of SiON and HfSiON MOSFETs for various metal gate materials [17]. (Reproduced by permission of the Japan Society of Applied Physics)

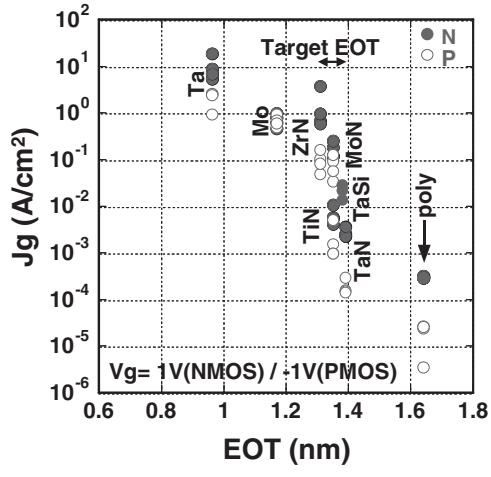

Figure 10.17 EOT–leakage current J_g characteristics for various metal gate materials [17]. (Reproduced by permission of the Japan Society of Applied Physics)

shows the relationship between flatband voltages for SiON and HfSiON MOSFETs [17]. In this case, TiN seems to be suitable for *p*MOS and Ta or ZrN for *n*MOS, from the view point of V_{fb}. When the EOT/leakage current J_g characteristics are considered, however, the Ta gate exhibited EOT thinning after MOSFET fabrication process, as shown in Figure 10.17. This is probably due to the reaction between the Ta and the HfSiON film during thermal treatment, showing that thermal stability is another issue for metal gate technology. Metal silicide or metal nitride films seem more stable, (Figure 10.17), and good subthreshold characteristics for sub-100 nm gate lengths have been obtained with ZrN and TiN *n*- and *p*MOSFETs, as shown in Figure 10.18.

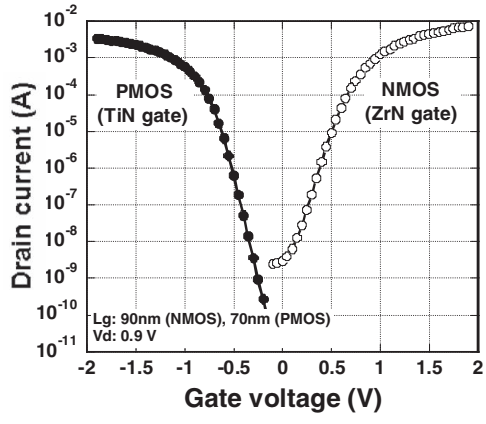

Figure 10.18 Subthreshold characteristics with sub-100 nm gate length MOSFETs with ZrN and TiN metal gates [17]. (Reproduced by permission of the Japan Society of Applied Physics)

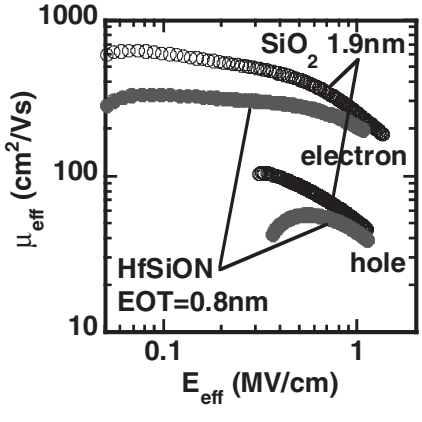

Figure 10.19 Effective electron and hole mobilities for HfSiON MOSFETs with EOT 0.8 nm [12]. (Reproduced by permission of Japanese Journal of Applied Physics)

10.5 INTEGRATION OF 65 NM NODE SRAM HFSION TRANSISTORS

Among the various high-*k* materials, HfSiON is thought to be the most suitable material because it has high thermal stability, good electrical characteristics due to exellent interfacial properties, and leakage current reduction, due to its moderate dielectric constant. HfSiON also has potential usefulness for further scaled devices with smaller EOT, as shown in Figure 10.19, in which high mobility characteristics with an EOT of 0.8 nm is demonstrated [12].

In this final section, integration of an HfSiON transistor into 65 nm node technology is discussed [16]. The device fabrication procedure is as follows. After well and

punch-through stopper implantations, a counter-implant was applied to reduce V_{th} for *p*FETs. $HfSiO_x$ was deposited by MOCVD after the interfacial oxide formation, which was followed by O_3 and NH_3 post-deposition anneals. A 65 nm node CMOS process flow compatible to SiON gate stacks has been adopted, in which the activation anneal was performed with the combination of flash-lamp annealing and conventional spike-RTA (rapid thermal annealing)[18]. Ni was used for salicidation. Three-level Cu interconnects with CVD SiOC interlayer dielectric was fabricated for SRAM array. Figure 10.20 shows I_{on}–I_{off} of *n*FETs and *p*FETs, fabricated with a low thermal budget. I_{on} is 350 μA/μm for *n*FETs, and 150 μA/μm for *p*FETs, respectively, at I_{off} of 20 pA/μm and 1.1 V supply voltage. V_{th} roll-off of the optimized transistors is shown in Figure 10.21. Symmetrical V_{th} values (±0.2 V) have been obtained at L_g = 50 nm for *n*FET and *p*FET. Figure 10.22 shows the cell layout and cross-sectional TEM image of the array transistor. The design rule is 65 nm, in which the gate pitch is 190 nm. The SRAM sell size is $0.56 \times 1.98 = 1.11\,um^2$ and the bit density is 1 Mbit. The relationship between SRAM bit yield and supply voltage is shown in Figure 10.23. The bit yield drops abruptly with the reduction of supply voltage unless the pFET's V_{th} is adjusted to be low.

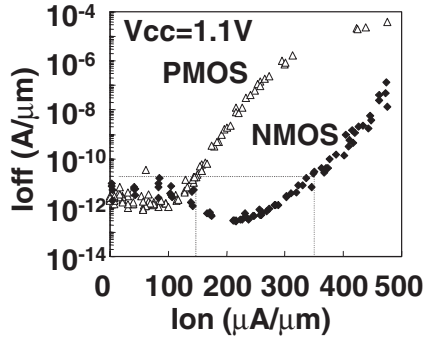

Figure 10.20 I_{on}–I_{off} characteristics for HfSiON MOSFETs with low thermal budget device design [16]. (Copyright (2004) IEEE)

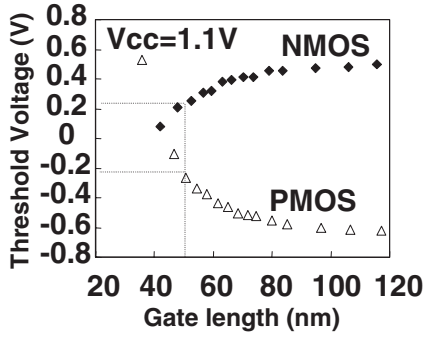

Figure 10.21 V_{th} roll-off characteristics for optimized HfSiON MOSFETs, in which symmetrical V_{th} was obtained for *n*- and *p*MOSFETs at gate length 50 nm [16]. (Copyright (2004) IEEE)

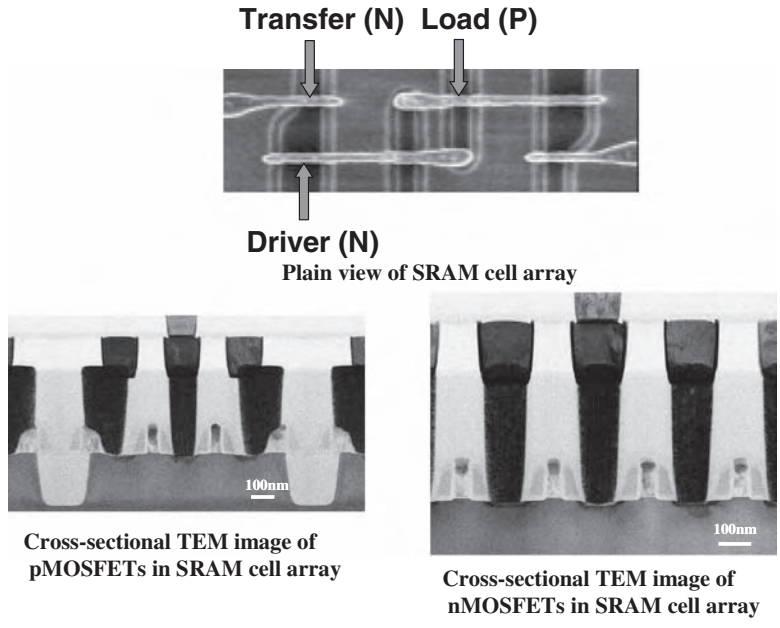
Transfer (N) Load (P)
Driver (N)
Plain view of SRAM cell array
100nm
Cross-sectional TEM image of pMOSFETs in SRAM cell array
100nm
Cross-sectional TEM image of nMOSFETs in SRAM cell array

Figure 10.22 Micrographs of SRAM cell array with poly-Si gate HfSiON MISFETs [16]. (Copyright (2004) IEEE)

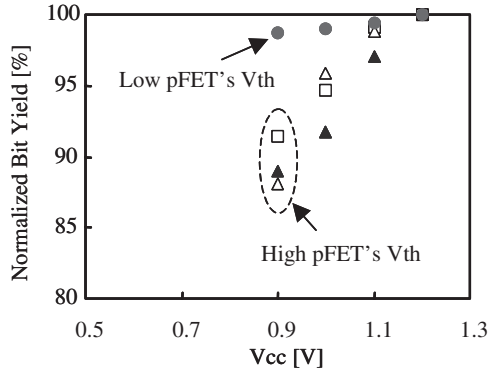

Figure 10.23 Relationship between SRAM bit yield and supply voltage [16]. (Copyright (2004) IEEE)

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11 Anisotropic Conductive Film (ACF) for Advanced Microelectronic Interconnects

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11.1 INTRODUCTION

Recent advances in high-performance low-cost consumer products such as cell phones, laptop computers, electronic toys and personal digital assistants (PDAs), etc., are due to the advances of the microelectronic packaging which interconnects high-performance integrated circuits (ICs) and other discrete components (i.e., resistors, inductors and capacitors) on a common printed circuit board substrate to form an electronic system. Tin–lead solder alloys are widely used interconnect materials in most areas of electronic packaging, such as pin-through hole (PTH), surface mount technology (SMT), ball grid array (BGA) package, chip-scale package (CSP), and flip-chip technology [1, 2] (Figure 11.1). There are increasing concerns about the use of tin–lead alloy solders. First, tin–lead solders contain lead, a material hazardous to human and environment [3]. Each year, thousands tons of lead are manufactured into electronic products, especially consumer electronics. Most of these products have a short life cycle and often end up in landfills within a few months or years. In response to the concerns for the environment and human health, Japan has required all new electronic products to be lead-free since January 2005; the European Union (EU) has also introduced legislation to ban lead-containing electronics by 1 July 2006. In response to the new legislation, most major electronic manufacturers have stepped up their search efforts for alternatives to lead-containing solders.

To date, these efforts have focused on two alternatives: lead-free solders and polymer-based electrically conductive adhesives (ECAs) [4, 5, 6]. The most promising lead-free alloys contain tin as the primary element, because it melts at a relatively low temperature (232°C) and easily wets other metals which are used in most electronic interconnects. Depending on the applications, a number of lead-free solder alloys have found their way into commercial products [7, 8]. However, most currently commercial lead-free solders, such as tin/silver (Sn/Ag), tin/silver/copper (Sn/Ag/Cu), have higher melting temperatures than that of tin–lead eutectic solder (183°C), typically at least 30°C higher. Therefore, the reflow temperature during electronic assembly must be raised by 30–40°C. This increased

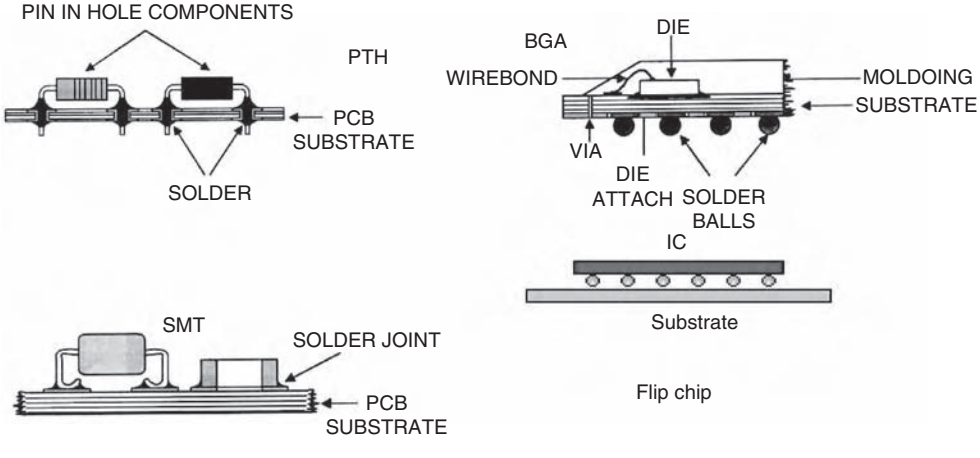


Figure 11.1 Schematic structures of PTH, SMT, BGA and flip chip packages using solder interconnects

temperature reduces the integrity, reliability and functionality of the printed wiring board substrates, and other attached components, as such, severely limits the applicability of these metal alloys to organic/polymer packaged components and low-cost organic printed circuit boards. Although some low-melting-point alloys are available such as Sn/In (tin/indium, T_m = 120°C), Sn/Bi (tin/bismuth, Tm = 138°C), Sn/Zn/Ag/Al/Ga (Tm = 189°C) [9, 10], their material properties and processibility in the SMT assembly are still of concern.

One the other hand, electrically conductive adhesives (ECA) can be processed at a much lower temperature. ECAs mainly consist of an organic/polymeric binder matrix and metal filler. These conductive particle-filled dielectric composite materials provide both physical adhesion and electrical conductivity. Compared with the solder technology, ECA offers numerous advantages, such as environmental friendliness, low processing temperature, few processing steps (reducing processing cost), and especially, the fine pitch capability due to the availability of small-sized conductive fillers, especially for anisotropic conductive adhesives or films (ACA or ACF) [11, 12, 13].

ECA can be categorized with respect to conductive filler loading level into anisotropically conductive adhesives (ACA, typically with 3–5 μm sized conductive fillers, or sometimes in film form, ACF) and isotropically conductive adhesives (ICA, with 5–10 μm sized fillers), which are shown in Figure 11.2 (a, b) [11, 13]. The difference between ACA and ICA is based on the percolation theory (Figure 11.3). The percolation threshold depends on the shape and size of the fillers, but is typically of the order of 15–25% volume fraction when filler size is a few micrometers of Ag flakes [14, 15]. For ICA, the loading level of conductive fillers is much more than the percolation threshold, providing electrical conductivity in *x*, *y* and *z* directions. For ACF, on the other hand, the loading level of conductive fillers is far below the percolation threshold, and the low volume loading is insufficient for inter-particle contact which prevents conductivity in the *x*–*y* plane of the adhesive dielectrics. Therefore, in the *x*–*y* plane, ACF exhibits excellent dielectric properties. High-performance dielectric polymers such as epoxies or polyimides are commonly used for this type of application. The electrical conductivity is restricted to the vertical or *z*-axis. Both adhesive types are being adapted as interconnect materials for surface mount technology

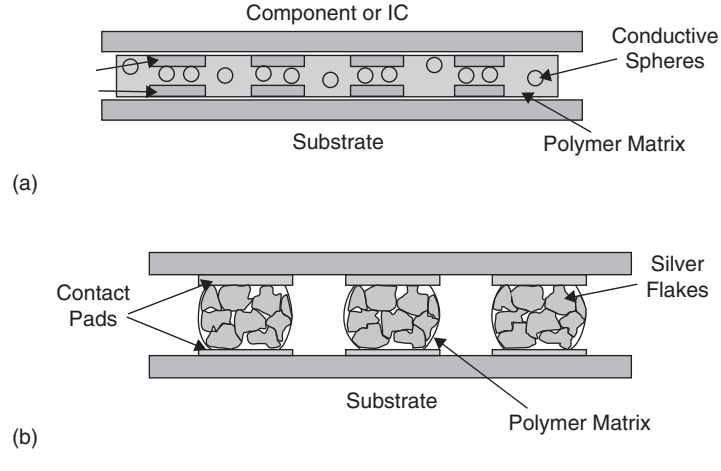
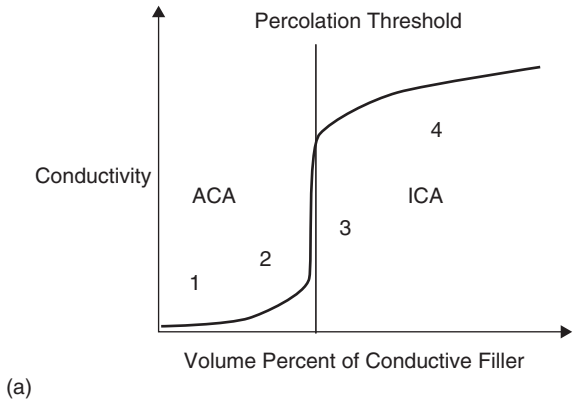
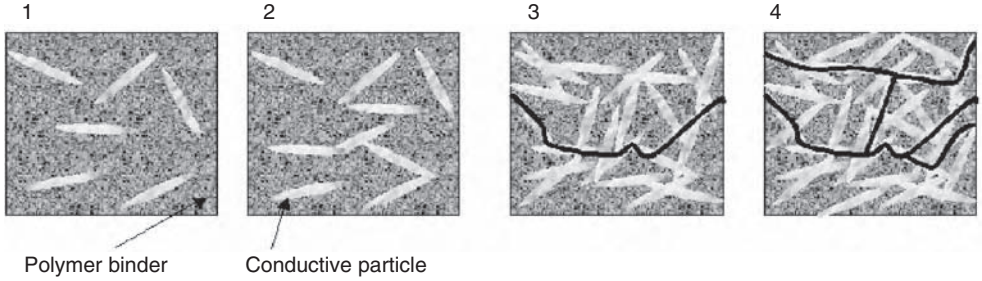


Figure 11.2 Schematic illustrations of: (a) ACA; (b) ICA in flip-chip bonding



(a)



(b)

Figure 11.3 Percolation of conductive filler-filled polymer composite materials: (a) a typical percolation curve showing the abrupt drop in resistance at the percolation threshold; (b) schematic representatives of percolation phenomena

(SMT) processes, such as chip-on-glass (COG), chip-on-flex (COF) and flip-chip bonding technologies in electronic packaging industries where most of the high-performance, low-cost consumer products are assembled by the SMT process. In this chapter, applications and recent advances of anisotropic conductive adhesives or films (ACA or ACF) are reviewed.

11.2 MATERIALS

In general, ACA materials are prepared by dispersing electrically conductive particles in an adhesive dielectric matrix at a concentration far below the percolation threshold. The concentration of conductive particles is controlled such that enough particles are present to assure reliable electrical conductivity between assembled parts in the z direction while too few particles are present to achieve conduction in the x–y plane, which has maintained an excellent dielectric property in the x–y plane of the ACF. Usually, heat and pressure is applied to the composite film to cure the resin while at the same time compressing the conductive particles to generate more contact area in forming interconnections between the conductive bumps on the IC and the conductive tracks or pads on the substrate. As such,

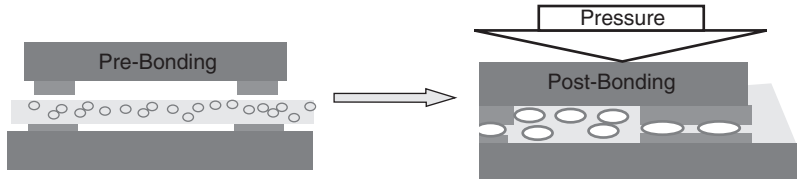


Figure 11.4 Schematic diagram of accomplishment of z direction interconnects using ACF

current only flows normal (in the z direction) to the substrate, hence the name 'anisotropic' conductive adhesive. Figure 11.4 shows the configuration of a component and a substrate bonded with ACF. Once the electrical continuity is produced, the polymer binder is hardened by thermally initiated chemical reaction (cross-linking for thermosets) or by cooling (solidification for thermoplastics). The hardened dielectric polymer matrix holds the components and substrate together and helps maintain the compressive contact between component surfaces, conductive particles and the substrate. Because of the anisotropy, ACA/ACF may be deposited over the entire contact region, greatly facilitating materials application. Also, an ultra-fine pitch interconnection (<0.04 mm) can be achieved easily by employing nano-size conductive particles. The fine pitch capability of ACA/ACF would be limited by the particle size of the conductive filler, which can be a few micrometers to a few nanometers in diameter.

11.2.1 Adhesive matrix

Two basic types of adhesives are available: thermosetting and thermoplastic materials [16]. Thermoplastic adhesives such as high-performance preimidized polyimides, liquid crystal polymers (polyetheretherketones, polysulfones, polyphenylenes, etc.) are rigid materials at temperatures below the glass transition temperature T_g of a polymer. Above the T_g, polymers exhibit flow characteristics. When using this type of material, assembly temperatures must exceed T_g to achieve good adhesion. The principal advantage of the thermoplastic adhesives is the relative ease with which the interconnection can be disassembled for repair operations. However, thermoplastic binder will soften or melt if heated to a high enough temperature, and is therefore somewhat limited in service temperature performance. Thermoplastics also have a tendency to flow under the application of force, i.e., cold flow or creep. Thermosetting adhesives, such as epoxies, polyimides, benzocyclobutenes, polyolefins and silicones, form a three-dimensional cross-linked network structure when cured under prescribed conditions. Curing techniques include heat and UV light. As a result of this irreversible cure reaction, the initial non-cross-linked material is transformed into a rigid solid. The curing reaction is not reversible. This fact may hinder disassembly and interconnection repair. The ability to maintain strength at high temperature and the deformation of robust adhesive covalent chemical bonds are the principal advantages of these materials. For the selection of the adhesive, excellent adhesive bonds should be formed to all surfaces involved in the interconnection. Numerous materials surfaces can be found in microelectronic product interconnection such as SiO_2, Si_3N_4, SiOH (as device passivation layer materials), polyimide, epoxies printed circuit board FR-4, glass, gold, copper, and aluminum. Adhesion to these surfaces must be preserved after standard tests such as temperature–humidity bias

aging and temperature cycling. Some surfaces may require chemical treatments to achieve good adhesion. In addition, the adhesive dielectrics must not contain ionic impurities that would degrade and corrode electrical performance of the interconnections.

11.2.2 Conductive fillers

The materials used as conductive particles must also be carefully selected. Silver (Ag) offers moderate cost, high electrical conductivity, high current-carrying ability—even its oxide is still electrical conductive—and low chemical reactivity. Therefore, silver is the most commonly used conductive filler for ICA. However, problems with electromigration, especially under high bias conditions may occur. Besides silver, gold (Au) is also widely used conductive filler due to its high conductive and inertness nature, However, it is a noble metal and has a high cost. Copper (Cu) due to its high conductivity and low cost appears to be another logical choice, but the challenge of easy oxidation under heat and humidity conditions somewhat limits its wide application in conductive adhesives unless plating or complexing approaches are used. Nickel (Ni) is a lower-cost alternative, but corrosion and oxidation of nickel surfaces has been found during accelerated aging tests. The material that offers the best properties is gold; however, costs may be prohibitive for large-volume applications. Metal- (Ni and Au)-plated polymeric particles may offer the best combination of properties at moderate cost and therefore are commonly used in fine-pitch interconnection. Some ACA/ACF materials use solder (Sn/Pb) particles to ensure electrical contacts with high reliability by creating a metallurgical bond.

11.3 ELECTRICAL PROPERTIES

Anisotropic conductive films (ACFs) are widely used for high density interconnections between LCD (liquid crystal display) panels and TAB (tape-automated bonding) as a replacement for traditional soldering or rubber connections [11, 17, 18]. High connection reliability and very fine pitch interconnections of ACFs have seen rapid development since the progressing of LCD technologies in early 1980s. However, there are some key issues that hinder their implementations as interconnect materials for high-performance devices, such as microprocessor and application-specific integrated circuit (ASIC) applications which require high current-carrying capacity. The ACA/ACF joints have lower electrical conductivity and poor current-carrying capability due with the restricted contact area and poor interfacial bonding of the ACA/ACF and metal bond pads, compared with the metallurgical joint of the metal solders.

11.3.1 Self-assembled monolayer (SAM)

In order to enhance the electrical performance of ACA materials, a class of chemicals that form a self-assembled monolayer (SAM) of conjugated molecular nanowires were introduced. These SAM molecules adhere to the metal surface and form physichemical bonds, which allow electrons to flow more freely; they reduce electrical resistance and enable a high current flow. The unique electrical properties of SAM originate from their linear chain

structure and electron delocalization along the conjugated chain. Preliminary data have also shown that the current density of a SAM molecular wire such as 1,4-benzenedithiol can be up to 1×10^8 A/cm^2, so the potential for conductivity improvement and high current density are significant [19, 20, 21]. Figure 11.5 schematically shows the electrical junctions between Au contact pad and Au conductive fillers in an ACF interface with SAM molecular wires.

An important consideration when examining the advantages of SAM compounds pertains to the affinity of SAM compounds to specific metal surfaces. Table 11.1 gives examples of the SAM molecules preferred for maximum interactions with specific metal finishes; although only molecules with symmetrical functionalities for both head and tail groups are

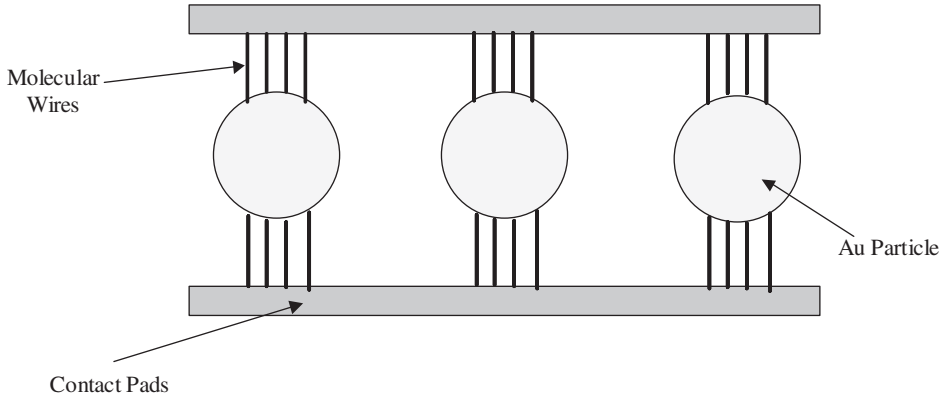
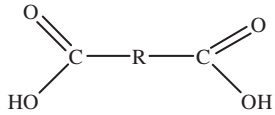
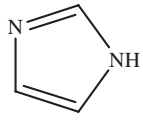


Figure 11.5 Schematic of electrical junction between Au contact pad and Au conductive filler in ACF

Table 11.1 Potential SAM interfacial modifier for different metal finishes

Formula	Compound	Metal finish
H–S–R–S–H	Dithiol	Au, Ag, Sn, Zn
N≡C–R–C≡N	Dicyanide	Cu, Ni, Au
O=C=N–R–N=C=O	Diisocyanate	Pt, Pd, Rh, Ru
	Dicarboxylate	Fe, Co, Ni, Al, Ag
	Imidazole and derivatives	Cu

R denotes alky and aromatic groups

shown, molecules and derivatives with different head and tail functional groups are possible for interfaces concerning different metal surfaces.

Different types of SAMs have been employed to treat different metal surfaces and the results show that SAM molecules can readily adhere to metal surfaces. The change of contact angle on metal surfaces after treatment indicates the coating of SAM on the metal surfaces [22]. Figure 11.6 shows contact angle values of DI (deionized) water droplet on gold surfaces as a function of treatment time with different SAM compound solutions of octadecanethiol (ODT), mercaptoacetic acid (MAA) and 1,4-benzenethiol (Dithiol). For hydrophobic ODT-treated Au surfaces (Figure 11.6a), the contact angles increased with treating time dramatically, while for hydrophilic MAA- and dithiol-treated Au surfaces, an obviously decreased contact angle was observed (Figures 11.6b, c). The results indicated that the thiol molecules were coated on the Au surface, because the S–H functional group chemically anchored on the Au surface and the other terminal material groups contacted the water droplets, changing the contact angles. Different weight losses for the untreated and treated metal particles from thermogravimetric analysis (TGA) give proof of the coating on particles. In addition, Fourier transform infrared with attenuated total reflection (FTIR

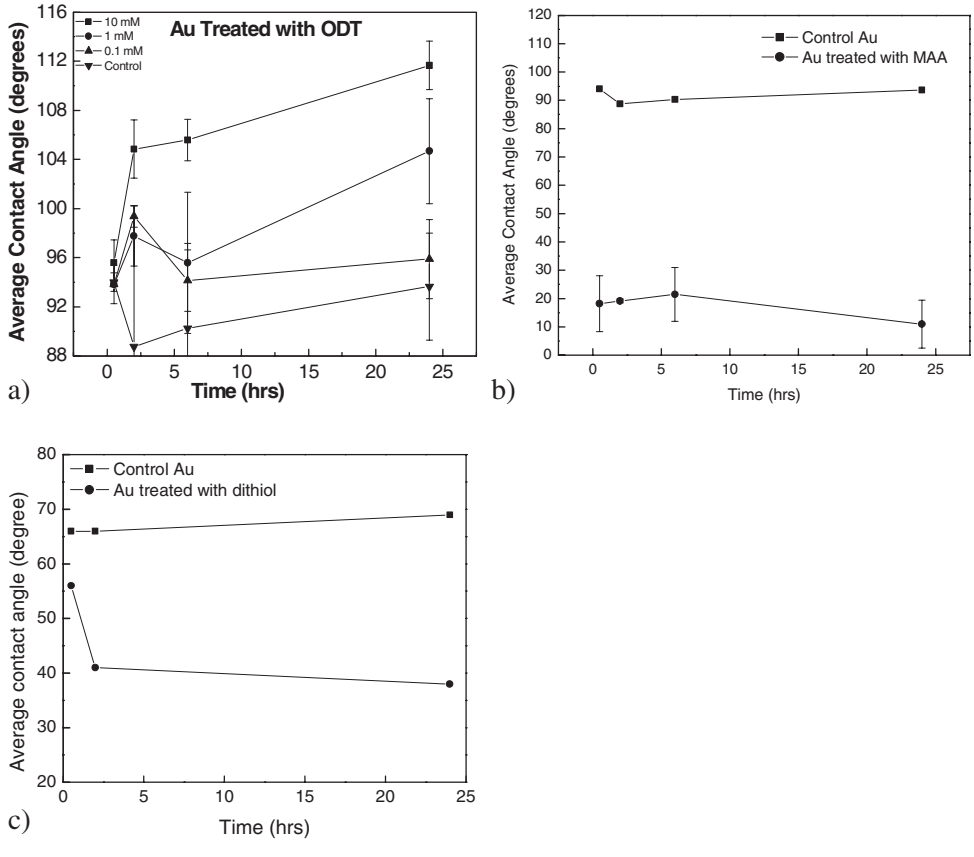


Figure 11.6 Contact angle values of DI water droplets on the Au surfaces treated with different SAMs as a function of the treating time: (a) in ODT solutions; (b) in MAA solutions; (c) in dithiol solutions [22] (Reproduced with permission from the Mineral, Metals and Materials Society)

and FTATR) spectroscopy and X-ray photoelectron spectroscopy (XPS) spectrum can also be utilized to study the chemical status of the monolayers.

11.3.2 Thermal behavior of monolayer coating

The thermal stability of the SAM nanomolecular coating will be a critical issue regarding its practical use because the SAM coating will be used to improve the interface between conductive adhesive joints. A study [22] showed that the contact angles of all metals remained relatively the same for 2 h when coated with SAM at room temperature and heat-treated at 100°C; however, when heat-treated at 150°C, the contact angles for some SAM-treated surfaces tended to change back to the original values, indicating that the coating of such SAMs suffered degradation at high temperatures (Figure 11.7), and methods to enhance the thermal stability is needed for future research in this area.

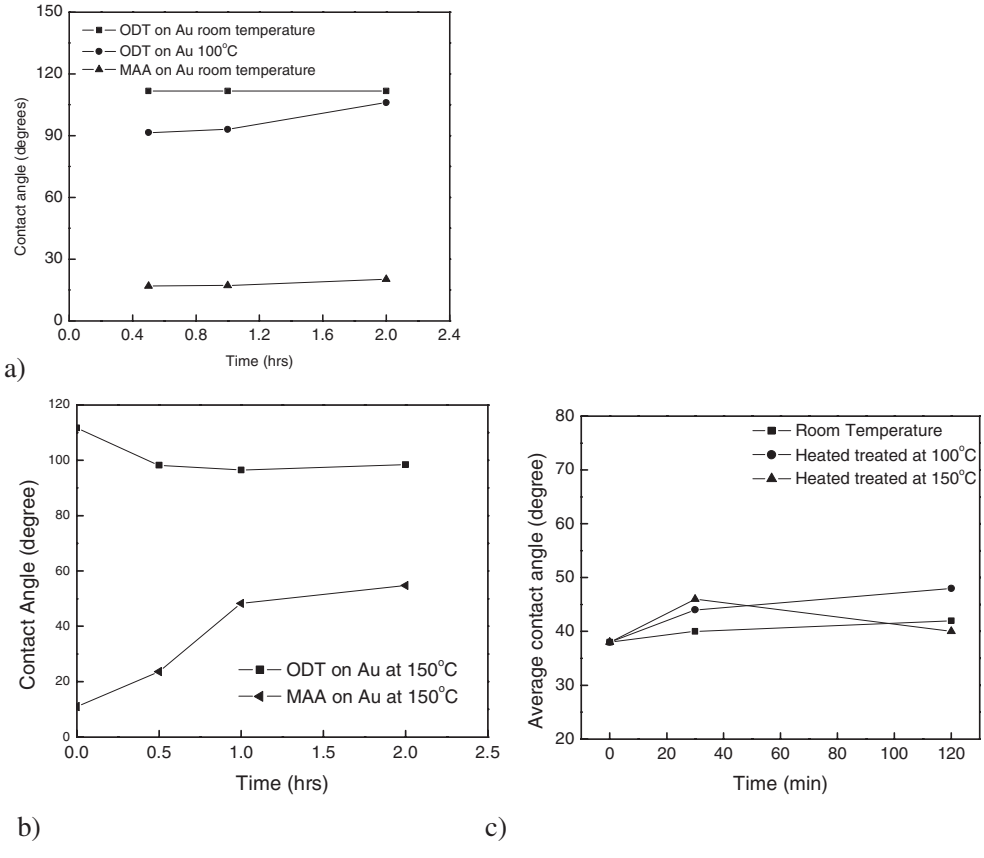


Figure 11.7 Contact angle values of SAMs on gold surfaces as a function of treatment time at different temperatures: (a) ODT- and MAA-treated Au at room temperature and 100°C; (b) ODT- and MAA-treated Au at 150°C; (c) dithiol-treated Au at room temperature, 100°C and 150°C [22] (Reproduced with permission from the Minerals, Metals and Minerals Society)

11.3.3 Electrical properties of ACA with SAM

Different SAM compounds, dicarboxylic acids and dithiols have been introduced into ACA joints for silver-filled and gold-filled ACAs [22, 23]. Due to the strong affinity and selectivity between those SAM compounds and metal fillers and metal bond pads, physichemical bonding was introduced on the interface between the metal particles and between the ACAs/metal bond pads. The physichemical bonding could allow electrons to flow freely, as such, the molecules can reduce electrical resistance and achieve a high current density in the interface. For dithol-incorporated ACA with micrometer-sized gold-coated polymer fillers, significantly lower joint resistance and higher maximum allowable current (highest current applied without inducing joint failure) was achieved for low-temperature curable ACA (<100°C). For high-curing-temperature ACA, (150°C), the improvement is not as significant as low-curing-temperature ACAs, due to the partial degradation of SAM compounds at the relatively high temperature (Figure 11.8). However, when dicarboxylic acid or dithiol was introduced into the interface of nano-silver-filled ACA, significantly improved electrical properties could be achieved at high-temperature-curable ACA, suggesting debonding/degradation of SAM did not occur on silver nanoparticles at the curing temperature (150°C, Figure 11.9). The enhanced bonding could be attributed to the larger surface area and higher surface energy of nanoparticles, which enabled the SAMs to be more readily coated on the metal surfaces [23]. Furthermore, the dicarboxylic acid or dithiol SAM compounds can also react with the polymer dielectric matrix to enhance the polymer–filler interaction which would further improve the performance of the ACA.

11.3.4 Thermal conductivity of ACA

For the ACA interconnect joints to deliver high current, not only a low electrical resistance, but also a high thermal conductivity of the interconnect materials is required. The higher

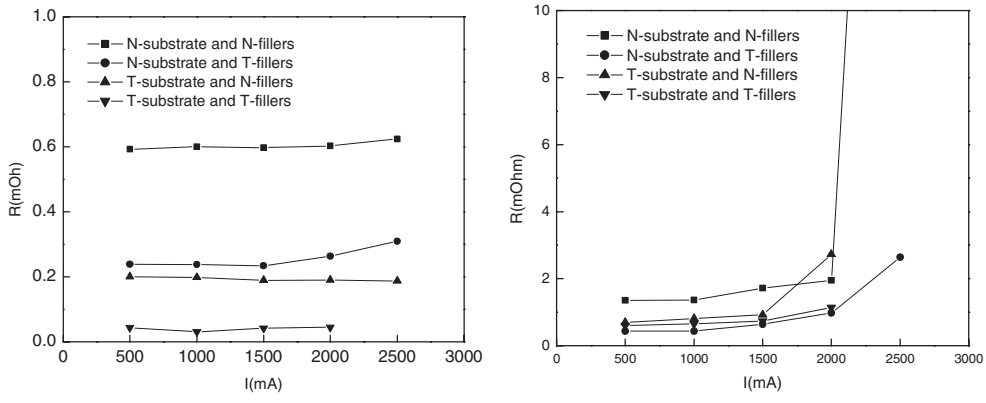


Figure 11.8 Electrical properties of micro-sized gold-filled ACA joints with dithiol. (a) low curing temperature (75°C) ACA; (b) high curing temperature (150°C) ACA [22] (Reproduced with permission from the Minerals, Metals and Materials Society)

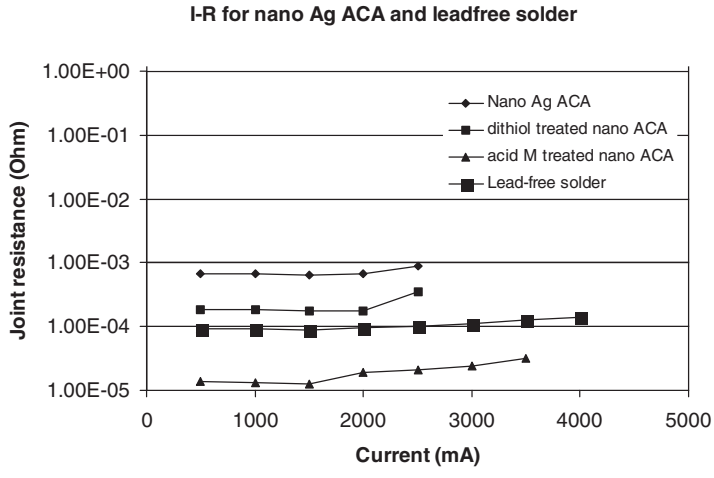


Figure 11.9 Electrical properties of nano-Ag-filled ACA with SAM and lead-free solder (tin–silver–copper) [23] (Reproduced with permission from the Minerals, Metals and Materials Society)

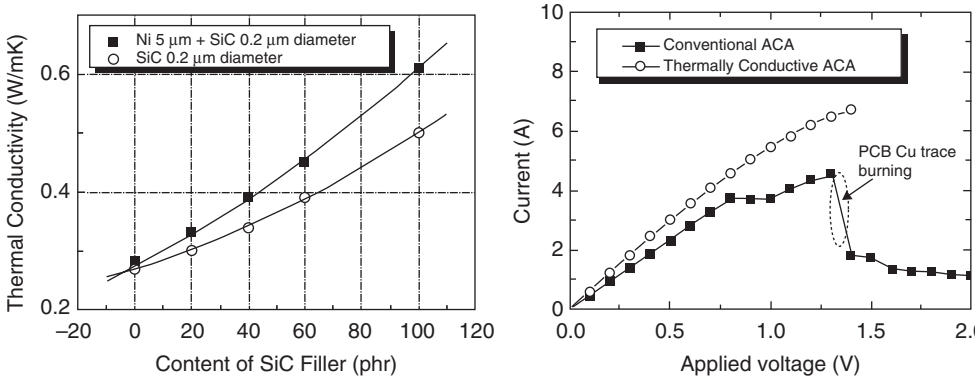


Figure 11.10 Thermal conductivity and *I–V* measurement of ACA with high-thermal-conductivity fillers [24] (Reproduced with permission from the Minerals, Metals and Materials Society)

thermal conductivity can help dissipate heat more effectively from adhesive joints generated at high current. Therefore, a higher thermal conductivity could contribute to an improved current-carrying capability. With the introduction of suitable SAM treatment, an improved interface property between metal fillers and polymer resins could be achieved, which enhanced the thermal conductivity of ACA joints. Studies show that SAM-enhanced ACA joints with the best electrical properties also had a higher thermal conductivity. Reports also show that with the addition of high-thermal-conductivity fillers (e.g., SiC, AlN) into the ACA formulation, the higher thermal conductivity could be achieved, which also rendered a high current-carrying capability [24] (Figure 11.10). Furthermore, carbon nanotubes, with high thermal conductivity (>3000 W/mK from theoretical calculations) can also be aligned within the composite matrix to enhance the thermal conductivity.

11.3.5 Low-temperature sintering of nano-Ag-filled ACA

One of the concerns for ACA/ACF is the higher joint resistance, since interconnection using ACA/ACF relies on mechanical contact, unlike the metal bonding of soldering. An approach to minimize the joint resistance of ACA/ACF is to make the conductive fillers fuse each other and form metallic joints such as metal solder joints. However, to fuse metal fillers in polymers does not appear feasible, since a typical organic printed circuit board, on which the metal-filled polymer is applied, cannot withstand such a high temperature; the melting temperature T_m of Ag, for example, is around 960°C. Research showed that T_m and sintering temperatures of materials could be dramatically reduced by decreasing the size of the materials [25–27]. It has been reported that the surface premelting and sintering processes are a primary mechanism of the T_m depression of the fine nanoparticles [26]. For nano-sized particles, sintering behavior could occur at much lower temperatures, as such, the use of the fine metal particles in ACAs would be promising for fabricating high electrical performance ACA joints through eliminating the interface between metal fillers. The application of nano-sized particles can also increase the number of conductive fillers on each bond pad and result in more contact area between fillers and bond pads. Figure 11.11 shows the SEM photographs of nano-Ag particles annealed at various temperatures. Although very fine particles (20 nm) were observed for as synthesized (Figure 11.11a) and the 100°C-treated particles (Figure 11.11b), dramatically larger particles were observed after heat treatment at 150°C and above. With increasing temperatures, the particles became larger and appeared as a solid matter rather than porous particles or agglomerates. The particles shown in Figures 11.11 (c–e) were fused through their surface and many of dumbbell type particles could be found. The morphology was similar to a typical morphology of an initial stage in the typical sintering process of ceramic, metal and polymer powders. This low-temperature sintering behavior of the nanoparticles is attributed to the extremely high interdiffusivity of the nanoparticle surface atoms, due to the significantly energetically unstable surface status of the nanoparticles, in particular, nano-sized particles with large proportion of the surface area to the entire particle volume.

For the sintering reaction in a certain material system, temperature and duration are the most important parameters, in particular, the sintering temperature. The current–voltage (I–V) relationship of the nano-Ag-filled ACA is shown in Figure 11.12. As can be seen from the figure, with increasing curing temperatures, the resistance of the ACA joints decreased significantly, from 10^{-3} to $5 \times 10^{-5}\,\Omega$. Also, higher-curing-temperature ACA samples exhibited higher current-carrying capability than the low-temperature samples. This phenomenon suggested that more sintering of nano-Ag particles and subsequently superior interfacial properties between fillers and metal bond pads were achieved at higher temperatures [28], yet the x–y direction of the ACF maintains an excellent dielectric property for insulation.

11.4 ASSEMBLY

The ACF assembly process requires the application of pressure during adhesive cure. Curing of adhesive needs a standard method to supply the energy and initiate the chemical reaction. Heat is the typical method, but sometimes ultraviolet (UV) radiation is also used to initiate the reaction. These energy sources are easily incorporated into the process. Special equipment is needed to apply pressure during cure. Typically, heat is supplied from

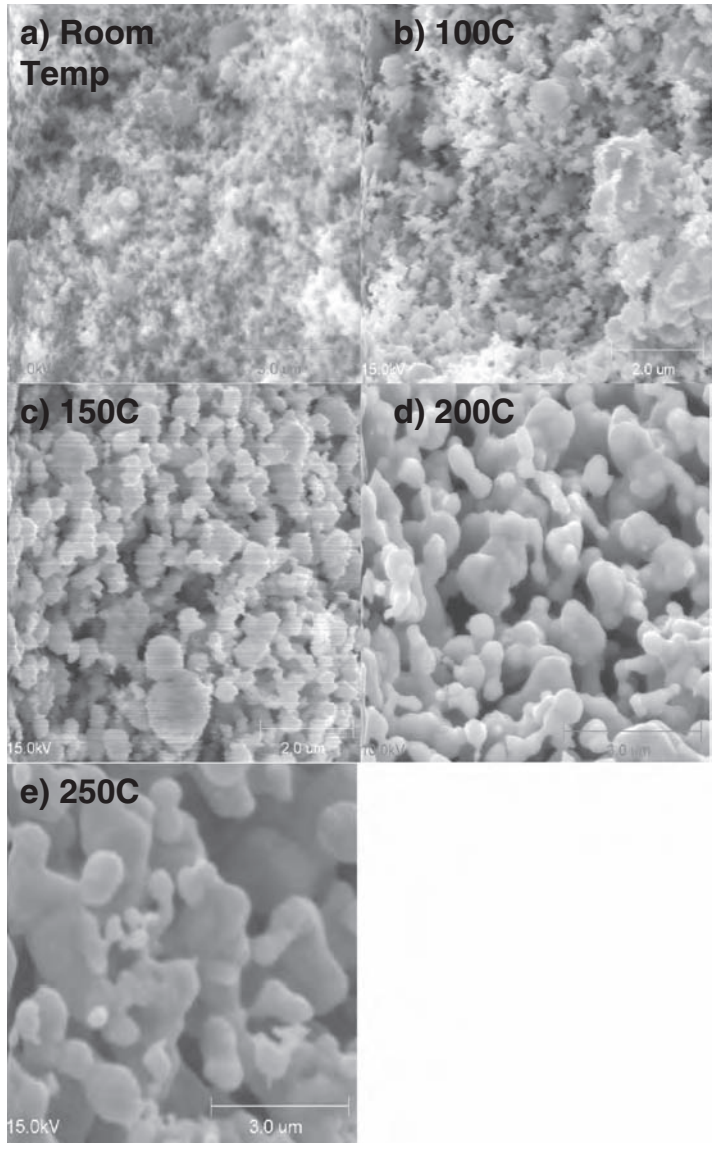


Figure 11.11 SEM photographs of 20 nm-sized Ag particles annealed at different temperatures for 30 min: (a) room temperature (no annealing); (b) annealed at 100°C; (c) annealed at 150°C; (d) annealed at 200°C and (e) annealed at 250°C [25] (Reproduced with permission from the Minerals, Metals and Materials Society)

the thermode used for component pick-up, whereas UV is usually brought through the substrate by optical fiber bundles. Figure 11.13 shows a typical ACF bonding process, a piece of ACF that fits the footprint of the chip or component is placed on the substrate. The chip would be aligned to the contact pads on the substrate prior to being heated and pressed during assembly process. Therefore, an ultra-fine pitch interconnection (<0.04 mm) can be

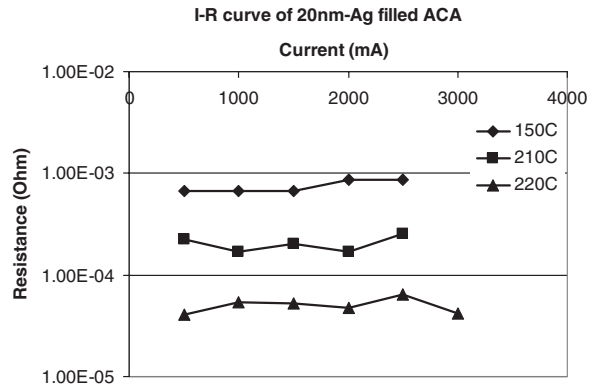


Figure 11.12 Current–resistance relationship of nano-Ag-filled ACAs with different curing temperatures [28]

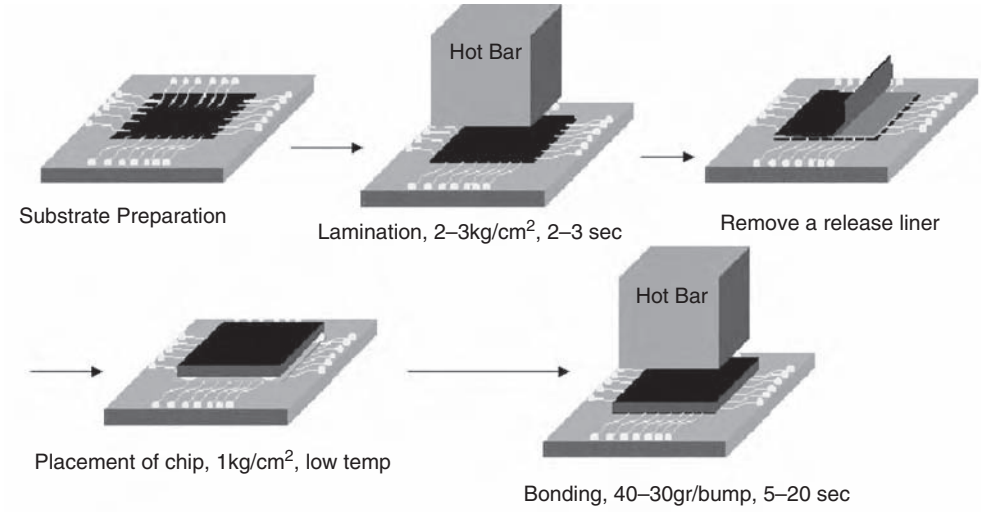


Figure 11.13 Schematic of ACF bonding process

achieved easily using ACF. The fine pitch capability of ACF would be limited by the particle size of the conductive filler, which can be a few micrometers in diameter.

Important process parameters for ACA assembly are temperature, load, tacking time (time needed for the adhesive to soften and flow), and bonding time (final cure time) [11, 29]. For typical ACF processes, one of the interconnecting parts is preheated to a temperature below the ACF bonding temperature, but high enough to partially soften the film so that it has the ability to flow and fill void areas. The bonding load should be high enough to allow the conductive spheres to make good physical contact between conductors, but not high enough to damage any of the parts. Finally, the tacking time should be sufficient to give adequate time for the film to flow before cure begins so that it seals the contact area during the final bonding process. Many parameters can affect the bonding quality during the ACA bonding process, including:

- curing temperature and time of the ACA;
- bonding temperature and time;
- temperature ramp rate;
- alignment accuracy;
- pressure value, pressure distribution and pressure application rate;
- bump height and uniformity;
- board planarity and stiffness of the contact interfaces.

11.5 APPLICATIONS

11.5.1 Application of ACA/ACF in flip-chip

Conventional flip-chip assembly involves two main steps: solder reflow and application of underfill, which is an organic adhesive placed between the IC chip and the substrate to improve mechanical reliability. In recent years, ACA flip-chip technology (where the active IC is bonded face down toward the substrate) has been employed in many applications where flip-chips are bonded to rigid chip carriers [30, 31]. This includes personal digital assistants (PDAs), sensor chip in digital cameras, and memory chips in laptop computers. In all the applications, the common feature is that ACA flip-chip technology is used to assemble bare chips where the pitch is extremely fine, normally less than 100 μm. For those fine applications, it is apparently use of ACA flip-chip instead of soldering is more cost effective.

ACA flip-chip bonding exhibits better reliability on flexible chip carriers because the flex provides compliance to relieve stresses. For example, the internal stress generated during resin curing can be absorbed by the deformation of the chip carrier. ACA joint stress analysis conducted by Wu *et al*. indicated that the residual stress is larger on rigid substrates than on flexible substrates after bonding [32]. Furthermore, the interconnect profile is much smaller, improves the miniaturization of the electronics and reduces the processing temperature; as such, it reduces the thermal stress of the electronic components and enhances the product reliability and performance.

ACF flip-chip interconnection for flip-chip devices

As already stated, ACF provides a simpler flip-chip interconnection process because there is no need for an underfill encapsulant process, compared with solder joints. However, thermal and mechanical stresses and strains induced by CTE (coefficient of thermal expansion) mismatches between the chip and the organic substrates need to be considered in flip-chip interconnections to organic substrates such as FR-4 PCBs (printed wiring boards) and FPCs (flexible printed circuits). In order to apply ACF to flip-chip interconnection to PCBs, the reliability of adhesives resins has been improved by formulating with epoxy resins, modifiers and flexbilizing agents. It is also of concern that contact resistance may not be low since interconnection using ACF relies on mechanical contact, as described

earlier, unlike the metal bonding of soldering. Bonding process parameters such as temperature, pressure and curing time have an important influence on the interconnection resistance between both electrodes. For example, if the bonding temperature is too low, the mechanical contact between bonding electrodes is not maintained. Also, conducting particles dispersed in adhesive films cannot make good electrical contacts with bonding electrodes.

ACF flip-chip interconnection for bumpless devices

ACF can be applied for bumpless flip-chip interconnection to FR-4 PCBs, when bumps are produced on substrate electrodes. The use of bumpless chips allows a reduction in the cost of the flip-chip bonding process, since Au bumping on the chip is not required. For unbumped flip-chips, a pressure-engaged contact must be established by bringing the particles to the aluminum chip pads rather than a bump. The pressure must be sufficient to break the oxide on the aluminum pads. A sufficient quantity of particles must be trapped in the contact pad area and remain in place during bonding and curing to achieve a reliable interconnection. In addition to maximizing the number of particles in the contact area, the number of particles located between adjacent pads must be minimized to prevent electrical shorts. An additional factor that must be taken into account in the case of unbumped flip-chip devices is adhesive flow during bonding and curing. It is essential to control the temperature heating to be sufficiently slow when the polymeric resin is cured so the conductive filler particles can migrate from the chip carrier side to the chip side pad [33].

11.5.2 SMT applications

ACF has been investigated as replacement for SnPb solder in surface mount attachment for fine-pitch applications. The key attractive advantage is the cost effectiveness of using ACF to bond fine-pitch surface mount components. A limitation of ACF is the need to cure under a contact pressure. The concept of using an ACF as a solder replacement on rigid chip carriers utilizing conventional surface mount technology has been demonstrated by J. Liu *et al.* [34]. Fine-pitch SM components were bonded to FR4 boards with ACF using a fine-pitch bonder and then components with larger pitches were bonded with ICAs using standard SM equipment. The study demonstrated that standard surface-mounting tools could be used to assemble conductive adhesives. The connection resistance of solder-plated, plastic components (0.65 mm pitch) with ACF bonding did not change after an accelerated temperature cycling test (ATC) conducted at −40 to 85°C. However, similar parts failed under conditions of −55 to 125°C for 1000 cycles [35]. The mechanical stability problem may have been the result of an improper joint geometry, i.e., not optimized for ACF bonding.

11.5.3 ACF for liquid crystal display (LCD) applications

ACFs have been widely used for packaging technologies in FPDs (flat panel displays) such as LCDs (liquid crystal displays) for the last few decades. So far, various packaging tech-

nologies such as TCP (tape carrier packaging) on LCD panel or printed wiring board (PWB), COF (chip-on-flex) on LCD panel or PWB and COG (chip-on-glass) using ACFs have been realized to meet the requirement of fine pitch capability and make the flat panel displays smaller, lighter and thinner for high-performance consumer products, such as cell phones and laptop computers [18].

Tape carrier packaging (TCP)

Most LCD modules are now assembled by TCP (tape carrier packaging) interconnection technologies using ACFs [36, 37]. The TCP interconnection technologies are divided into a flat type and a bending type. The flat type is advantageous in making the LCD module thinner, but it is disadvantageous in making the frame size smaller. On the other hand, the bending type is advantageous in making the frame size of the modules smaller. When TCP is mounted using ACF onto a LCD panel, the CTE mismatch between the TCP and the panel should be considered for thermal bonding. The TCP extends beyond the panel and the extension will be retained after the adhesive of the ACF is cured. Therefore, the correction value should be considered in design of TCP to conduct the alignment precisely. The fine pitch capability smaller than 50 μm is required in outer lead interconnection of TCP using ACF, as LCD resolution increases.

Chip-on-flex packaging (COF)

Chip-on-flex (COF) is presently the most popular method for packaging LCDs [18, 38]. It uses tape-automated bonding (TAB) of the ICs for connecting the liquid crystal panel and the PWBs in bridge form. With the bridge connection, the peripheral indicator area generally becomes larger. To reduce it, the film carrier is bent 90 or 180°, or into an S-shape. TAB carriers are increasingly being used. Almost 40% of all TAB ICs are used for LCDs. In TAB packaging, a multipin arrangement of up to 200 pins can be realized and the entire process, from testing to assembly, can be accomplished in reel form to increase productivity. In TAB with conventional gang (one-shot) bonding, bonding conditions are difficult to control, and the thermal stress that the chips are subjected to increases with chip size and pin count. Accordingly, single-point TAB bonding is being introduced. For fine-pitch COF packages that use TAB carriers, one may wish to replace conventional mushroom bumps with straight humps, which are formed by using thick resists for electrolytic plating. A two- or three-layer film carrier tape is commonly used. With a two-layer tape that has no bond layer, micropitch connection and fold finishing by inner-lead bonding (ILB) or outer-lead bonding (OLB) are comparatively easy because fine conductors and via holes can be formed by semi-additive electrolytic plating. Etching on the polyimide film is also possible.

The COF technologies using ACF would overcome the limitation of the fine-pitch capability in TCP by using thin Cu (copper) foils and low-CTE-base film materials. Therefore, outer-lead interconnection of COF using ACF has been of much interest because it provides the fine-pitch capability, smaller than 50 μm pitch.

Chip-on-glass (COG) packaging

With COG packaging, bare chips are connected directly to the liquid crystal panel. COG packaging can minimize connection pitch by flip-chip, face-down, IC bonding. This is cost-effective and makes the LCD module smaller and lighter since no materials other than ICs are required. However, COG has a disadvantage in that the mounting of ICs on the LCD panel requires additional area for the IC chips and bus lines, thereby enlarging the peripheral area of the display [39, 40]. Attempts have been made to reduce the area allocated for packaging by concentrating the position of the driver ICs and by changing the IC length-to-width ratio.

11.6 RELIABILITY

The reliability of ACF interconnections depends on the specific formulation, process, substrate and component combination. It is essential to have precise control over the bonding parameters in order to achieve high reliability. Correct curing temperature and pressure are important parameters to form a good adhesive joint. With the use of organic materials such as adhesives, bonds may be electrically unstable at either low or high temperature or in a high-humidity environment, as the adhesive may swell or creep. With the application of ACF interconnection, the failure mechanisms are different from soldered connections. For solder joints, the failure mechanisms are associated with the formation of intermetallic compounds and coarsening of grains. With ACF interconnections, there are two main failure mechanisms that can affect the contacts. The first is the formation of an insulating film on either the contact areas or conductive particle surfaces. The second is the loss of mechanical contact between the conductive elements due to either a loss of adhesion, or relaxation of the compressive force.

The compressive forces acting to maintain contact among the conductive components are partly achieved due to curing shrinkage achieved when curing the polymeric matrix of ACF. Both the cohesive strength of the adhesive matrix and the interfacial adhesion strength between the adhesive matrix and the chip carrier must be sufficient to maintain the compressive force. However, the thermal expansion of adhesives, their swelling due to moisture adsorption, and mechanical stresses due to applied loads tend to diminish this compressive force created as a result of curing. Moreover, water not only diffuses into the adhesive layer, but also penetrates to the interface between adhesive and chip/chip carrier causing a reduction in adhesion strength. As a result, the contact resistance increases and can even result in a complete loss of electrical contact [41]. However, most of these contact resistance increases can be recovered (self-healing) after a drying process. Good dielectric materials such as silicones, benzocyclobutenes can have a 100% desorption properties that can meet the recovery requirement.

Electrochemical (galvanic) corrosion of non-noble metal bumps, pads, and conductive particles results in the formation of insulating metal oxides and significant increase in contact resistance. Electrochemical corrosion only occurs in the presence of moisture and metals that possess different electrochemical potentials. Humidity generally accelerates oxide formation and so too the increase in contact resistance. Reliability test results for flip-chip-on-flex (FCOF) using gold bumps and ACFs filled with Ni particles indicated that the connection resistance increased with time under elevated temperature and humidity

storage conditions [42]. In this case, the gold bump acts as a cathode and the Ni particle as an anode. A nickel oxide, which is electrically insulating, eventually forms on the surface of the Ni particles.

In addition, for very-fine-pitch applications, such as chips with small (<10 μm) bump gap, it becomes more challenging to maintain in-plane electrical insulation. One of the important reliability issues concerning the use of ACF for fine-pitch interconnections is the possibility of short-circuiting between adjacent joints under an applied electric field. Instability of joints is frequently found over time when voltage is applied, particularly in situations where a cluster of conductive particles are trapped between bump gaps. The failure mechanism was considered to be due to the movement of conductive particles at a microscopic level in the presence of applied electric field [43]. However, a good dispersion and high-performance dielectric polymeric materials can prevent this problem.

11.7 FUTURE ADVANCES OF ACF

Significant research has been conducted on ACF as a potential solder replacement for some electronic packaging applications. However, many aspects of this technology such as high current capability/density, self-alignment during the interconnect process, etc., must be better understood before it can be widely used to replace lead-bearing solders. Some critical issues which must be addressed in the future are described.

11.7.1 Materials development

It is important to develop new ACA materials with high-performance dielectric properties, high purity, good adhesion, high T_g, fast curing, storage stability at ambient, and stable contact resistance after various conditions frequently encountered in the field such as thermal aging and cycling, thermal shock, high-temperature/high-humidity/bias, etc. Also, ACAs with low CTE are required. Commercially available ACAs typically exhibit very high CTEs because of the low filler loading levels utilized. Some preliminary studies have shown that ACAs with a low CTE created by introducing nonconductive fused silica fillers (with CTE of 0.5 ppm) have a lower shear strain and better contact resistance stability during the thermal cycling test [44]. In addition to CTE mismatch, the current-carrying capability of ACF needs to be improved for high-power devices applications, such as microprocessor and application-specific integrated circuit (ASIC) applications.

11.7.2 High-frequency compatibility

For wireless/ RF (radiofrequency) electronic applications, a number of high-frequency (in excess of 2.45 to >10 GHz) applications and utilizations are increasing rapidly, thus it is important to characterize the cross-talk between particles, coupling with semiconductor devices and other fundamental behavior of ACAs under high-frequency conditions. It is also necessary to maximize the current-carrying capability of ACAs in the high-frequency range, and after exposure to various environment tests. Good dielectrics with low loss factor tan δ and low dielectric constant k are critically needed.

11.7.3 Reliability

It is necessary to understand the effect of the chip carrier material on ACF join reliability. This is a key issue before ACF technology is widely utilized in manufacturing (i.e., in high-volume and low-cost applications). It is also necessary to establish failure rate prediction models for ACF joints for a wide variety of field conditions. It is essential to gain full understanding of the effects of high current and high power on ACF joints, degradation and stress relaxation of polymeric matrices; and the effects of temperature, humidity, and other environments on matrix materials and the effects of fillers.

11.7.4 Wafer-level application

For the next generation low-cost, high-efficiency ACF assembly, wafer-level application might be a solution. Figure 11.14 shows the process of nano-wafer-level ACF (WLACF) [45]. Instead of using ACF in the assembly process, the ACF is applied on the wafer-level before dicing. This process eliminates the dispensing step in the component level and thus makes the ACF interconnect compatible with standard thermocompression assembly process. The WLACF provides a lead-free and fine-pitch-capable interconnect, as well as a wafer-level package to protect the wafer during test and burn-in. The cost of packaging can be dramatically reduced because it avoids the solder bumping process, combines interconnect and encapsulation, and enables wafer-level test and burn-in. After the chip assembly, the ACF layer also acts as an underfill to redistribute the thermomechanical stress generated from the CTE mismatch between the chip and the substrate.

11.8 CONCLUSION

Applications and recent advances of anisotropic conductive films (ACF) are reviewed in this chapter. ACFs have excellent dielectric properties in the *x*–*y* plane, while the

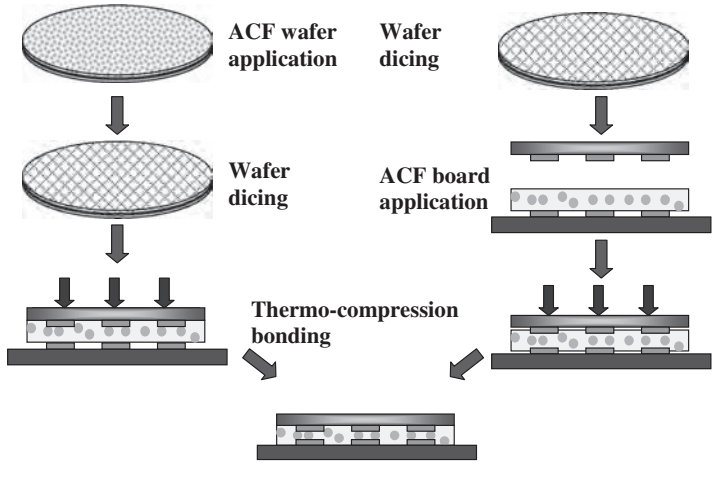


Figure 11.14 Schematic illustration of wafer-level ACF process

electrical conductivity is only restricted to the vertical z axis when pressure and heat are applied during curing of the material are essential. The unique structures and properties enable ACFs to be widely used as interconnect materials for surface mount technology (SMT) processes, such as chip-on-glass (COG), chip-on-flex (COF) and flip-chip bonding technologies in electronic packaging industries where most of the high-performance, low-cost consumer products are assembled. However, some limitations of ACF still hinder their implementations for high-power devices and many efforts have been conducted to address these issues.

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